/VI/IXI/VI

Calibrated 12-Bit ADC with T/H and Reference

MAX178

General Description

The MAX178 is a complete, calibrated 12-bit A/D converter (ADC) which includes a precision voltage reference, track-and-hold, and conversion clock. Internal calibration circuitry maintains true 12-bit performance over the full operating temperature range without external adjustments. In addition, each conversion includes an auto-zero cycle which reduces zero errors to typically below 100µV.

CHIP SELECT, READ, and WRITE inputs are included for easy microprocessor interfacing without additional logic. 2-byte, 12-bit conversion data is provided over an 8-bit three-state output bus. Either byte may be read first. Two converter busy flags facilitate polling of the converter's status.

The MAX178's analog input range is 0V to +5V when using a +5V reference. The MAX178A's internal reference accuracy is ±0.3%, while the MAX178B is intended for use with an external reference.

Applications

Digital-Signal Processing
Audio and Telecom Processing
High-Speed Data Acquisition
High-Accuracy Process Control

Features

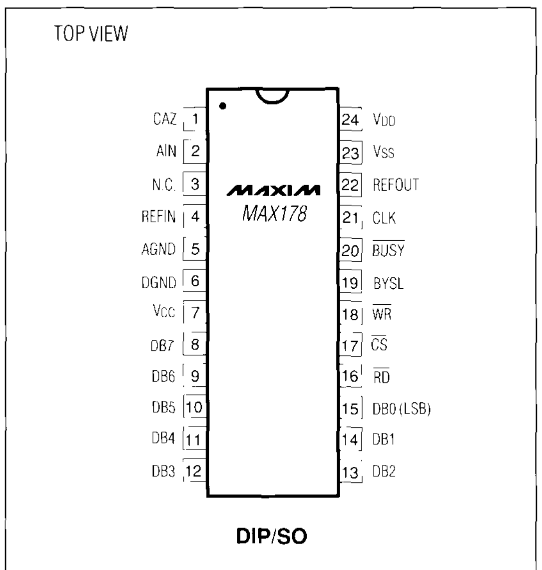
- ♦ Continuous Transparent Calibration of Offset and Gain
- ♦ True 12-Bit *Performance* without Adjustments
- ♦ T/H Front End and Internal Reference
- ♦ DC and Dynamically Specified
- ♦ Zero Error Typically <100µV
- ♦ Standard Microprocessor Interface
- ♦ 24-Pin DIP and Wide SO Packages

Ordering Information

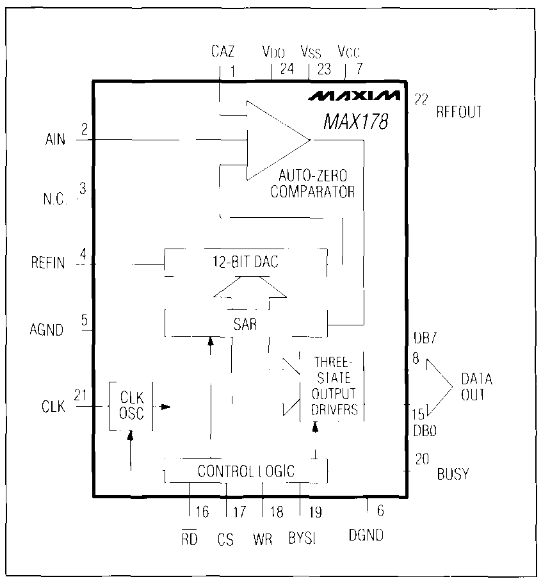
PART	TEMP. RANGE	PIN-PACKAGE
MAX178ACNG	0°C to +70°C	24 Plastic DIP
MAX178BCNG	0°C to +70°C	24 Plastic DIP
MAX178ACWG	0°C to +70°C	24 Wide SO*
MAX178BCWG	0°C to +70°C	24 Wide SO*
MAX178AENG	-40°C to +85°C	24 Plastic DIP
MAX178BENG	-40°C to +85°C	24 Plastic DIP
MAX178AEWG	-40°C to +85°C	24 Wide SO*
MAX178BEWG	-40°C to +85°C	24 Wide SO*
MAX178AMRG	-55°C to +125°C	24 CERDIP
MAX178BMRG	-55°C to +125°C	24 CERDIP

** Consult factory.*

Pin Configuration



Functional Diagram



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ABSOLUTE MAXIMUM RATINGS

V_{DD} to DGND . . . . -0.3V, +17V
V_{SS} to DGND . . . . +0.3V, -7V
AGND to DGND . . . . -0.3V, REFIN +0.3V
V_{CC} to DGND . . . . -0.3V, +7V
REFIN to AGND . . . . -0.3V, V_{DD} +0.3V
AIN to AGND . . . . -0.3V, V_{DD} +0.3V
Digital Input Voltage to DGND . . . . -0.3V, V_{DD} +0.3V
Digital Output Voltage to DGND . . . . -0.3V, V_{DD} +0.3V

Operating Temperature Range
MAX178_C . . . . 0°C to +70°C
MAX178_E . . . . -40°C to +85°C
MAX178_M . . . . -55°C to +125°C
Power Dissipation (any Package)
To +75°C 1,000mW
Derate above +75°C by . . . . 10mW/°C
Storage Temperature . . . . -65°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +15V, V_{CC} = +5V, V_{SS} = -5V, REFIN = +5.0V, all specifications T_A = T_{MIN} to T_{MAX}, f_{CLK} = 266.67kHz external, unless otherwise

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ACCURACY						
Resolution			12			Bits
Total Unadjusted Error (Note 1)	TUE				±1	LSB
Differential Nonlinearity	DNL	No missing codes guaranteed			±1	LSB
Full-Scale Error (Gain Error)		T_A = +25°C			±1/2	LSB
Full-Scale Error Tempco				0.5		ppm/°C
Zero Error		T_A = +25°C			±1/2	LSB
Zero Error Tempco				0.5		ppm/°C
ANALOG INPUT						
Input Voltage Range		V_{REF} = +5V	0		+5	V
On-Channel Input Capacitance	C_{AIN}			8		pF
Input Leakage Current	I_{AIN}	AIN = 0V to +5V: T_A = +25°C T_A = T_{MIN} to T_{MAX}			 10 100	nA
DYNAMIC ACCURACY ($f_{\overline{WR}}$ = 14.81kHz, f_{AIN} = 2.011kHz, T_A = 25°C, Note 2)						
Signal-to-Noise + Distortion	S/(N + D)		70			dB
Total Harmonic Distortion	THD				-80	dB
Peak Harmonic or Spurious Noise					-80	dB
REFERENCE INPUT						
REFIN Range	V_{REFIN}	For specified performance Degraded transfer accuracy	 +4	+5 ±5% 	 +6	V
REFIN Input Current		REFIN = +5V			1.0	mA
REFERENCE OUTPUT						
MAX178A						
REFOUT Voltage		T_A = +25°C	+4.985	+5	+5.015	V
REFOUT Temp (C°)				±10	±40	ppm/°C
REFOUT Sink Current					1	mA
MAX178B						
Use External Reference Only						

ELECTRICAL CHARACTERISTIC (continued)

(V_{DD} = +15V, V_{CC} = +5V, V_{SS} = -5V, REFIN = +5.0V, all specifications T_A = T_{MIN} to T_{MAX}, f_{CLK} = 266.67kHz external, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LOGIC INPUTS						
$\overline{RD}$, CS, $\overline{WR}$, BYSL						
Input High Voltage	V_{IH}	V_{CC} = +5V ±5%	+2.4			V
Input Low Voltage	V_{IL}	V_{CC} = +5V ±5%			+0.8	V
Input Current	I_{IN}	V_{IN} = 0 to V_{CC}; T_A = +25°C T_A = T_{MIN} to T_{MAX}			±1 ±10	µA
Input Capacitance	C_{IN}	(Note 3)			10	pF
CLOCK						
Input High Voltage	V_{IH}	V_{CC} = +5V ±5%	+3.0			V
Input Low Voltage	V_{IL}	V_{CC} = +5V ±5%			+0.8	V
Input High Current	I_{IH}	V_{CC} = +5V ±5%			1.5	mA
Input Low Current	I_{IL}	V_{CC} = +5V ±5%			1.2	mA
LOGIC OUTPUTS						
DB0-DB7, $\overline{BUSY}$						
Output High Voltage	V_{OH}	V_{CC} = +5V ±5%, I_{SOURCE} = 200µA	+4.0			V
Output Low Voltage	V_{OL}	V_{CC} = +5V ±5%, I_{SINK} = 1.6mA			+0.4	V
Floating State Leakage Current (DB0-DB7)	I_{LKG}	V_{OUT} = 0V to V_{CC}			±1	µA
Floating State Output Capacitance (DB0-DB7)	C_{OUT}	(Note 3)			15	pF
CONVERSION TIME (Note 4)						
With External Clock		f_{CLK} = 266.67kHz	60			µs
With Internal Clock		T_A = +25°C	90		140	µs
POWER REQUIREMENTS (Note 5)						
Power-Supply Voltage	V_{DD}		+11.4		+15.75	V
	V_{SS}		-4.75		-5.25	
	V_{CC}		+4.75		+5.25	
V_{DD} Supply Rejection		V_{DD} = +14.25V to +15.75V, V_{SS} = -5V		±1/8		LSB
V_{SS} Supply Rejection		VSS = -4.75V to -5.25V, V_{DD} = +15V		±1/8		LSB
V_{DD} Supply Rejection		V_{DD} = +11.4V to +12.6V, V_{SS} = -5V		±1/8		LSB
V_{SS} Supply Rejection		V_{SS} = -4.75V to -5.25V, V_{DD} = +12V		±1/8		LSB
Power-Supply Current	I_{DD}	V_{IN} = V_{IL} or V_{IH}		6	10	mA
	I_{SS}				8	
	I_{CC}			0.1	1.0	

Note 1: Includes: Full-Scale Error, Offset Error, Relative Accuracy.
Note 2: Up to 5th Harmonic is measured.
Note 3: Guaranteed by design.
Note 4: Track/Hold aquisition time included in conversion time, using t_{13} condition (see Timing Characteristics).
Note 5: Power-supply current is measured when MAX178 is inactive ($\overline{CS}$ = $\overline{WR}$ = $\overline{RD}$ = $\overline{BUSY}$ = High).

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TIMING CHARACTERISTICS (Note 6, Figures 1 and 2)

(V_{DD} = +15V, V_{CC} = +5V, V_{SS} = -5V, REFIN = +5.0V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	T_A = +25°C			T_A = -40°C to +85°C			T_A = -55°C to +125°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
CS to $\overline{WR}$ Setup Time	t_1		0			0			0			ns
$\overline{WR}$ Pulse Width	t_2		120			120			120			ns
$\overline{CS}$ to $\overline{WR}$ Hold Time	t_3		0			0			0			ns
WR to $\overline{BUSY}$ Propagation Delay	t_4			85	120		100	140		115	160	ns
$\overline{BUSY}$ to CS Setup Time	t_5	(Note 3)	0			0			0			ns
$\overline{CS}$ to $\overline{RD}$ Setup Time	t_6		0			0			0			ns
RD Pulse Width	t_7		120			120			120			ns
$\overline{CS}$ to RD Hold Time	t_8		0			0			0			ns
BYSL to RD Setup Time	t_9		50			50			50			ns
BYSL to $\overline{RD}$ Hold Time	t_{10}		0			0			0			ns
RD to Valid Data (Note 7)	t_{11}	(Bus Access Time)		60	100		70	110		90	130	ns
$\overline{RD}$ to Three-State Output (Note 8)	t_{12}	(Bus Relinquish Time)	20		100	20		100	20		100	ns
$\overline{WR}$ to CLK for 16 Clock Conversions (Note 9)	t_{13}		20			20			20			ns
WR to CLK for 17 Clock Conversions (Note 9)	t_{14}		20			20			20			ns

Note 6: Data is timed from V_{OH}, V_{OL}; all input control signals are timed from a voltage level of +1.6V and specified with $t_r = t_f$ = 20ns (10% to 90% of +5V).
Note 7: t_{11}, the time required for an output to cross 0.8V or 2.4V, is measured with the load circuits of Figure 3.
Note 8: t_{12}, the time required for the data lines to change 0.5V, is measured with the load circuits of Figure 4.
Note 9: See Figure 7.

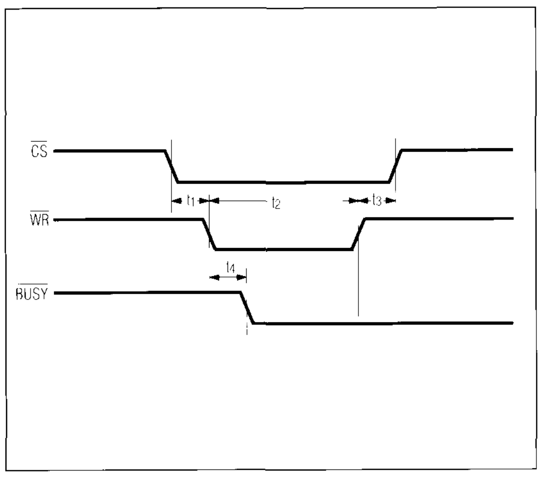

Figure 1: Start Cycle Timing

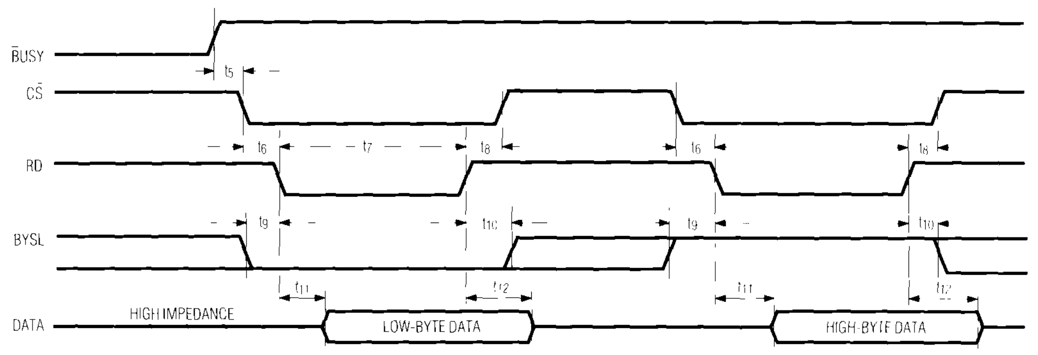

Figure 2. Read Cycle Timing

Pin Description

PIN	NAME	FUNCTION
1	CAZ	Auto-Zero Capacitor Input. Connect other end of capacitor to AGND.
2	AIN	Analog Input
3	N.C.	No Connect
4	REFIN	Voltage Reference Input. The MAX178 is specified with REFIN = +5V.
5	AGND	Analog Ground
6	DGND	Digital Ground
7	V_{CC}	Logic Supply. Digital inputs and outputs are TTL compatible for V_{CC} = +5V.
8-15	DB0-DB7	Three-State Data Outputs. Active when $\overline{CS}$ and $\overline{RD}$ are brought low. Individual pin functions depend upon BYTE SELECT (BYSL) input.

DATA BUS OUTPUT, $\overline{CS}$, $\overline{RD}$ = LOW		
PIN	**BYSL = HIGH**	**BYSL = LOW**
8	BUSY (Note 10)	DB7
9	LOW (Note 11)	DB6
10	LOW (Note 11)	DB5
11	LOW (Note 11)	DB4
12	DB11 (MSB)	DB3
13	DB10	DB2
14	DB9	DB1
15	DB8	DB0 (LSB)

PIN	NAME	FUNCTION
16	$\overline{RD}$	READ Input. Used with CS to enable the three-state data outputs. RD is active low.
17	$\overline{CS}$	CHIP SELECT Input. Used with either $\overline{RD}$ or $\overline{WR}$ for control. $\overline{CS}$ is active low.
18	$\overline{WR}$	WRITE Input. In combination with CS, this active low signal starts a new conversion.
19	BYSL	BYTE SELECT. BYSL selects high- or low-byte output during a data READ operation. (RD, CS = low). See pins 8-15.
20	$\overline{BUSY}$	Converter Status. BUSY is only low during conversion.
21	CLK	CLOCK Input. Internal clock operation, with this pin floating and unloaded, typically results in 120μs conversion time (Figure 8). This can be lowered by using an external 74HC clock source (Figure 9).
22	REFOUT	Reference Output
23	V_{SS}	Negative Supply Voltage, -5V
24	V_{DD}	Positive Supply Voltage, +15V

Note 10: High during a conversion. BUSY is a converter status flag.

Note 11: When BYSL is high, pins 9-11output a logic low. The 12-bit digital result is in DB0-DB11. DB11 is the MSB.

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Detailed Operation

Operating Information

Figure 5 shows an operational diagram for the MAX178. The only required passive components are a hold capacitor (CAZ) and a reference bypass capacitor and resistor. Individual pin functions are listed in the Pin Description table.

On-Chip Clock Operation

The on-chip oscillator requires no external components. Therefore, the CLK pin can be left unconnected resulting in a typical 120µs conversion time. The conversion time can be increased by adding a capacitive load on the CLK pin. The timing diagrams in Figures 6 and 7 show the resulting tracking duration for relative positions of $\overline{WR}$ and CLK. Figure 8 is a schematic for on-chip clock operation.

A new conversion is initiated by bringing $\overline{WR}$ low, with CS low. This starts a track acquisition sequence. In this state, the T/H goes into track mode. Capacitor CAZ charges to the analog input voltage minus the input offset voltage of the comparator. Note: when WR is low (with CS low), the MAX182 is in track mode. When $\overline{WR}$ goes high, tracking time is extended by another 4 to 5 clock periods (4 clock periods beginning with the first falling clock edge following the rising edge of WR). 16 to 17 clock periods are required for each conversion (Figure 7).

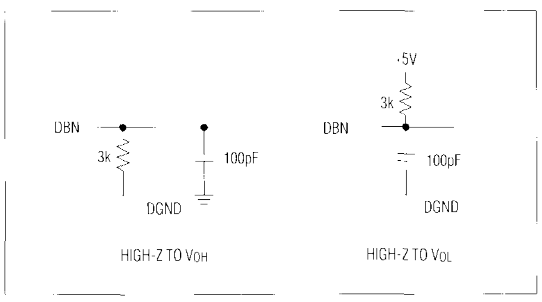

Figure 3. Load Circuits for Access Time Test (t_{11})

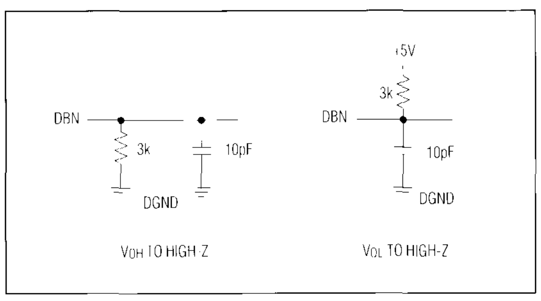

Figure 4. Load Circuits for Output Three-State Delay Test (t_{12})

The MAX178 is in track mode between conversions when $\overline{BUSY}$ is high. After the tracking sequence, the most significant bit (MSB) decision is made. Following this, the remaining 11 bits are digitized on successive clock cycles, as indicated in Figure 6. The WR pulse need not be synchronized with the internal clock.

External Clock Operation

For external clock operation, drive the CLK input with a 74HC compatible clock source (Figure 9).

The MAX178 automatically tracks for the appropriate time by means of an on-chip counter. Both WR and CS must be low to initiate a new conversion. Whenever WR and CS are low, the chip enters into track mode until WR or $\overline{CS}$ rises. After the rising edge of WR, the next falling edge of the clock starts a counter, which extends the tracking time by 4 to 5 external clock periods.

The analog input acquisition is complete at the end of the tracking period, and the signal is stored in the internal track-and-hold. The external clock source need not be synchronized with the WR pulse.

Reading Data

The 12-bit result of a conversion plus the converter status flag are accessible over an 8-bit data bus. The data is available from the MAX178 in right-justified format (the least significant bit (LSB) is the right-most bit in a 16-bit word). Two byte sized read operations are needed. The Byte Select (BYSL) input determines which byte is to be read first, 8LSBs or 4MSBs plus status flag.

It is necessary to wait for the end of a conversion to obtain valid 12-bit data from the MAX178's successive approx-

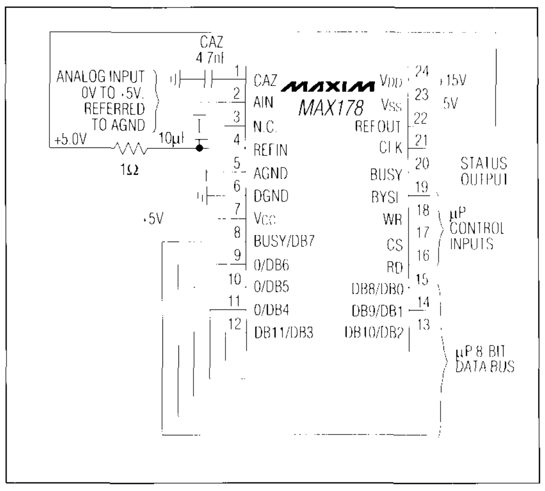

Figure 5. MAX178 Operational Diagram

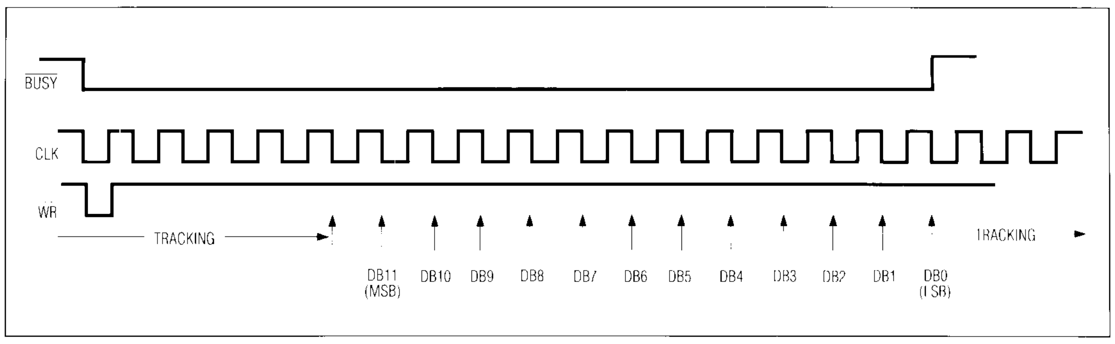

Figure 6. MAX178 Timing Diagram

imation register (SAR). If a read operation instruction is performed during a conversion, the MAX178 will dump the existing contents of the SAR onto the data bus. There are three methods to ensure correct operation:

1. Insert a software delay longer than the ADC conversion time between the conversion start and the data read operations.
2. The $\overline{BUSY}$ output is low during the conversion and high at the conversion end. Use this signal as an interrupt to the µP.
3. Poll the converter status flag, BUSY, at user-defined intervals after a conversion start. The status flag is available on DB7 during a high-byte READ. The flag is the left-most bit and can be shifted directly into the µP's carry flag for testing. BUSY is high during a conversion.

A write operation to the MAX178 during a conversion restarts the conversion.

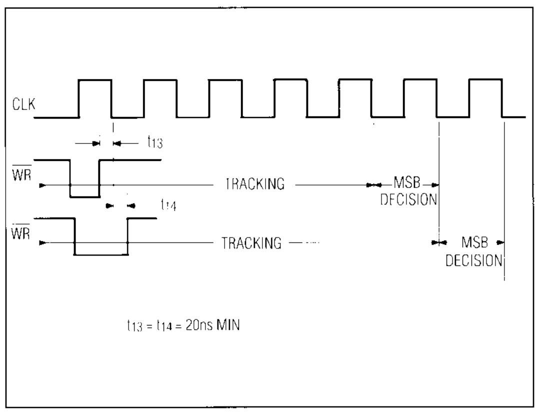

Figure 7. Width of Tracking Interval as a Function of WR Rising Edge Timing with Respect to CLK Falling Edge

Application Hints

Auto-Zero Capacitor (CAZ)

CAZ (Figure 5) must be a low-leakage, low-dielectric absorption capacitor such as polypropylene, polystyrene, or teflon. Connect the outside foil of CAZ to AGND to minimize noise. CAZ should be 4,700pF.

Clock

Figure 10 shows typical conversion time versus temperature when using the MAX178's on-chip clock. Due to variations in manufacturing, the actual operating frequency can differ from chip-to-chip by up to 20%. For this reason, it is suggested that an external clock be used when fixed conversion times are required.

Analog Inputs

The high-impedance analog input, AIN, allows simple analog interfacing. Signal sources from 0V to +5V may be connected directly to AIN without extra buffering for source impedances up to 5kΩ (Figure 11). The input/output (I/O) transfer characteristic and transition points for this input signal range are demonstrated in Figure 12 and Table 1. The MAX178 transfer characteristic has transi-

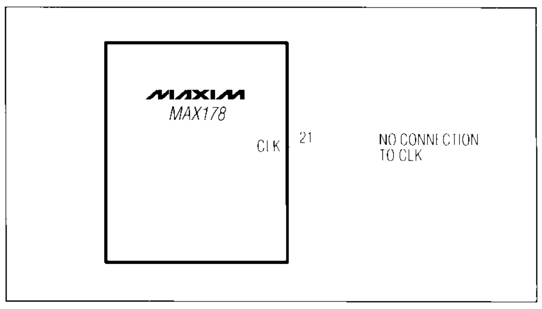

Figure 8. Internal Clock Operation

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tion points designed to occur on integer multiples of 1LSB. The output code is natural binary with:

$$1LSB = (Full\ Scale\ (FS))/4096 = (5/4096)V = 1.22mV.$$

For signal ranges other than 0V to +5V, use resistor divider networks to provide 0V to +5V signal ranges at the MAX178 input pins. The connection in Figure 13 shows a divider network for a 0V to +10V signal range. Resistors should be of the same type and manufacturer to ensure matched temperature coefficients. The source impedance must now be as low as possible since it adds to the resistor divider impedance.

Figure 14 shows how bipolar signals -5V to +5V are accommodated by referencing the resistor divider network to REFIN. The signal source must be capable of sinking 0.5mA with the resistor values shown. Refer to Figure 15 and Table 2 for the I/O transfer characteristic and transition points for this signal range. Output coding is offset binary with an LSB size of:

$$(FS)(1/4096) = (10/4096)V = 2.44mV.$$

To adjust bipolar zero error, apply 1.22mV (+1/2LSB) to AIN and adjust the offset of A1 so that the ADC output switches between 1000 0000 0000 and 1000 0000 0001.

Power-Supply Decoupling

Power supplies to the MAX178 should be bypassed with either a 10µF electrolytic or tantulum capacitor in parallel with a 0.01µF disc ceramic capacitor for clean, high-frequency performance. Place all capacitors as close as possible to the MAX178 supply pins.

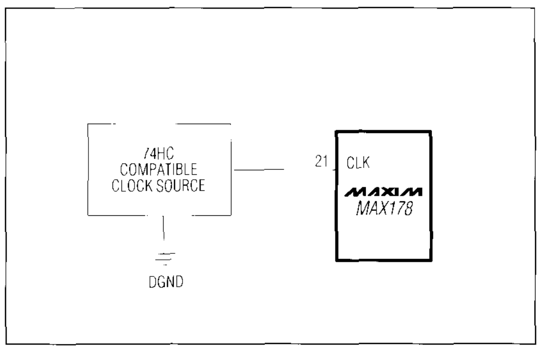

Figure 9. External Clock Operation

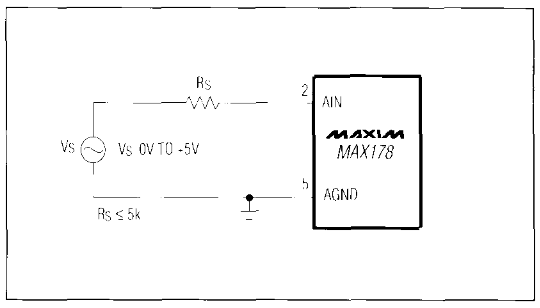

Figure 11. Unipolar 0V to +5V Operation

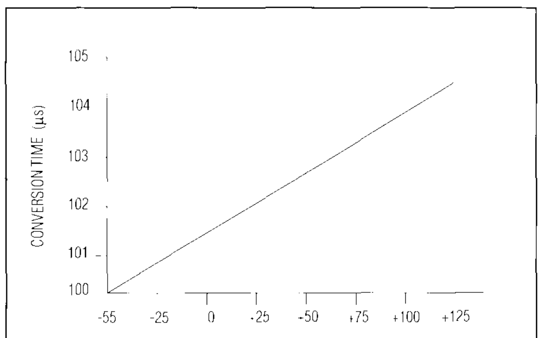

Figure 10. Typical Change in Conversion Time Variation vs. Temperature when Using Internal Clock

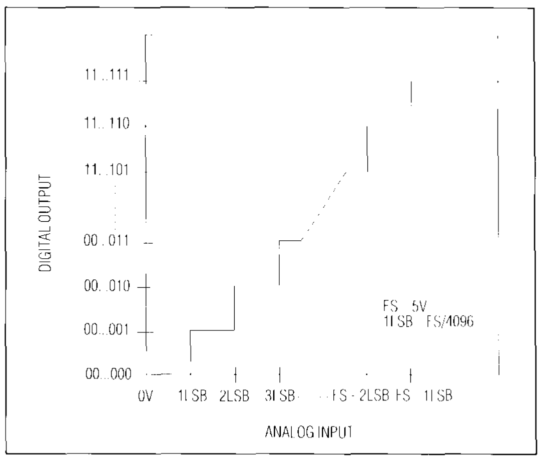

Figure 12. Ideal Input/Output Transfer Characteristic for Unipolar Circuit of Figure 11

Internal Reference

The internal reference (REFOUT) should be bypassed with a 1Ω resistor in series with a capacitor. The capacitor should be a 10μF electrolytic or tantalum in parallel with a 0.01μF disc ceramic (Figure 16). Figure 17 shows a circuit that allows input adjustment which is useful for trimming out initial (room temperature) error in the reference voltage.

Table 1. Transition Points for Unipolar 0V to +5V Operation

Analog Input (V)	Digital Output
0.00122	0000 0000 0001
0.00244	0000 0000 0010
. . .	. . .
2.49878	0111 1111 1111
2.50000	1000 0000 0000
2.50122	1000 0000 0001
. . .	. . .
4.99756	1111 1111 1110
4.99878	1111 1111 1111

Table 2. Transition Points for Bipolar -5V to +5V Operation

Analog Input (V)	Digital Output
-4.99878	0000 0000 0001
-4.99634	0000 0000 0010
. . .	. . .
-0.00122	1000 0000 0000
+0.00122	1000 0000 0001
. . .	. . .
+4.99389	1111 1111 1110
+4.99634	1111 1111 1111

External Reference Circuit

Figure 18 shows how to set up a MX584LH to generate a reference voltage of 5.00V. A typical adjustment range of 75mV is provided by R2. Over the commercial temperature range, the MX584LH contributes no more than ±1LSB of gain error.

During a conversion, transient currents flow at the REFIN input. To prevent dynamic errors, place either a 10μF electrolytic or tantalum smoothing capacitor in parallel with a 0.01μF disc ceramic from the REFIN pin to AGND.

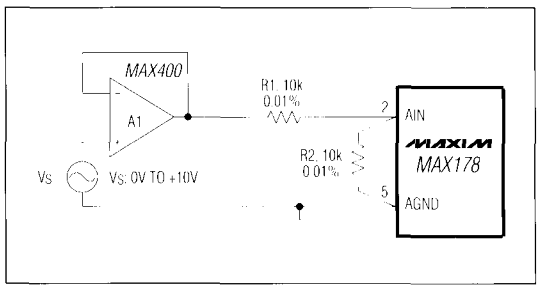

Figure 13. Unipolar 0V to +10V Operation

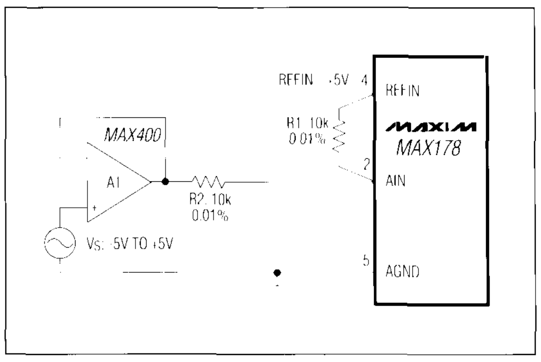

Figure 14. Bipolar -5V to +5V Operation

Layout

When designing layout for a printed circuit board, keep digital and analog signal lines separated whenever possible. It is critical that no digital line runs alongside an analog signal line or near the CAZ. Guard the analog inputs, the reference input and the CAZ input with AGND.

Establish a single-point analog ground (AGND) as close to the MAX178 as possible, isolated from the logic system. Connect the single-point analog ground to the digital system ground, which is attached to DGND at one point, as close as possible to the MAX178. The following should be returned to the analog ground point: input-signal common, input guards, the CAZ, and any bypass capacitors for the reference input and the analog supplies. Low-impedance analog and digital power-supply common returns, with wide trace widths, are essential for quiet operation of the MAX178.

Noise

To minimize input noise coupling, input signal leads to AIN and signal return leads from AGND should be kept as short as possible. A shielded cable between source and ADC is suggested in applications where longer leads are required. Also, care should be taken to reduce ground circuit impedances as much as possible since any potential difference in grounds between the signal source and ADC creates an error voltage in series with the input signal.

When interfacing to continuously busy and noisy µP buses, it is possible to get errors at the LSB level. These errors exist because of feedthrough from the bus to the integrated circuit through the package. The problem can be minimized in ceramic packaged chips by grounding the metal lid. Another solution is to isolate the MAX178 from the noisy µP bus using three-state buffers.

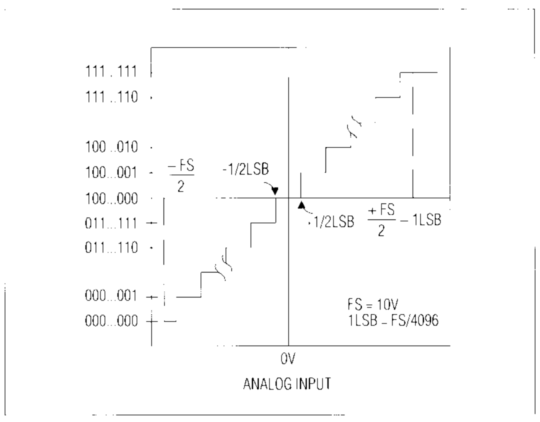

Figure 15. Ideal Input/Output Transfer Characteristic for Bipolar Circuit of Figure 14

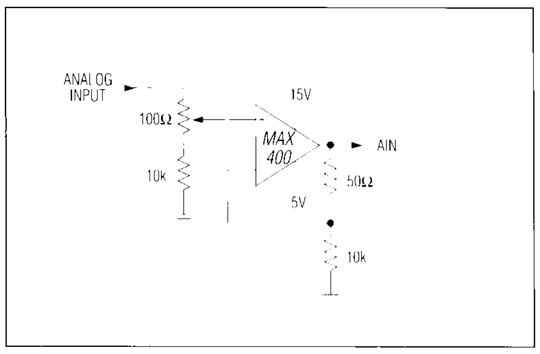

Figure 17. Adjusting Analog Input Gain to Trim Out Initial Reference Voltage Error

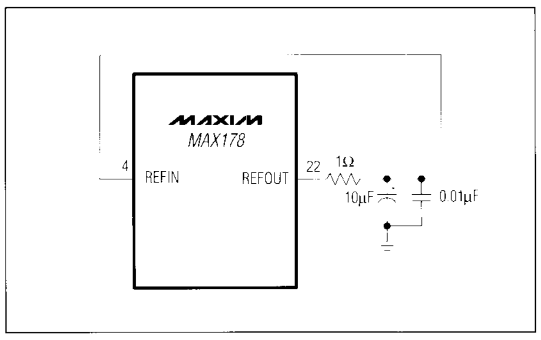

Figure 16. Internal Reference Hookup.
Note: Reference Value Is Not Adjustable.

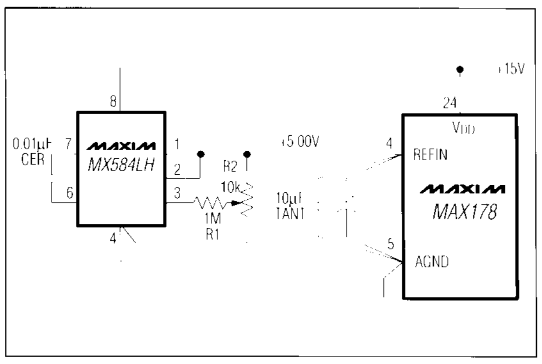

Figure 18. MX584LH as Reference Generator

Chip Topography