MAX14640–MAX14644/MAX14651

USB Host Adapter Emulators

General Description

The MAX14640–MAX14644/MAX14651 are next-generation USB 2.0 host charger adapter emulators that combine USB Hi-Speed analog switches with a USB adapter emulator circuit.

The MAX14640/MAX14651 feature an I²C interface to fully configure the charging behavior with different address options. The MAX14641–MAX14644 are controlled by two GPIO inputs (CB1/CB0) and support USB data and automatic charger mode. In charging downstream port (CDP) pass-through mode, the devices emulate the CDP function while supporting normal USB traffic. The MAX14641/MAX14642/MAX14643 have a CEN output for an active-high CLS enable input, and the MAX14644 has a $\overline{CEN}$ output for an active-low CLS enable input to restart the peripheral connected to the USB host.

The MAX14640–MAX14644/MAX14651 feature 2A high-current autodetect mode. The MAX14641 features 1A high-current forced mode instead of regular DCP mode. The MAX14640/MAX14651 can be configured through I²C to support various dedicated charger modes such as DCP, Apple® 1A/2A forced, or Apple 1A/2A automatic mode.

All the devices support CDP and standard downstream port (SDP) charging while in the active state (S0) and support the dedicated charging port (DCP) charging while in the standby state (S3/S4/S5). All devices support low-speed remote wake-up by monitoring DM, and the MAX14642 also supports remote wake-up in sleep mode (S3).

The MAX14640–MAX14644/MAX14651 are available in an 8-pin (2mm x 2mm) TDFN-EP package and are specified over the -40°C to +85°C extended temperature range.

***Ordering Information* and *Typical Operating Circuit* appear at end of data sheet.**

Benefits and Features

- **Improved Charger Interoperability**
  - **USB (CDP) Emulation**
    - **Smart CDP**
    - **Foolproof CDP**
  - **Meets New USB Battery Charging (BC) Revision 1.2 Specification**
  - **Backward Compatible with Previous USB BC Revisions**
  - **Meets China YD/T1591-2009 Charging Specification**
  - **Supports Standby-Mode Charging for Apple BC Revision 1.2 Compatible Devices**
- **Provide Greater Application Flexibility**
  - **I²C Controls Multiple Modes (MAX14640/MAX14651)**
  - **CB0 and CB1 Pins Control Multiple Automatic and Manual Charger States**
- **Enhance Performance with High Level of Integrated Features**
  - **Supports Remote Wake-Up**
  - **Low-Capacitance USB 2.0 Hi-Speed Switch to Change Charging Modes**
  - **Automatic Current-Limit Switch Control**
  - **±15kV ESD Protection on DP/DM**
- **Minimize PCB Area**
  - **2mm x 2mm, 8-Pin TDFN Package**

Applications

Laptop/Desktop Computers

USB Hubs

Universal Chargers Including iPod®/iPhone®/iPad®

Selector Guide

PART NUMBER	I/O MODE	CEN POLARITY	REMOTE WAKE-UP IN AM	FORCED CHARGER MODE	BIAS IN FM
MAX14640	I²C (0x35)	N/A	Optional	Yes	DP/DM short
MAX14641	GPIO	CEN	No	No	Apple 1A
MAX14642	GPIO	CEN	Yes	Yes	DP/DM short
MAX14643	GPIO	CEN	No	Yes	DP/DM short
MAX14644	GPIO	$\overline{CEN}$	No	Yes	DP/DM short
MAX14651	I²C (0x15)	N/A	Optional	Yes	DP/DM short

*For related parts and recommended products to use with this part, refer to: **www.maximintegrated.com/MAX14640.related**.*

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim Integrated's website at www.maximintegrated.com.

19-6472; Rev 1; 4/13

ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND.)
V_{CC}, TDP, TDM, DP, DM, SDA, SCL,
CB0, CB1, CEN, $\overline{CEN}$, $\overline{INT}$.....-0.3V to +6V
Continuous Current into Any Terminal ..... ±30mA
Continuous Power Dissipation (T_A = +70°C)
TDFN (derate 11.9mW/°C above +70°C).....953.5mW

Operating Temperature Range ..... -40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL CHARACTERISTICS (Note 1)

TDFN
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....83.9°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) .....37°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 3.0V to 5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = 5.0V and T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER SUPPLY							
V_{CC} Supply Voltage	V_{CC}	CB0 = high		3.0		5.5	V
		CB0 = low (Note 3)		4.75		5.25	
V_{CC} Supply Current	I_{CC}	MAX14641–MAX14644	CB1 = CB0 = low (AM2 mode)			200	µA
			CB1 = CB0 = high (CM mode)			100	
			CB1 = low, CB0 = high (PM mode)			20	
		MAX14640/MAX14651	MODE_SEL[2:0] = 000 (AM2 mode)			200	
			MODE_SEL[2:0] = 011 (CM mode)			100	
			MODE_SEL[2:0] = 001 (PM mode)			20	
POR Delay	t_{POR}				50		ms
ANALOG SWITCHES (DP, DM, TDP, TDM)							
Analog Signal Range	V_{DP}, V_{DM}	(Note 4)		0		V_{CC}	V
TDP/TDM On Resistance	R_{ON}	V_{IN} = 0V to V_{CC}, I_{IN} = 10mA			3.5	6.5	Ω
TDP/TDM On-Resistance Matching Between Channels	ΔR_{ON}	V_{CC} = 5.0V, I_{IN} = 10mA, V_{IN} = 0.4V			0.1		Ω
TDP/TDM On-Resistance Flatness	R_{FLAT}	V_{CC} = 5.0V, I_{IN} = 10mA, V_{IN} = 0V to V_{CC}			0.1		Ω
DP/DM Short On-Resistance	R_{SHORT}	V_{DP} = 1V, R_L = 20kΩ on DM			70	128	Ω

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 3.0V to 5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = 5.0V and T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Off Leakage Current	$I_{COM(OFF)}$	V_{CC} = 3.6V, V_{DP} = V_{DM} = 0.3V to 3.3V, V_{TDP} = V_{TDM} = 3.3V to 0.3V	-1	1.5nA	+1	µA
On Leakage Current	$I_{COM(ON)}$	V_{CC} = 3.6V, V_{DP} = V_{DM} = 0.3V to 3.3V	-1	90nA	+1	µA
DYNAMIC PERFORMANCE						
Turn-On Time	t_{ON}	V_{TDP} or V_{TDM} = 1.5V, R_L = 300Ω, C_L = 35pF, Figure 1 (Note 4)		20		µs
Turn-Off Time	t_{OFF}	V_{TDP} or V_{TDM} = 1.5V, R_L = 300Ω, C_L = 35pF, Figure 1 (Note 4)		1		µs
TDP/TDM Propagation Delay	t_{PHL}, t_{PLH}	R_L = R_S = 50Ω, DP and DM connected to TDP and TDM, Figure 2		60		ps
DP/DM Output Skew	t_{SKEW}	R_L = R_S = 50Ω, DP and DM connected to TDP and TDM, Figure 2		40		ps
DP/DM On-Capacitance (Connected to TDP, TDM)	C_{OFF}	f = 240MHz, V_{BIAS} = 0V, V_{IN} = 500mV_{P-P}		5		pF
Bandwidth	BW	R_L = R_S = 50Ω, Figure 3		1000		MHz
Off-Isolation	V_{ISO}	V_{IN} = 0dBm, R_L = R_S = 50Ω, f = 250MHz, Figure 3		-20		dB
Crosstalk	V_{CT}	V_{IN} = 0dBm, R_L = R_S = 50Ω, f = 250MHz, Figure 3		-25		dB
DCP INTERNAL RESISTORS						
DP/DM Short Pulldown	R_{PD}		320	500	700	kΩ
RP1/RP2 Ratio	RT_{RP}		1.485	1.5	1.515	
RP1 + RP2 Resistance	R_{RP}		92	125	158.5	kΩ
RM1/RM2 Ratio	RT_{RM}		0.844	0.85	0.864	
RM1 + RM2 Resistance	R_{RM}		68	93	118	kΩ
RSS1/RSS2 Ratio	RT_{RSS}		2.9	3	3.1	
RSS1 + RSS2 Resistance	R_{RSS}		30	40	60	kΩ
CDP INTERNAL RESISTORS						
DP Pulldown Resistor	R_{DP_CDP}	CDP mode	14.25	19.53	24.80	kΩ
DM Pulldown Resistor	R_{DM_CDP}	CDP mode	14.25	19.53	24.8	kΩ
CDP HIGH-SPEED COMPARATORS						
Threshold Voltage	V_{TH_CDP}		100	161	205	mV
CDP LOW-SPEED COMPARATORS						
V_{DM_SRC} Voltage	V_{DM_SRC}	I_{LOAD} = 0 to 200µA	0.5		0.7	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 3.0V to 5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = 5.0V and T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
V_{DP_REF} Voltage	V_{DP_REF}			0.25		0.4	V
V_{LGC} Voltage	V_{LGC}			0.8		2.0	V
I_{DP_SINK} Current	I_{DP_SINK}	V_{DP} = 0.15V to 3.6V		50		150	µA
LOGIC INPUTS (CB0, CB1, SDA, SCL)							
Input Logic High Voltage	V_{IH}			1.4			V
Input Logic Low Voltage	V_{IL}					0.4	V
Input Leakage Current	I_{IN}	$0V \le V_{IN} \le V_{IL}$ or $V_{IH} \le V_{IN} \le V_{CC}$, V_{CC} = 5.5V		-1		+1	µA
CB0/CB1 Debounce Time	$t_{DEB\_CB\_}$				250		µs
OPEN-DRAIN LOGIC OUTPUTS (SDA, $\overline{INT}$, $\overline{CEN}$, CEN)							
$\overline{INT}$, SDA, CEN Output Low Voltage	V_{OL}	Output asserted, I_{SINK} = 4mA				0.4	V
$\overline{INT}$, SDA, CEN Output Leakage Current	I_{OH}	Output not asserted, $V_{CC} = V_{OUT}$ = 5.5V				1	µA
CEN, $\overline{INT}$, Output High Voltage	V_{OH}	Output asserted, I_{SOURCE} = 4mA		V_{CC} - 0.4			V
CEN, $\overline{INT}$, Output Leakage Current	I_{OL}	Output not asserted, V_{CC} = 5.5V, $V_{\overline{CEN}}$ = 0V				1	µA
V_{BUS} Toggle Time Accuracy	t_{VBT}				±10		%
I²C TIMING CHARACTERISTICS (SEE FIGURE 4)							
I²C Maximum Clock Frequency	f_{SCL}					400	kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}			1.3			µs
START Condition Setup Time	$t_{SU:STA}$			0.6			µs
Repeated START Condition Setup Time	$t_{SU:STA}$	70% of SCL to 70% of SDA		0.6			µs
START Condition Hold Time	$t_{HD:STA}$	30% of SDA to 70% of SCL		0.6			µs
STOP Condition Setup Time	$t_{SU:STO}$	70% of SCL to 30% of SDA		0.6			µs
Clock Low Period	t_{LOW}	30% to 30%		1.3			µs
Clock High Period	t_{HIGH}	70% to 70%		0.6			µs
Data Valid to SCL Rise Time	$t_{SU:DAT}$	Write setup time		100			ns
Data Hold Time to SCL Fall	$t_{HD:DAT}$	Write hold time			100		ns
PROTECTION SPECIFICATIONS							
ESD Protection	V_{ESD}	Human Body Model	DP and DM pins		±15		kV
			All other pins		±2		

Note 2: All units are production tested at T_A = +25°C. Specifications over temperature are guaranteed by design.

Note 3: The MAX1464_ is operational from 3.0V to 5.5V. However, in order for the valid Apple resistor-divider network to function, V_{CC} must stay within the 4.75V to 5.25V range.

Note 4: Guaranteed by design, not production tested.

Note 5: Guaranteed by design.

Test Circuits/Timing Diagrams

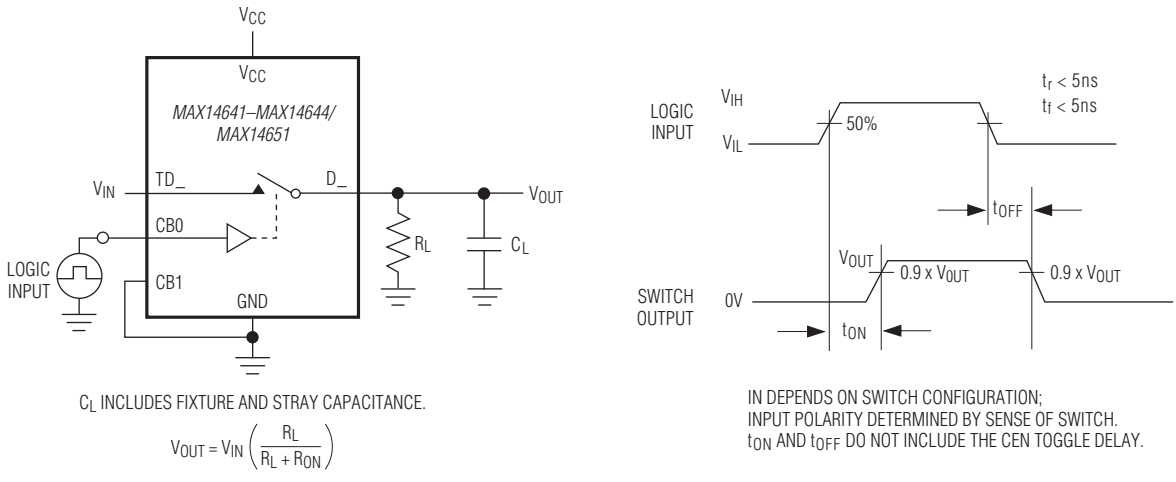


Figure 1. Switching Time

Test Circuits/Timing Diagrams (continued)

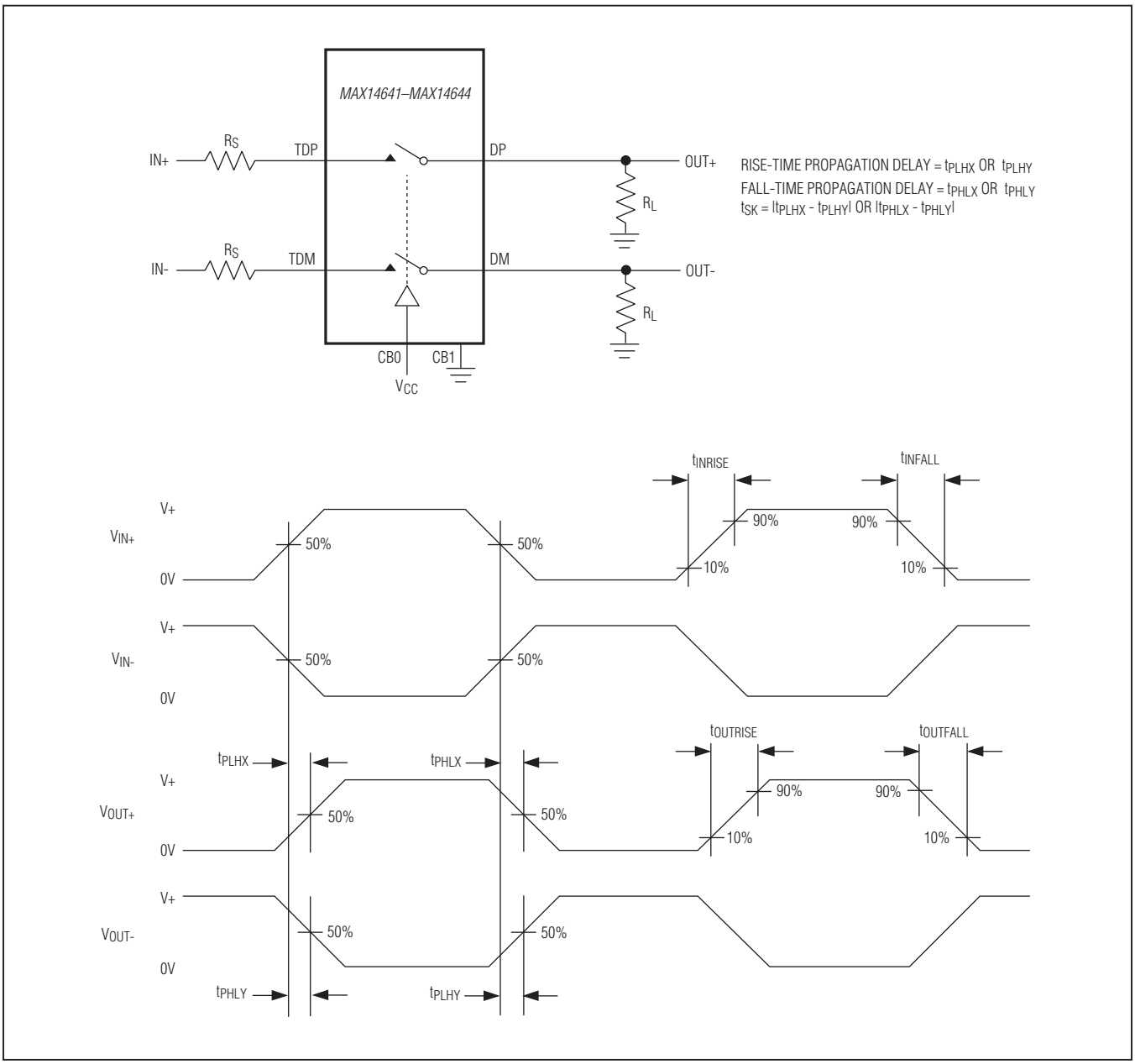


Figure 2. Propagation Delay and Output Skew

Test Circuits/Timing Diagrams (continued)

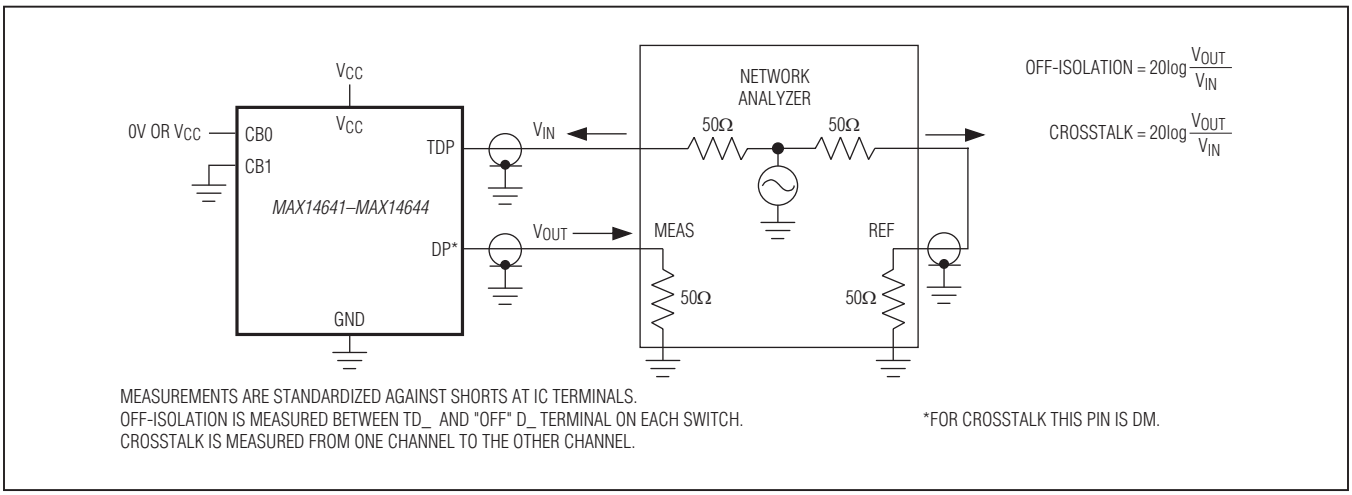


Figure 3. Bandwidth, Off-Isolation, and Crosstalk

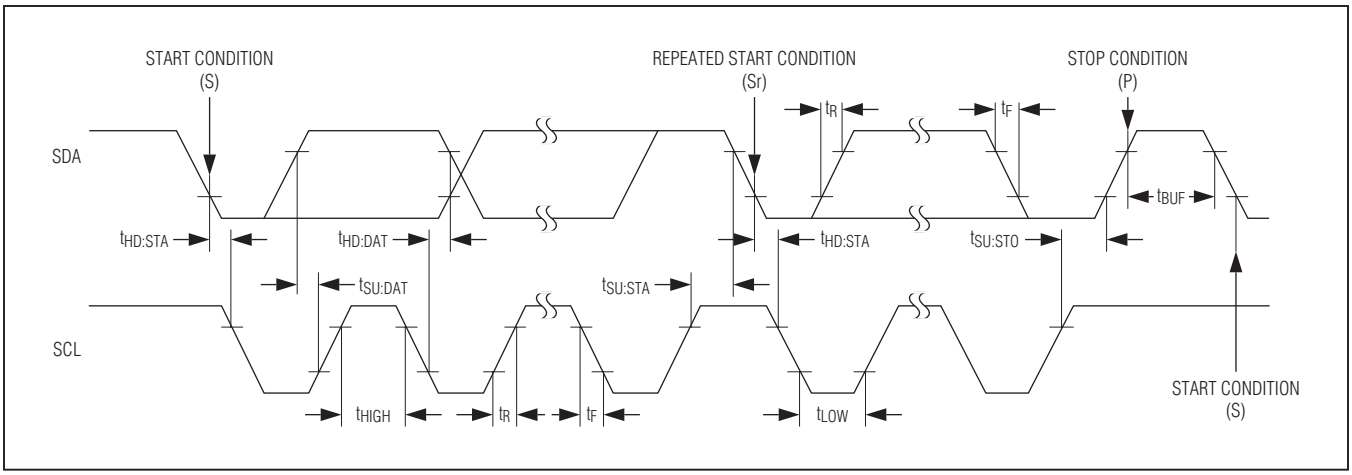
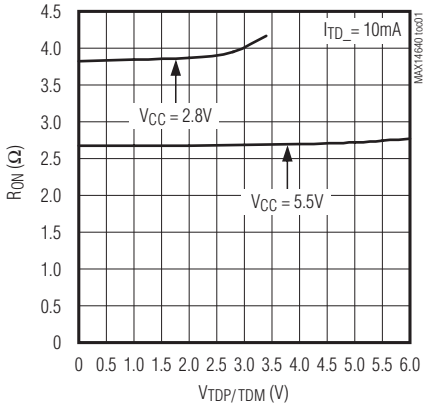


Figure 4. I^2C Timing Diagram. Note that t_R and t_F are per the I^2C fast-mode specification.

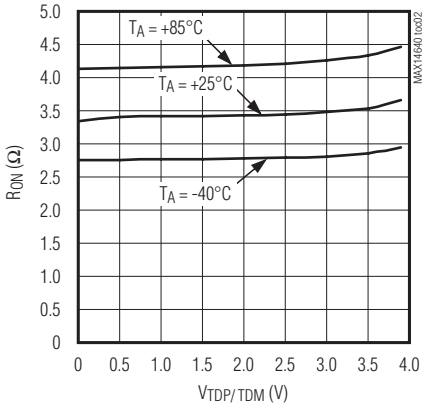
Typical Operating Characteristics

(V_{CC} = +5V, T_A = +25°C, unless otherwise noted.)

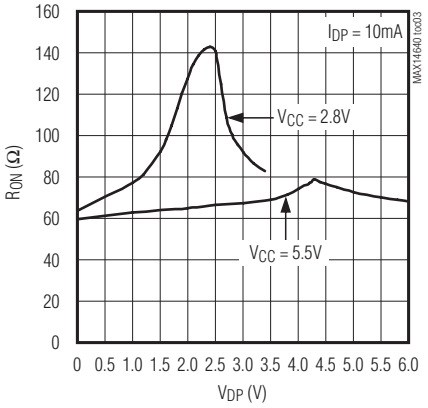
USB SWITCH ON-RESISTANCE vs. SIGNAL VOLTAGE



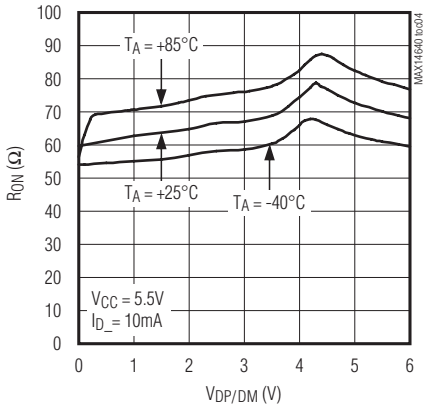
USB SWITCH ON-RESISTANCE vs. SIGNAL VOLTAGE



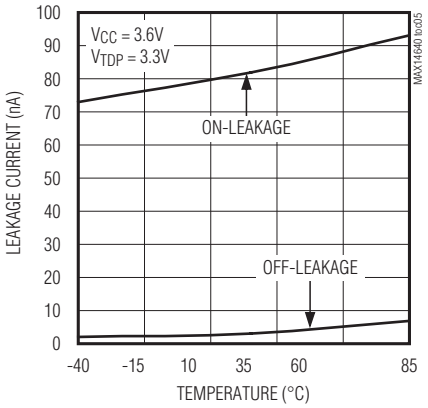
DP/DM SHORT ON-RESISTANCE vs. SIGNAL VOLTAGE



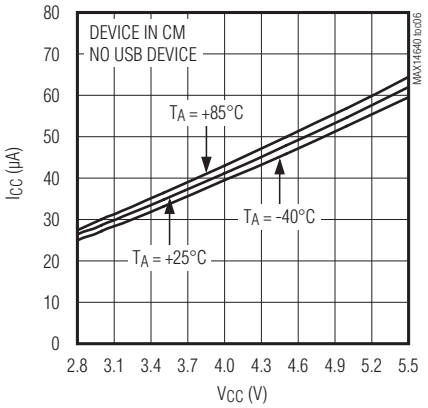
DP/DM SHORT ON-RESISTANCE vs. SIGNAL VOLTAGE



TDP/DP LEAKAGE CURRENT vs. TEMPERATURE



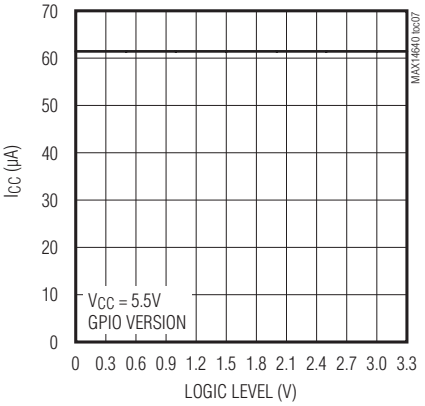
SUPPLY CURRENT vs. SUPPLY VOLTAGE



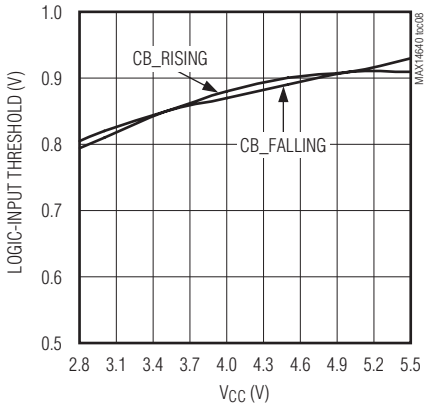
Typical Operating Characteristics (continued)

(V_{CC} = +5V, T_A = +25°C, unless otherwise noted.)

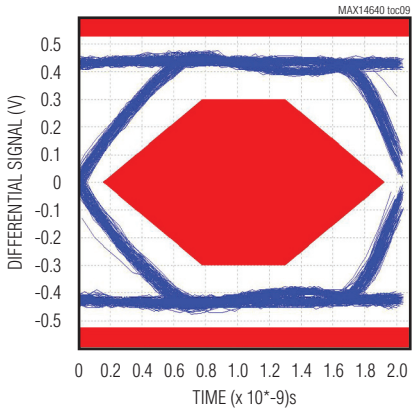
SUPPLY CURRENT vs. LOGIC LEVEL



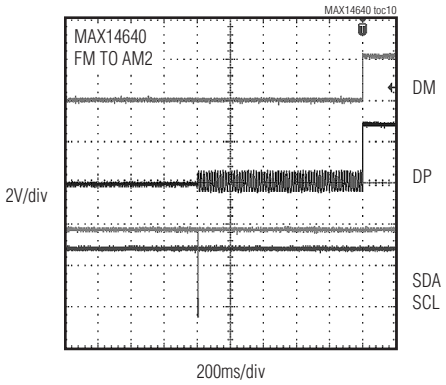
LOGIC-INPUT THRESHOLD vs. SUPPLY VOLTAGE



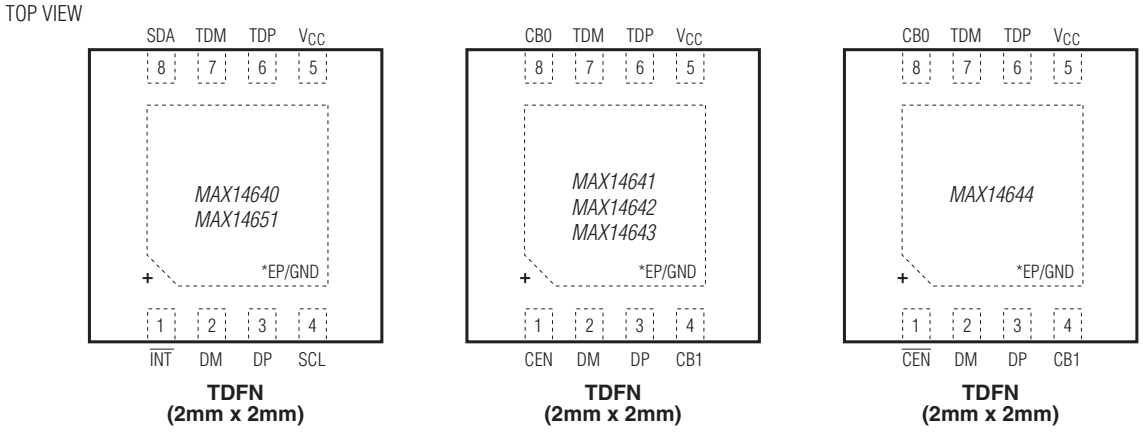
EYE DIAGRAM



AUTO DETECTION MODE



Pin Configurations

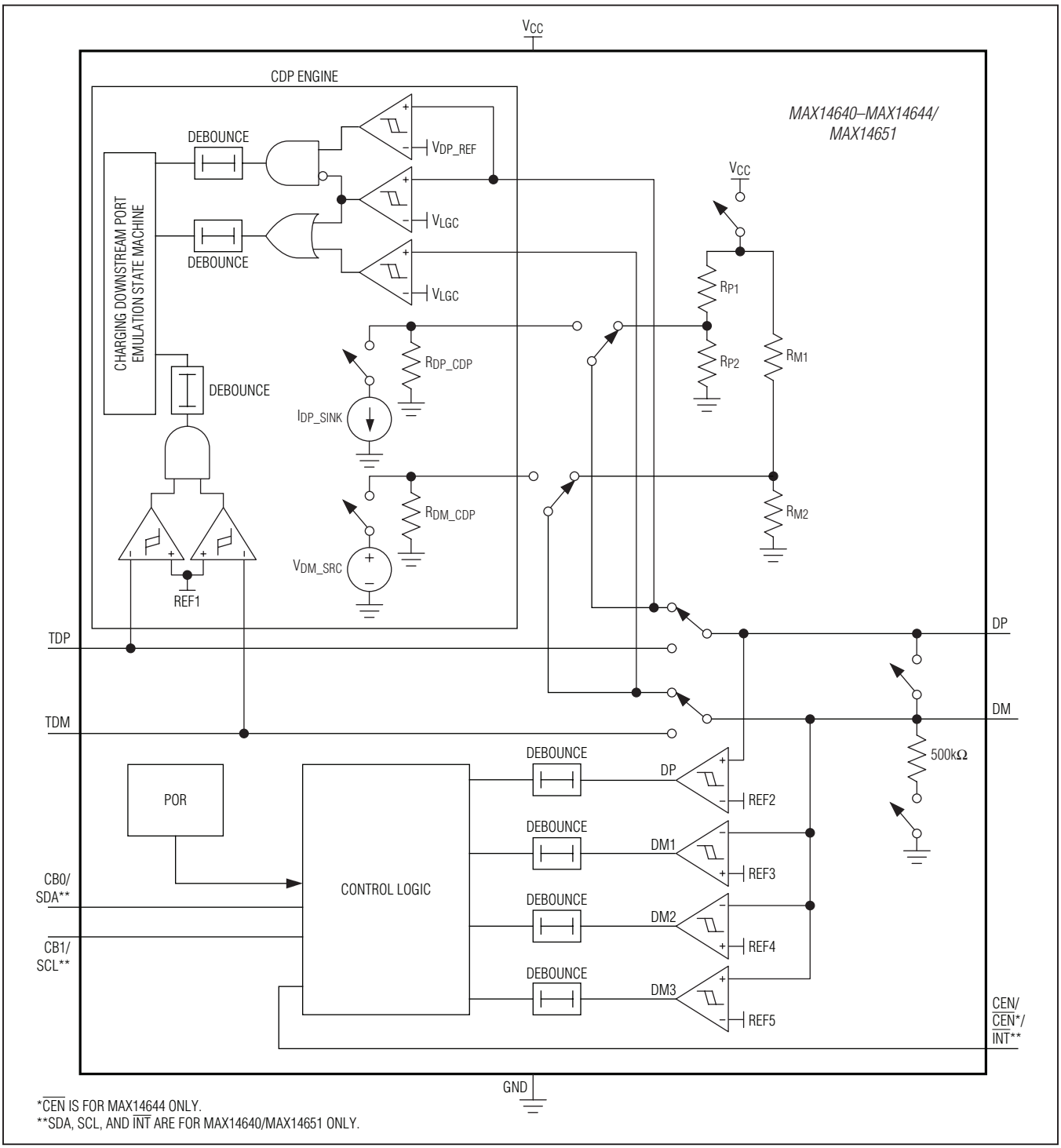


*CONNECT THE EXPOSED PAD (EP/GND) TO THE GROUND PLANE.

Pin Description

PIN			NAME	FUNCTION
MAX14640/ MAX14651	MAX14641/ MAX14642/ MAX14643	MAX14644		
1	—	—	$\overline{INT}$	Open-Drain Interrupt Output. $\overline{INT}$ asserts low when interrupt occurs.
—	1	—	CEN	nMOS Open-Drain Output. Pull up CEN to V_{CC} by 10kΩ. CEN high enables the current-limit switch and V_{BUS} ON, and nMOS ON makes CEN low and the current-limit switch OFF. When CB_ transitions from low to high or high to low, CEN is low for 1s (typ).
—	—	1	$\overline{CEN}$	pMOS Open-Drain Output. Pull down $\overline{CEN}$ to GND by 10kΩ. $\overline{CEN}$ low enables the current-limit switch and V_{BUS} ON, and pMOS ON makes $\overline{CEN}$ high and the current-limit switch OFF. When CB_ transitions from low to high or high to low, $\overline{CEN}$ is high for 1s (typ).
2	2	2	DM	USB Connector D- Connection
3	3	3	DP	USB Connector D+ Connection
4	—	—	SCL	I^2C Serial-Clock Input
—	4	4	CB1	Switch Control Input Bit 1. See the Switch Control Input Truth tables (Tables 2, 3, and 4).
5	5	5	V_{CC}	Power-Supply Input. Bypass V_{CC} to GND with a 0.1µF ceramic capacitor as close as possible to the device.
6	6	6	TDP	Host USB Transceiver D+ Connection
7	7	7	TDM	Host USB Transceiver D- Connection
8	—	—	SDA	I^2C Serial-Data Input/Output
—	8	8	CB0	Switch Control Input Bit 0. See the Switch Control Input Truth tables (Tables 2, 3, and 4).
—	—	—	EP/ GND	Exposed Pad and Ground. The exposed pad is the ground connection for the device. Connect EP/GND to the ground plane.

Functional Diagram



Detailed Description

The MAX14640–MAX14644/MAX14651 adapter emulator devices have high-speed USB analog switches that support USB hosts by identifying the USB port as a charger when the USB host is in a low-power mode and cannot enumerate USB devices. The devices feature low 4pF (typ) on-capacitance and low 4Ω (typ) on-resistance when the USB switches are connected. DP and DM are capable of handling signals between 0V and 5.5V over the entire 3.0V–5.5V supply range.

The MAX14640/MAX14651 are controlled by an I²C interface while the MAX14641–MAX14644 are controlled by the CB0 and CB1 logic inputs. The I²C interface allows further customization over which mode the MAX14640/MAX14651 operate in and can be used to read back connection information.

Improvements over the MAX14600 USB detector family include support for some smartphones that do not connect after applying 0.6V in charging downstream port (CDP) mode. The devices also support high-current charging of Apple devices while in sleep mode.

Resistor-Dividers

The MAX14640–MAX14644/MAX14651 feature internal resistor-divider networks on the data lines to provide support for Apple devices. The resistor-divider is disconnected while not in use to minimize the supply current. The resistor-dividers are not connected in pass-through mode. Table 1 summarizes the resistor values connected to DP/DM in different charging modes.

Switch Control

Digital Controls

The MAX14641–MAX14644 feature two digital select inputs, CB0 and CB1, for mode selection. Table 2, Table 3, and Table 4 show how the CB1/CB0 inputs can be used to enter autodetection charger mode (AM_), pass-through mode (PM), forced charger mode (FM and AP_), and pass-through mode with CDP emulation (CM).

In CDP emulation mode, the peripheral device with CDP detection capability draws charging current up to 1.5A immediately without USB enumeration.

Table 1. DP/DM Resistor-Dividers

CHARGING MODE	DP PULLUP (kΩ)	DP PULLDOWN (kΩ)	DM PULLUP (kΩ)	DM PULLDOWN (kΩ)
AM1	75	49.9	43.2	49.9
AM2	43.2	49.9	75	49.9

Table 2. Digital Input State Table for the MAX14641

CB1	CB0	CHARGER/USB	MODE	STATUS
0	0	CHARGER	AM2	2A Autodetection Charger Mode for Apple Devices. Resistor-dividers are connected to DP/DM.
1	0	CHARGER	AP1	Forced 1A Charger Mode for Apple Devices. Resistor-dividers are connected to DP/DM.
0	1	USB	PM	USB Pass-Through Mode. DP/DM are connected to TDP/TDM.
1	1	USB	CM	USB Pass-Through Mode with CDP Emulation. Auto connects DP/DM to TDM/TDM depending on CDP detection status.

Table 3. Digital Input State Table for the MAX14642

CB1	CB0	CHARGER/USB	MODE	STATUS
X	0	CHARGER	AM2	2A Autodetection Charger Mode for Apple Devices. Resistor-dividers are connected to DP/DM.
0	1	USB	PM	USB Pass-Through Mode. DP/DM are connected to TDP/TDM.
1	1	USB	CM	USB Pass-Through Mode with CDP Emulation. Auto connects DP/DM to TDM/TDM depending on CDP detection status.

X = Don't care.

Table 4. Digital Input State Table for the MAX14643/MAX14644

CB1	CB0	CHARGER/USB	MODE	STATUS
0	0	CHARGER	AM2	2A Autodetection Charger Mode for Apple Devices. Resistor-dividers are connected to DP/DM.
1	0	CHARGER	FM	Forced Dedicated Charger Mode. DP and DM are shorted.
0	1	USB	PM	USB Pass-Through Mode. DP/DM are connected to TDP/TDM.
1	1	USB	CM	USB Pass-Through Mode with CDP Emulation. Auto connects DP/DM to TDM/TDM depending on CDP detection status.

Table 5. Digital Input State Table for the MAX14640/MAX14651

MODE_SEL			CHARGER/USB	MODE	STATUS
[2]	[1]	[0]			
0	0	0	CHARGER	AM2	2A Autodetection Charger Mode for Apple Devices. Resistor-dividers are connected to DP/DM.
0	0	1	USB	PM	USB Pass-Through Mode. DP/DM are connected to TDP/TDM.
0	1	0	CHARGER	FM	Forced Dedicated Charger Mode. DP and DM are shorted.
0	1	1	USB	CM	USB Pass-Through Mode with CDP Emulation. Auto connects DP/DM to TDM/TDM depending on CDP detection status.
1	0	0	CHARGER	AM1	1A Autodetection Charger Mode for Apple Devices. Resistor-dividers are connected to DP/DM.
1	0	1	CHARGER	AP1	Forced 1A Charger Mode for Apple Devices. Resistor-dividers are connected to DP/DM.
1	1	0	CHARGER	AP2	Forced 2A Charger Mode for Apple Devices. Resistor-dividers are connected to DP/DM.
1	1	1	CHARGER	SS	Forced 2A Charger Mode for Samsung Galaxy Tablet

I²C Controls

The MAX14640/MAX14651 mode is controlled by the MODE_SEL[2:0] bits. Table 5 shows how these bits control the device. In addition to being configurable in all modes that the MAX14641–MAX14644 can enter, the MAX14640/MAX14651 can be configured to be compatible with the Apple and Samsung® Galaxy (SS mode) devices.

Legacy D+/D- Detect

The MAX14640–MAX14644/MAX14651 support charging devices that use a D+/D- short to indicate it is ready for charging. This is done by monitoring the voltage at both the DP and DM terminals and triggering when they are both higher than their comparator thresholds.

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Auto Peripheral Reset

The MAX14641–MAX14644 feature an auto current-limit switch control output. This feature resets the peripheral connected to V_{BUS} in the event the USB host switches to or from standby mode. $\overline{CEN}$ or CEN are pulsed for 1s (typ) on the rising or falling edge of CB0 or CB1 (Figure 5 and Figure 6.).

Pass-Through Mode

If the MAX14640–MAX14644/MAX14651 are configured in pass-through mode (PM), then TDP/TDM are always connected to DP/DM and no resistor-dividers or power sources are applied to DP/DM.

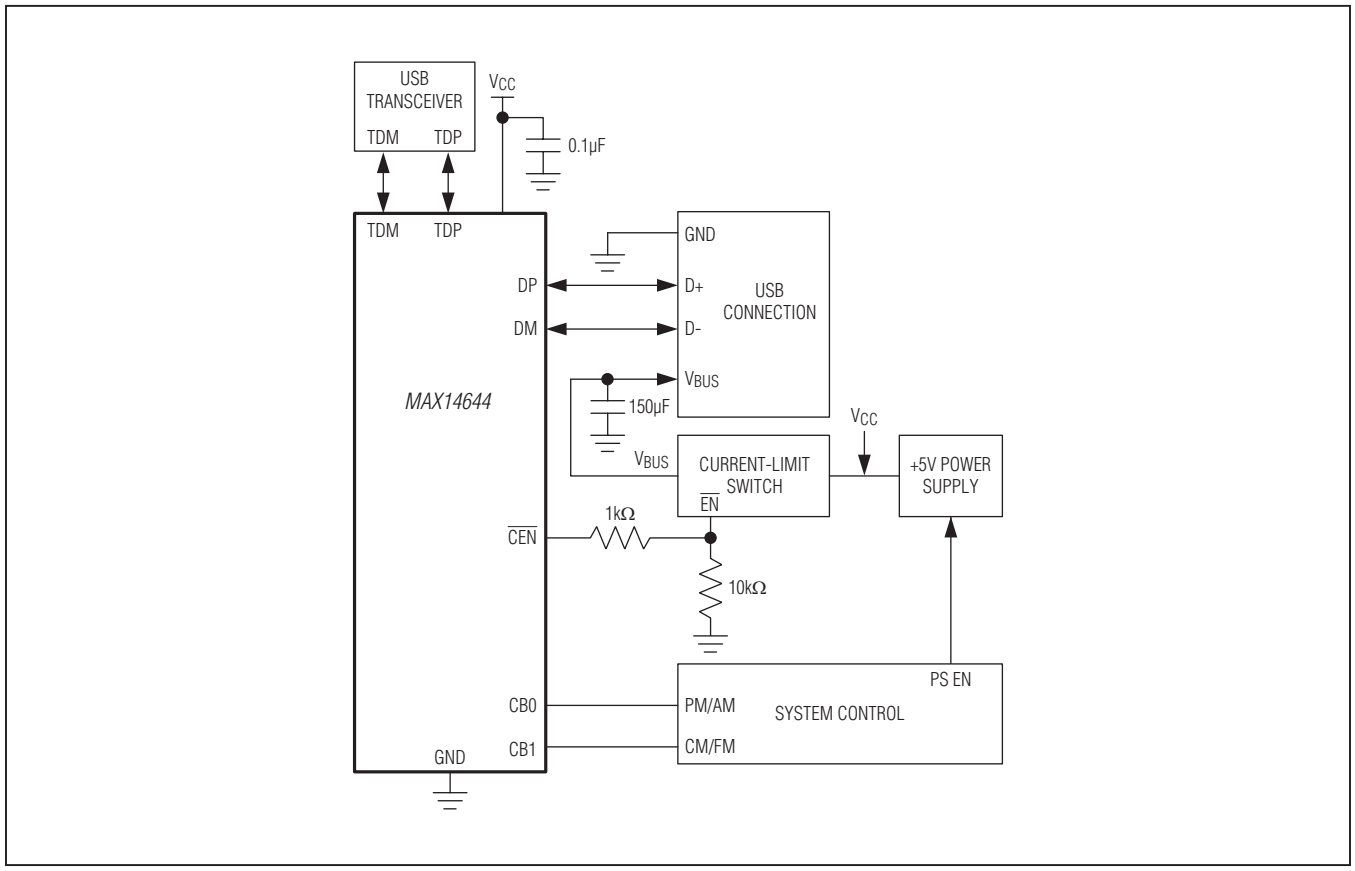


Figure 5. MAX14644 Peripheral Reset Applications Diagram

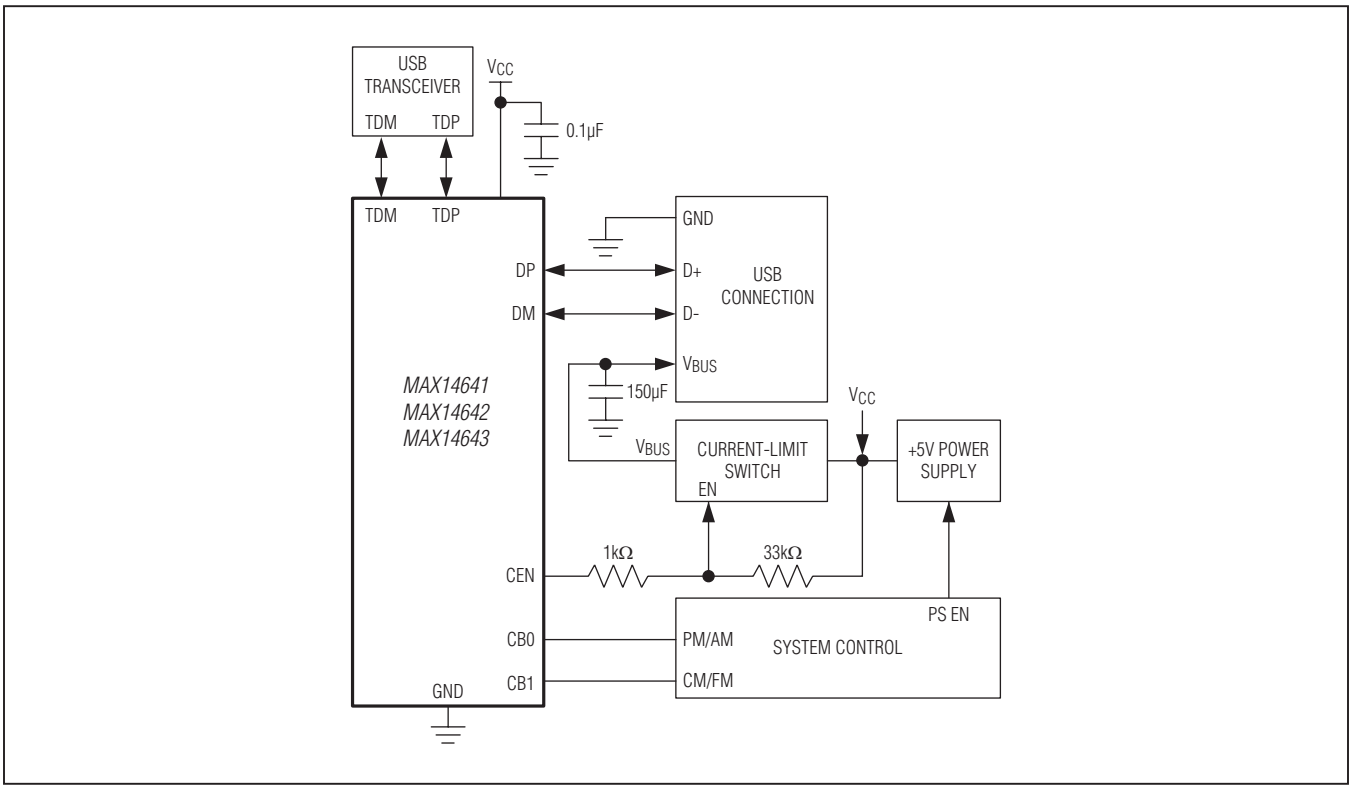


Figure 6. MAX14641/MAX14642/MAX14643 Peripheral Reset Applications

Table 6. Forced Charging Modes

CHARGING MODE	DP PULLUP (kΩ)	DP PULLDOWN (kΩ)	DM PULLUP (kΩ)	DM PULLDOWN (kΩ)
FM	N/A	N/A	N/A	N/A
SS	30	10	30	10
AP1	75	49.9	43.2	49.9
AP2	43.2	49.9	75	49.9

Forced Charger Modes

The MAX14640–MAX14644/MAX14651 can be configured in different forced dedicated charging port (DCP) modes; V_{BUS} is enabled and DP and DM are either shorted (FM) or connected to resistor-dividers (all other modes). Table 6 summarizes the resistor-divider values in each forced mode.

Automatic Detection with Remote Wake-Up Support

The MAX14640–MAX14644/MAX14651 feature automatic detection charger mode (AM1/AM2) for dedicated chargers and USB masters. In automatic detection charger mode, the device monitors the voltages on DM and DP with resistor-dividers connected to determine the type of device attached.

If a USB-compliant device is connected, DP and DM are shorted together to commence charging. Once the charging device is removed, the short between DP and DM is disconnected and the resistor-divider is applied. A pulldown resistor on the shorted DP/DM node ensures that a disconnect is detected.

USB Pass-Through Mode with CDP Emulation

The MAX14640–MAX14644/MAX14651 feature a pass-through mode with CDP emulation (CM). This is to support the higher charging current capability during the pass-through mode in normal USB operation (S0 state). The peripheral device equipped with CDP detection capability can draw a charging current as defined in USB battery charger specification 1.2 when the charging host supports the CDP mode. This is a useful feature since most host USB transceivers do not have the CDP function. Table 7 summarizes the USB host power states.

Table 7. USB Host Power States

STATE	DESCRIPTION
S0	System On
S1	Power to the CPU(s) and RAM is Maintained. Devices that do not indicate that they must remain on, may be powered down.
S2	CPU is Powered Off
S3	Standby (Suspend to Ram)—System Memory Context is Maintained. All other system context is lost.
S4	Hibernate—Platform Context is Maintained
S5	Soft Off

Register Map/Register Descriptions

REGISTER	ADDR	TYPE	POR	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
DeviceID	0x00	R	0x10*	CHIPID[3:0]				CHIPREV[3:0]			
Control1	0x01	R/W	0x87	FUO	FUO	FUO	FUO	FUO	FUO	FUO	FUO
Control2	0x02	R/W	0x50	LOW_PWR	FUO	FUO	FUO	FUO	FUO	DIS_CDP	FUO
Control3	0x03	R/W	0xE9	CEN_CNT[1:0]		CEN_DEL[2:0]			MODE_SEL[2:0]		
Control4	0x04	R/W	0x00	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
Control5	0x05	R/W	0x7B	INT_EN	USB_SW[1:0]		CEN_OUT	CEN_POL	FUO	RWU_DFT	RWU_LS
INT	0x06	R	0x00	CDP_DEVi	BYPASS_CDPi	CDP_CNi	RFU	USB_XFRi	RWUi	CEN_TOG_STi	CEN_TOG_SPi
STATUS	0x07	R	0x00	CDP_DEVs	BYPASS_CDPs	CDP_CNs	RFU	USB_XFRs	RWUs	RFU	CEN_TOG_SPs
MASK	0x08	R/W	0x00	CDP_DEVm	BYPASS_CDPm	CDP_CNm	RFU	USB_XFRm	RWUm	CEN_TOG_STm	CEN_TOG_SPm

FUO = Factory Use Only. Do not change from POR values.

RFU = Reserved for Future Use. Do not change from POR values.

**Applies to the MAX14640; the MAX14651 POR is 0x20.*

DeviceID Register

ADDRESS:	0x00							
MODE:	Read Only							
BIT	7	6	5	4	3	2	1	0
NAME	CHIPID[3:0]				CHIPREV[3:0]			
RESET	0	0	0	1	0	0	0	0
CHIPID[3:0]	The CHIPID[3:0] bits show information about the version of the MAX14640/MAX14651.							
CHIPREV[3:0]	The CHIPREV[3:0] bits show information about the revision of the MAX14640/MAX14651 silicon.							

Control1 Register

ADDRESS:	0x01							
MODE:	Read/Write							
BIT	7	6	5	4	3	2	1	0
NAME	FUO	FUO	FUO	FUO	FUO	FUO	FUO	FUO
RESET	1	0	0	0	0	1	1	1
FUO	Factory Use Only. Do not modify from reset values.							

Control2 Register

ADDRESS:	0x02							
MODE:	Read/Write							
BIT	7	6	5	4	3	2	1	0
NAME	LOW_PWR	FUO	FUO	FUO	FUO	FUO	DIS_CDP	FUO
RESET	0	1	0	1	0	0	0	0
LOW_PWR	Low-Power Mode. 0 = MAX14640/MAX14651 is in normal operation. 1 = MAX14640/MAX14651 is in low-power mode. All circuitry other than the I^2C interface is disabled.							
DIS_CDP	Disable CDP Signal. 0 = CDP signaling enabled 1 = CDP signaling disabled							
FUO	Factory Use Only. Do not modify from reset values.							

Control3 Register

ADDRESS:	0x03							
MODE:	Read/Write							
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME	CEN_CNT[1:0]		CEN_DEL[2:0]			MODE_SEL[2:0]		
RESET	1	1	1	0	1	0	0	1
CEN_CNT[1:0]	CEN State Control. Directly controls the CEN output independent of automatic cycling. 00 = CEN deasserted and CEN cycling disabled 01 = CEN cycling disabled between CB_ transitions during CDP modes and in AM mode 10 = CEN asserted 11 = CEN controlled by CDP/DCP/AM modes							
CEN_DEL[2:0]	CEN Pulse Delay. Controls how long V_{BUS} toggles last outside of AM mode. 000 = 125ms 001 = 250ms 010 = 350ms 011 = 500ms 100 = 750ms 101 = 1.0s 110 = 1.5s 111 = 2s							
MODE_SEL[2:0]	Operating Mode Control. 000 = AM2 001 = PM 010 = FM 011 = CM 100 = AM1 101 = AP1 110 = AP2 111 = SS							

Control4 Register

ADDRESS:	0x04							
MODE:	Read/Write							
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
RESET	0	0	0	0	0	0	0	0
RFU	Reserved for Future Use							

Control5 Register

ADDRESS:	**0x05**							
MODE:	**Read/Write**							
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME	INT_EN	USB_SW[1:0]		CEN_OUT	CEN_POL	FUO	RWU_DFT	RWU_LS
RESET	0	1	1	1	1	0	1	1

INT_EN	Interrupt Enable. 0 = Interrupt disabled 1 = Interrupt enabled
USB_SW[1:0]	USB DPDT Switch Control. When the USB switch is forced open (00) or closed (01), the state machine and CEN output are disabled. 00 = DP/DM in high-Z 01 = DP/DM connected to TDP/TDM 10 = DP/DM controlled by CDP/DCP/AM circuitry 11 = DP/DM controlled by CDP/DCP/AM circuitry
CEN_OUT	CEN/$\overline{INT}$ Function Select. Controls the function of the $\overline{INT}$ pin. 0 = $\overline{INT}$ output is used as interrupt 1 = $\overline{INT}$ output is used as CEN
CEN_POL	CEN/$\overline{INT}$ Polarity Select. Controls the polarity of the CEN/$\overline{INT}$ output. 0 = CEN/$\overline{INT}$ output is active-low CEN/$\overline{INT}$ 1 = CEN/$\overline{INT}$ output is active-high CEN/$\overline{INT}$
FUO	Factory Use Only. Do not modify from reset value.
RWU_DFT	Remote Wake-Up Default. 0 = Remote wake-up is off 1 = Remote wake-up is on
RWU_LS	Remote Wake-Up for Low-Speed Only Select. 0 = Remote wake-up for both FS/HS and LS USB devices 1 = Remote wake-up for only LS devices

Interrupt (INT) Register

ADDRESS:	**0x06**							
MODE:	**Read Only**							
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME	CDP_DEVi	BYPASS_CDPi	CDP_CNi	RFU	USB_XFRi	RWUi	CEN_TOG_STi	CEN_TOG_SPi
RESET	0	0	0	0	0	0	0	0

CDP_DEVi	CDP Device Detect Status Interrupt. CDP_DEVi is set when a CDP device is detected following the CDP handshake procedure in CM mode. 0 = No interrupt 1 = Interrupt
BYPASS_CDPi	Bypass CDP Running Status Interrupt. BYPASS_CDPi is set when the CDP handshake procedure is bypassed. 0 = No interrupt 1 = Interrupt
CDP_CNi	CDP Connect Status Interrupt. CDP_CNi is set whenever a CDP connection check is in progress. 0 = No interrupt 1 = Interrupt
RFU	Reserved for Future Use
USB_XFRi	USB Session Interrupt. USB_XFRi is set when there is USB data detected in CM mode and DP/DM are connected to TDP/TDM. 0 = No interrupt 1 = Interrupt
RWUi	Remote Wake-Up Status Interrupt. RWUi is set whenever a remote wake-up is performed in AM mode. 0 = No interrupt 1 = Interrupt
CEN_TOG_STi	CEN Toggle Start Monitor Interrupt. CEN_TOG_STi is set at the start of a V_{BUS} toggle, when V_{BUS} is first disabled. 0 = No interrupt 1 = Interrupt
CEN_TOG_SPi	CEN Toggle Stop Monitor Interrupt. CEN_TOG_SPi is set at the end of a V_{BUS} toggle, when V_{BUS} is no longer disabled. 0 = No interrupt 1 = Interrupt

STATUS Register

ADDRESS:	**0x07**							
MODE:	**Read Only**							
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME	CDP_DEVs	BYPASS_CDPs	CDP_CNs	RFU	USB_XFRs	RWUs	RFU	CEN_TOG_SPs
RESET	0	0	0	0	0	0	0	0
CDP_DEVs	CDP Device Detect Status. CDP_DEVs is set when a CDP device is detected following the CDP handshake procedure in CM mode and cleared when it is disconnected. 0 = CDP device not detected 1 = CDP device detected							
BYPASS_CDPs	Bypass CDP Running Status. BYPASS_CDPs is set when the CDP handshake procedure is bypassed. 0 = CDP signaling used 1 = CDP signaling bypassed							
CDP_CNs	CDP Connect Status. CDP_CNs is set while a CDP connection attempt is in progress. 0 = No CDP connection check in progress 1 = CDP connection check in progress							
RFU	Reserved for Future Use							
USB_XFRs	USB Session Status. USB_XFRs is set while there is USB data detected in CM mode and DP/DM are connected to TDP/TDM. 0 = No USB session in progress 1 = USB session in progress							
RWUs	Remote Wake-Up Status. RWUs is set while a remote wake-up is in progress in AM mode. 0 = Not waiting for RWU 1 = Waiting for RWU							
CEN_TOG_SPs	CEN Toggle Status. CEN_TOGs is cleared at the start of a V_{BUS} toggle and set at the end of the V_{BUS} toggle. 0 = V_{BUS} toggle in progress 1 = V_{BUS} toggle not in progress							

MASK Register

ADDRESS:	**0x08**							
MODE:	**Read/Write**							
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME	CDP_DEVm	BYPASS_CDPm	CDP_CNm	RFU	USB_XFRm	RWUm	CEN_TOG_STm	CEN_TOG_SPm
RESET	0	0	0	0	0	0	0	0

CDP_DEVm	CDP Device Detect Status Interrupt Mask. Prevents an interrupt from being generated in CDP_DEVi when CDP_DEVs is set to 1. 0 = Masked 1 = Not masked
BYPASS_CDPm	Bypass CDP Running Status Interrupt Mask. Prevents an interrupt from being generated in BYPASS_CDPi when BYPASS_CDPs is set to 1. 0 = Masked 1 = Not masked
CDP_CNm	CDP Connect Status Interrupt Mask. Prevents an interrupt from being generated in CDP_CNi when CDP_CNs is set to 1. 0 = Masked 1 = Not masked
RFU	Reserved for Future Use
USB_XFRm	USB Session Interrupt Mask. Prevents an interrupt from being generated in USB_XFRi when USB_XFRs is set to 1. 0 = Masked 1 = Not masked
RWUm	Remote Wake-Up Status Interrupt Mask. Prevents an interrupt from being generated in RWUi when RWUs is set to 1. 0 = Masked 1 = Not masked
CEN_TOG_STm	CEN Toggle Start Monitor Interrupt Mask. Prevents an interrupt from being generated in CEN_TOG_STi when CEN_TOG_STs is set to 1. 0 = Masked 1 = Not masked
CEN_TOG_SPm	CEN Toggle Stop Monitor Interrupt Mask. Prevents an interrupt from being generated in CEN_TOG_SPi when CEN_TOG_SPs is set to 1. 0 = Masked 1 = Not masked

Applications Information

I²C Interface

The MAX14640/MAX14651 contain an I²C-compatible interface for data communication with a host controller (SCL and SDA). The interface supports a clock frequency of up to 400kHz. SCL and SDA require pullup resistors that are connected to a positive supply.

START, STOP, and Repeated START Conditions

When writing to the MAX14640/MAX14651 using I²C, the master sends a START condition (S) followed by the MAX14640/MAX14651 I²C address. After the address, the master sends the register address of the register that is to be programmed. The master then ends communication by issuing a STOP condition (P) to relinquish control of the bus, or a Repeated START condition (Sr) to communicate to another I²C slave. See Figure 7.

Slave Address

The MAX14640 and MAX14651 are the I²C versions that have different slave addresses (Table 8). Set the read/write bit high to configure the MAX14640/MAX14651 to read mode. Set the read/write bit low to configure the MAX14640/MAX14651 to write mode. The address is the first byte of information sent to the MAX14640/MAX14651 after the START condition.

Bit Transfer

One data bit is transferred on the rising edge of each SCL clock cycle. The data on SDA must remain stable during the high period of the SCL clock pulse. Changes in SDA while SCL is high and stable are considered control signals (see the *START, STOP, and Repeated START Conditions* section). Both SDA and SCL remain high when the bus is not active.

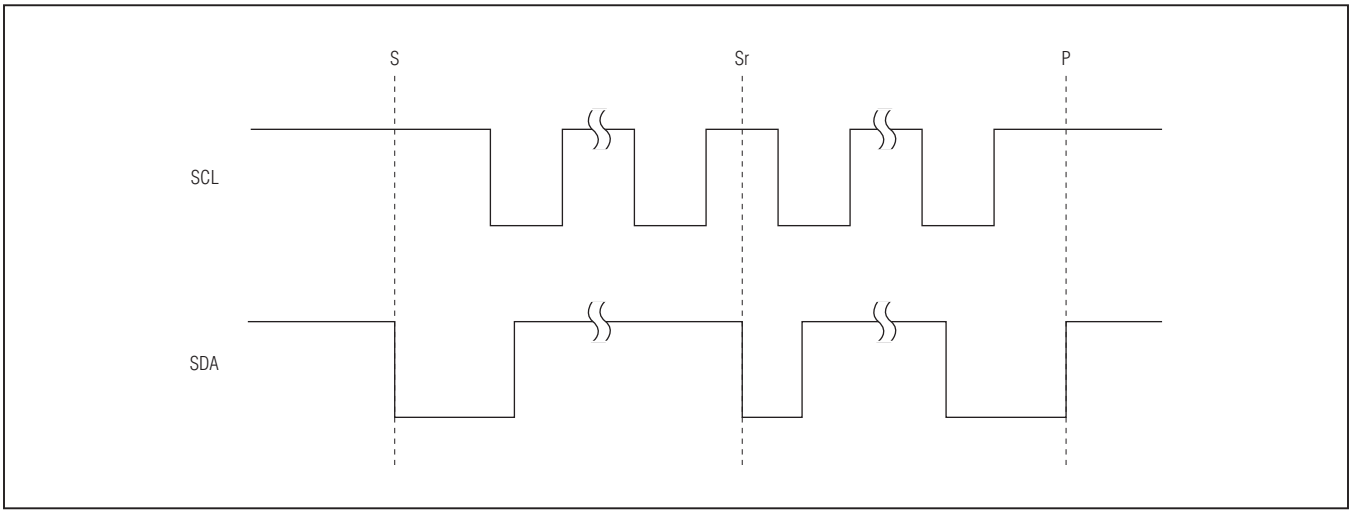


Figure 7. I²C START, STOP, and Repeated START Conditions

Table 8. I²C Slave Addresses

ADDRESS FORMAT	MAX14640		MAX14651	
	HEX	BINARY	HEX	BINARY
7-Bit Slave ID	0x35	011 0101	0x15	001 0101
Write Address	0x6A	0110 1010	0x2A	0010 1010
Read Address	0x6B	0110 1011	0x2B	0010 1011

Single-Byte Write

In this operation, the master sends an address and two data bytes to the slave device (Figure 8). The following procedure describes the single-byte write operation:

1) The master sends a START condition.
2) The master sends the 7-bit slave address plus a write bit (low).
3) The addressed slave asserts an ACK on the data line.
4) The master sends the 8-bit register address.
5) The slave asserts an ACK on the data line only if the address is valid (NAK if not).
6) The master sends eight data bits.
7) The slave asserts an ACK on the data line.
8) The master generates a STOP condition.

Burst Write

In this operation, the master sends an address and multiple data bytes to the slave device (Figure 9). The slave device automatically increments the register address after each data byte is sent, unless the register being accessed is 0x00, in which case the register address remains the same. The following procedure describes the burst write operation:

1) The master sends a START condition.
2) The master sends the 7-bit slave address plus a write bit (low).
3) The addressed slave asserts an ACK on the data line.
4) The master sends the 8-bit register address.
5) The slave asserts an ACK on the data line only if the address is valid (NAK if not).
6) The master sends eight data bits.
7) The slave asserts an ACK on the data line.
8) Repeat 6 and 7 (N - 1) times.
9) The master generates a STOP condition.

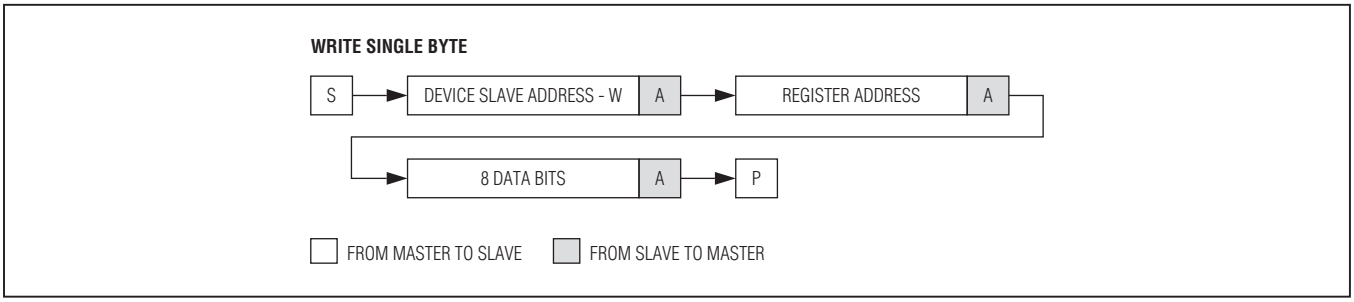


Figure 8. Write Byte Sequence

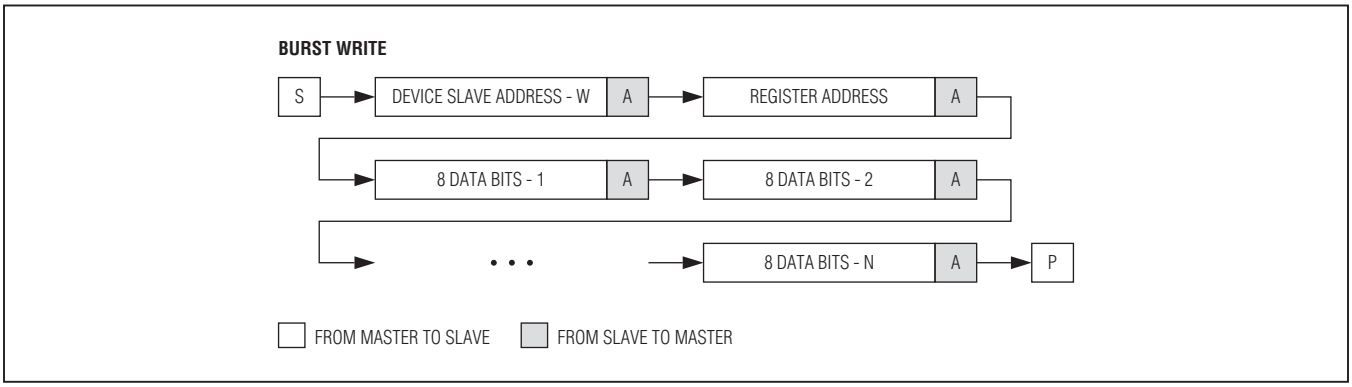


Figure 9. Burst Write Sequence

Single-Byte Read

In this operation, the master sends an address plus two data bytes and receives one data byte from the slave device (Figure 10). The following procedure describes the single-byte read operation:

1) The master sends a START condition.
2) The master sends the 7-bit slave address plus a write bit (low).
3) The addressed slave asserts an ACK on the data line.
4) The master sends the 8-bit register address.
5) The slave asserts an ACK on the data line only if the address is valid (NAK if not).
6) The master sends a Repeated START condition.
7) The master sends the 7-bit slave address plus a read bit (high).
8) The addressed slave asserts an ACK on the data line.
9) The slave sends eight data bits.
10) The master asserts a NACK on the data line.
11) The master generates a STOP condition.

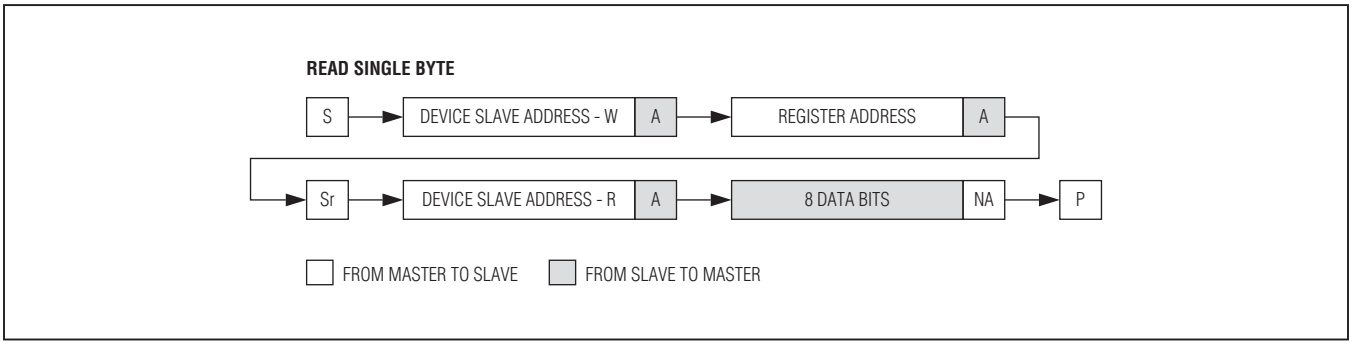


Figure 10. Read Byte Sequence

Burst Read

In this operation, the master sends an address plus two data bytes and receives multiple data bytes from the slave device (Figure 11). The following procedure describes the burst byte read operation:

1) The master sends a START condition.
2) The master sends the 7-bit slave address plus a write bit (low).
3) The addressed slave asserts an ACK on the data line.
4) The master sends the 8-bit register address.
5) The slave asserts an ACK on the data line only if the address is valid (NAK if not).
6) The master sends a Repeated START condition.
7) The master sends the 7-bit slave address plus a read bit (high).
8) The slave asserts an ACK on the data line.
9) The slave sends eight data bits.
10) The master asserts an ACK on the data line.
11) Repeat 9 and 10 (N - 2) times.
12) The slave sends the last eight data bits.
13) The master asserts a NACK on the data line.
14) The master generates a STOP condition.

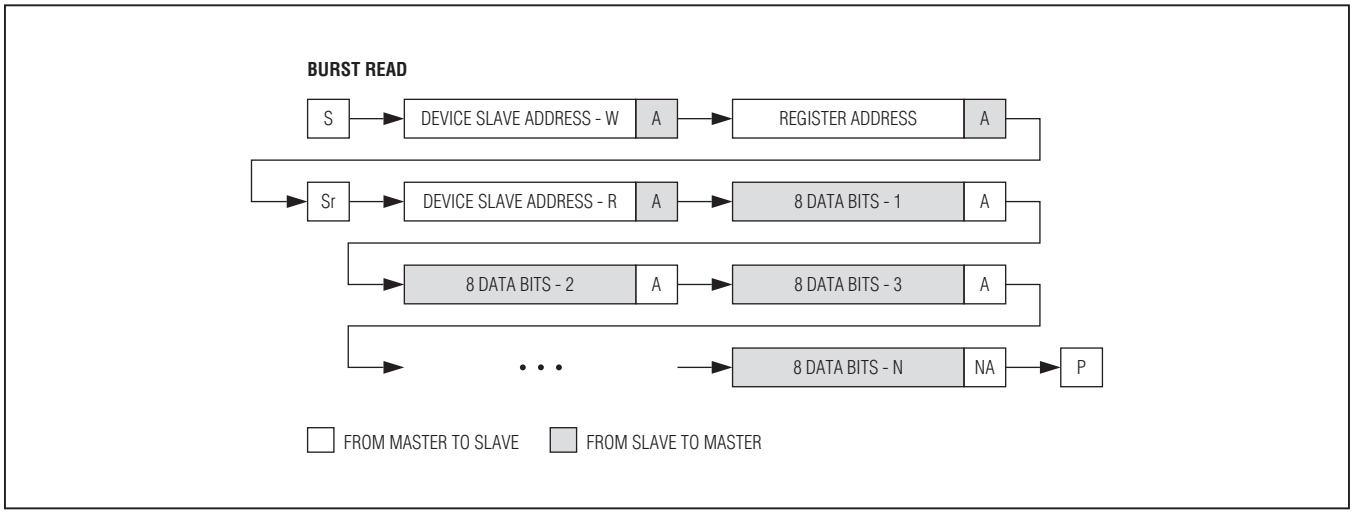


Figure 11. Burst Read Sequence

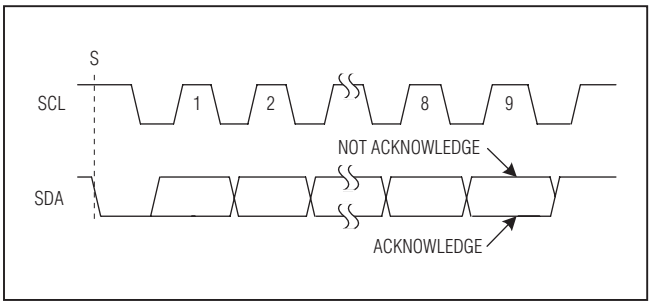


Figure 12. Acknowledge

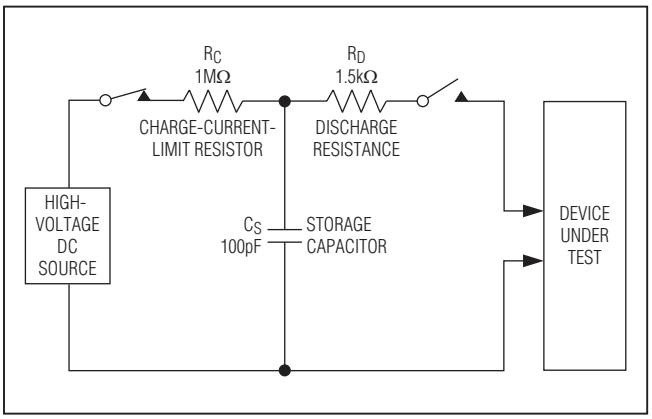


Figure 13. Human Body ESD Test Model

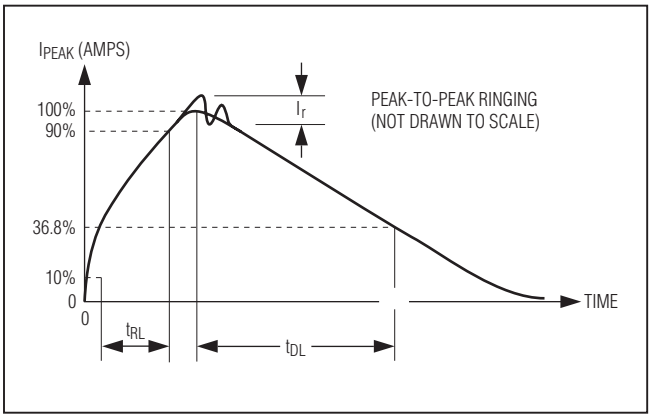


Figure 14. Human Body Current Waveform

Acknowledge Bits

Data transfers are acknowledged with an acknowledge bit (ACK) or a not-acknowledge bit (NACK). Both the master and the MAX14640/MAX14651 generate ACK bits. To generate an ACK, pull SDA low before the rising edge of the ninth clock pulse, and hold it low during the high period of the ninth clock pulse (see Figure 12). To generate a NACK, leave SDA high before the rising edge of the ninth clock pulse, and leave it high for the duration of the ninth clock pulse. Monitoring for NACK bits allows for detection of unsuccessful data transfers.

High-ESD Protection

Electrostatic Discharge (ESD)-protection structures are incorporated on all pins to protect against electrostatic discharges up to ±2kV Human Body Model (HBM) encountered during handling and assembly. DP and DM are further protected against ESD up to ±15kV (HBM) without damage. The ESD structures withstand high ESD both in normal operation and when the device is powered down. After an ESD event, the MAX14640–MAX14644/MAX14651 continue to function without latchup.

ESD Test Conditions

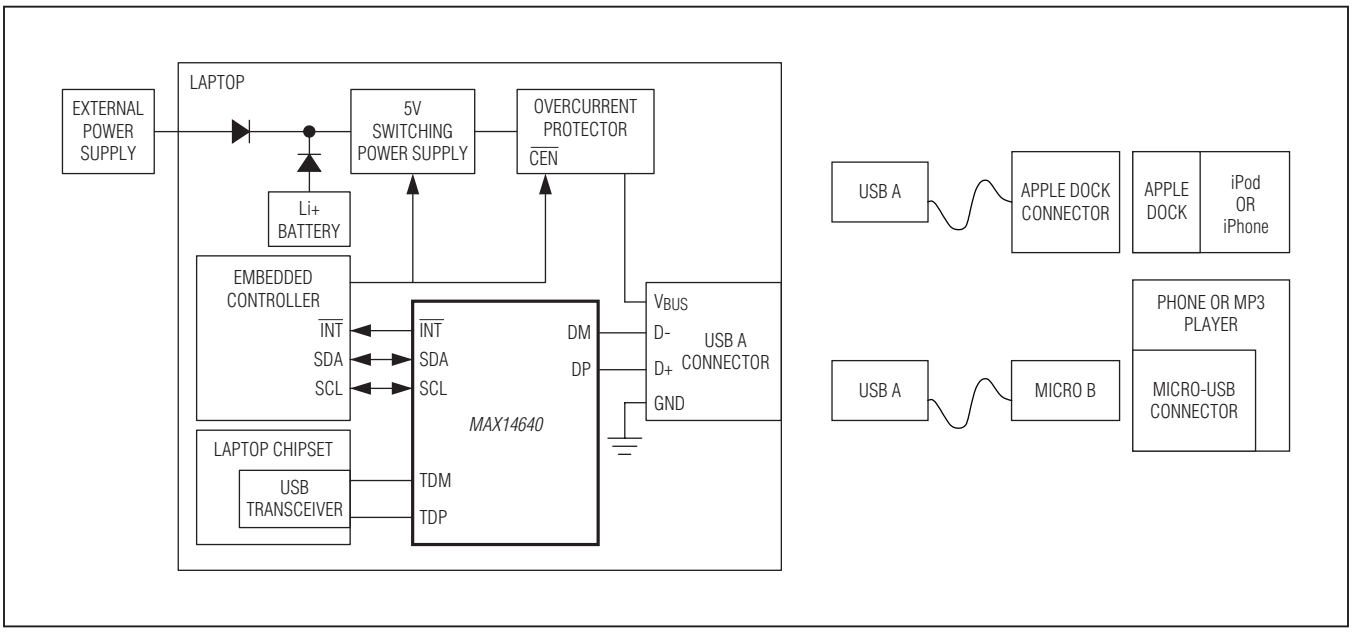
ESD performance depends on a variety of conditions. Contact Maxim for a reliability report that documents test setup, test methodology, and test results.

The MAX14640–MAX14644/MAX14651 require a 1µF capacitor on both V_{CC} to GND to guarantee full ESD protection.

Human Body Model

Figure 13 shows the Human Body Model. Figure 14 shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest that is then discharged into the device through a 1.5kΩ resistor.

Typical Operating Circuit



Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX14640ETA+T	-40°C to +85°C	8 TDFN-EP*
MAX14641ETA+T	-40°C to +85°C	8 TDFN-EP*
MAX14642ETA+T	-40°C to +85°C	8 TDFN-EP*
MAX14643ETA+T	-40°C to +85°C	8 TDFN-EP*
MAX14644ETA+T	-40°C to +85°C	8 TDFN-EP*
MAX14651ETA+T	-40°C to +85°C	8 TDFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*
T = Tape and reel.

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
8 TDFN	T822+2	21-0168	90-0065

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	9/12	Initial release	—
1	4/13	Updated *Electrical Characteristics* table, updated Figure 4, removed TOCS 11 and 12, updated *Pin Description* and *Register Map/Register Descriptions*.	3, 7, 9, 10, 16