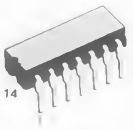
SGS-THOMSON MICROELECTRONICS

M54HC393
M74HC393

DUAL BINARY COUNTER

- HIGH SPEED
  t_{PD} = 14 ns (TYP) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS393

B1N
Plastic Package



F1
Ceramic Frit Seal Package

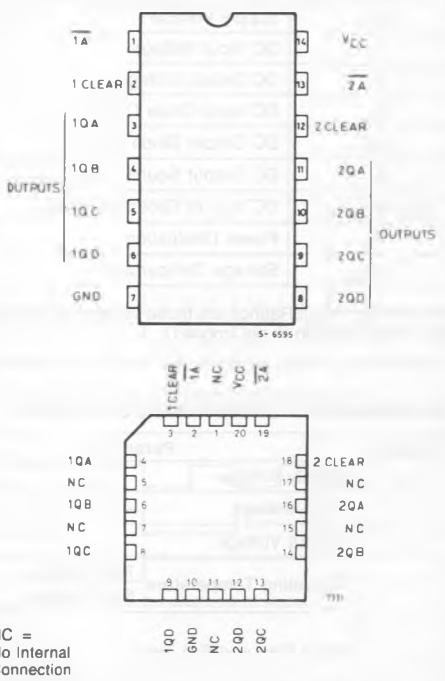
M1
Micro Package

C1
Plastic Chip Carrier

ORDERING NUMBERS:

M54HC393 F1
M74HC393 B1N
M74HC393 F1
M74HC393 C1
M74HC393 M1

PIN CONNECTION (top view)



NC = No Internal Connection

DESCRIPTION

The M54/74HC393 is a high speed CMOS DUAL BINARY COUNTER fabricated in silicon gate C²MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption.

This counter circuit contains independent ripple carry counters and two 4-bit ripple carry binary counters, which can be cascaded to create a single divide-by-256 counter.

Each 4-bit counter is incremented on the high to low transition (negative edge) of the clock input, and each has an independent clear input. When clear is set low all four bits of each counter are sec to a low level. This enables count truncation and allows the implementation of divide-by-N counter configurations.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

TRUTH TABLE

COUNT	OUTPUT			
	QD	QC	QB	QA
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

INPUTS		OUTPUTS			
$\overline{CLEAR}$	CLEAR	QA	QB	QC	QD
X	H	L	L	L	L
↓	L	COUNT UP			
↑	L	NO CHANGE			

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	− 0.5 to 7	V
V_I	DC Input Voltage	− 0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	− 0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	− 65 to 150	°C

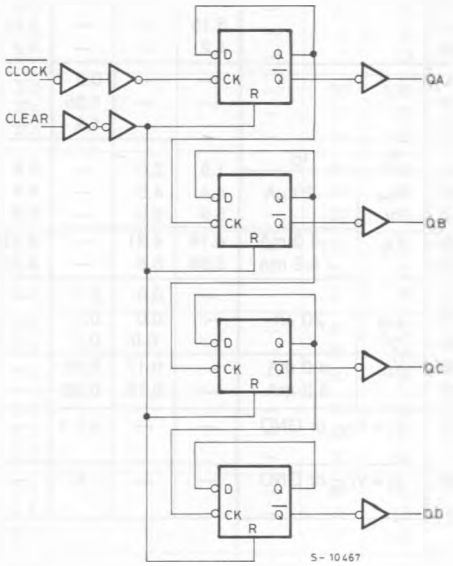
Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≡ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

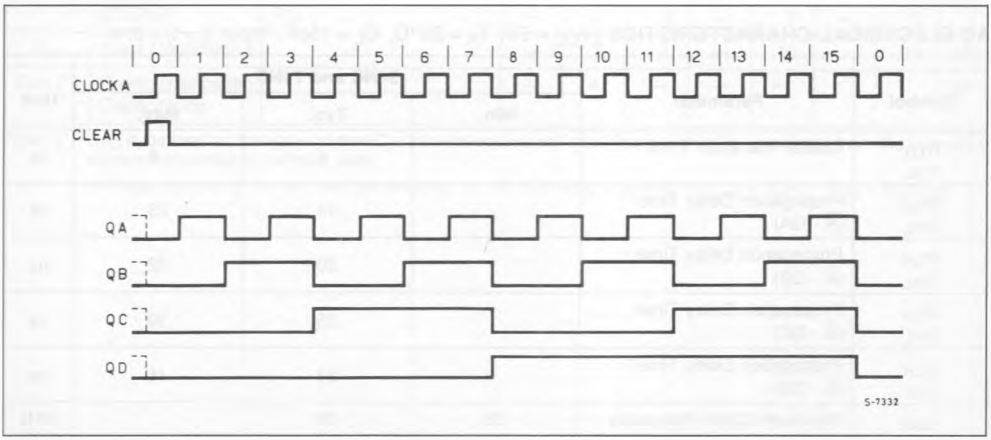
RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Limit		Unit
V_{CC}	Supply Voltage		2 to 6		V
V_I	Input Voltage		0 to V_{CC}		V
V_O	Output Voltage		0 to V_{CC}		V
T_A	Operating Temperature	74HC Series 54HC Series	− 40 to 85 − 55 to 125		°C
t_r, t_f	Input Rise and Fall Time		V_{CC} = 2 V	0 to 1000	ns
			V_{CC} = 4.5 V	0 to 500	
			V_{CC} = 6 V	0 to 400	

LOGIC DIAGRAM



TIMING CHART



DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		−4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−5.2 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0	V_{IH} or V_{IL}	20 μA	—	0.0	0.1	—	0.1	—	0.1	V
		4.5			—	0.0	0.1	—	0.1	—	0.1	
		6.0			—	0.0	0.1	—	0.1	—	0.1	
		4.5		4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
I_I	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND		—	—	±0.1	—	±1.0	—	±1.0	μA
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND		—	—	4	—	40	—	80	μA

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{A}$ - QA)		14	23	ns
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{A}$ - QB)		20	32	ns
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{A}$ - QC)		25	39	ns
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{A}$ - QD)		31	48	ns
f_{MAX}	Maximum Clock Frequency	35	68		MHz

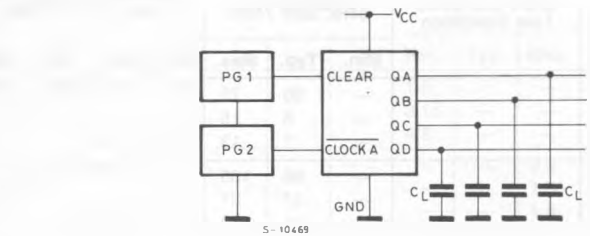
AC ELECTRICAL CHARACTERISTICS (C_L = 50pF, Input $t_r = t_f$ = 6ns)

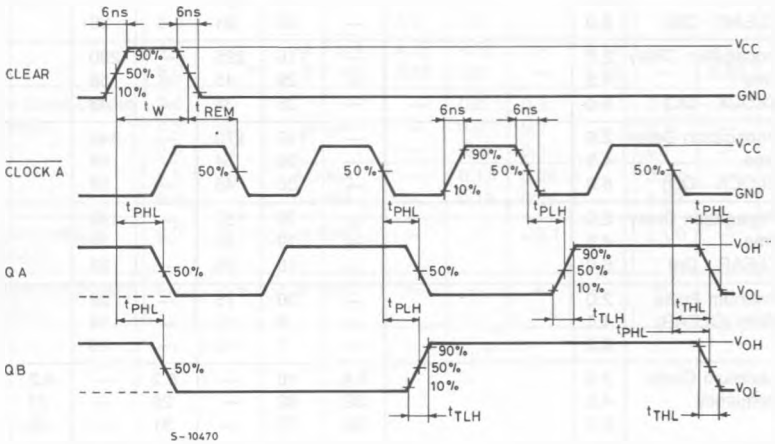
Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0		—	30	75	—	95		110	ns
		4.5		—	8	15	—	19		22	
		6.0		—	7	13	—	16		19	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{CLOCK}$ - QA)	2.0		—	68	135	—	170		205	ns
		4.5		—	17	27	—	34		41	
		6.0		—	14	23	—	29		35	
t_{PLH} t_{PHL}	Propagation Delay Time (CLEAR - QB)	2.0		—	92	180	—	225		270	ns
		4.5		—	23	36	—	45		54	
		6.0		—	20	31	—	38		46	
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK - QC)	2.0		—	116	225	—	280		340	ns
		4.5		—	29	45	—	58		68	
		6.0		—	25	38	—	48		58	
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK - QD)	2.0		—	140	270	—	340		405	ns
		4.5		—	35	54	—	68		81	
		6.0		—	30	46	—	58		69	
t_{PHL}	Propagation Delay Time (CLEAR - Qn)	2.0		—	76	150	—	190		225	ns
		4.5		—	19	30	—	38		45	
		6.0		—	16	26	—	33		38	
$t_{W(H)}$	Minimum Pulse Width (CLEAR)	2.0		—	30	75	—	95		110	ns
		4.5		—	8	15	—	19		22	
		6.0		—	7	13	—	16		19	
f_{MAX}	Maximum Clock Frequency	2.0		6.4	16	—	5.2	—	4.2	—	MHz
		4.5		32	62	—	26	—	21	—	
		6.0		38	73	—	31	—	25	—	
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width ($\overline{CLOCK}$)	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t_{REM}	Minimum Removal Time (CLEAR)	2.0		—	—	25	—	30	—	38	ns
		4.5		—	—	5	—	6	—	8	
		6.0		—	—	5	—	5	—	6	
C_{IN}	Input Capacitance			—	5	10	—	10		10	pF
C_{PD} (*)	Power Dissipation Capacitance			—	41	—	—	—			pF

Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load.

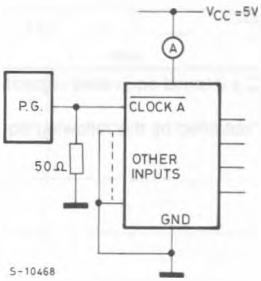
Average operating current can be obtained by the following equation $I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

SWITCHING CHARACTERISTICS TEST WAVEFORM





TEST CIRCUIT I_{CC} (Opr.)



INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST