SGS-THOMSON MICROELECTRONICS

M54/74HC192
M54/74HC193

HC192 - SYNCHRONOUS UP/DOWN DECADE COUNTER
HC193 - SYNCHRONOUS UP/DOWN BINARY COUNTER

- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  V_{NIH} = V_{NIL} = 28% V_{CC} (Min.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}|$ = I_{OL} = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  t_{PLH} = t_{PHL}
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS192-193

B1N
Plastic Package

F1
Ceramic Frit Seal Package

M1
Micro Package

C1
Plastic Chip Carrier

ORDERING NUMBERS:

M54HCXXX F1
M74HCXXX B1N
M74HCXXX F1
M74HCXXX C1
M74HCXXX M1

DESCRIPTION

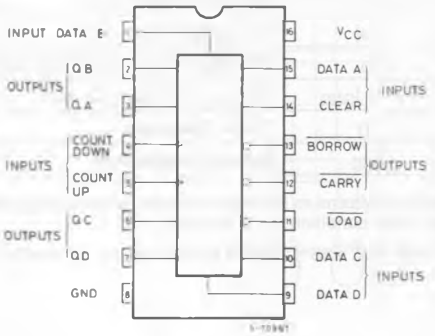
The M54/74HC192/193 are a high speed CMOS SYNCHRONOUS UP/DOWN DECADE COUNTERS fabricated in silicon gate C²MOS technology. They have the same high speed performance of LSTTL combined with true CMOS low power consumption. The counter has two separate clock inputs, an UP COUNT input and a DOWN COUNT input. All outputs of the flip-flop are simultaneously triggered on the low to high transition of either clock while the other input is held high. The direction of counting is determined by which input is clocked. This counter may be preset by entering the desired data on the DATA A, DATA B, DATA C, and DATA D input. When the LOAD input is taken low the data is loaded independently of either clock input. This feature allows the counters to be used as divide-by-n counters by modifying the count length with the preset inputs.

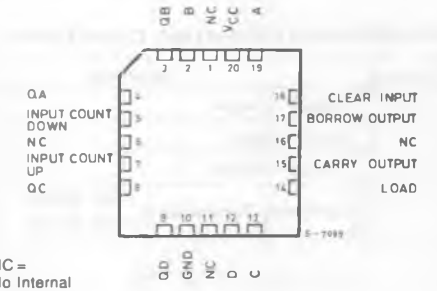
In addition the counter can also be cleared. This is accomplished by inputting a high on the CLEAR input. All 4 internal stages are set to low independently of either COUNT input.

Both a BORROW and CARRY output are provided to enable cascading of both up and down counting functions. The BORROW output produces a negative going pulse when the counter underflows and the CARRY outputs a pulse when the counter overflows. The counter can be cascaded by connecting the CARRY and BORROW outputs of one device to the COUNT UP and COUNT DOWN inputs, respectively, of the next device.

All inputs are equipped with protection circuits against static discharge and transient excess voltage.

PIN CONNECTIONS (top view)





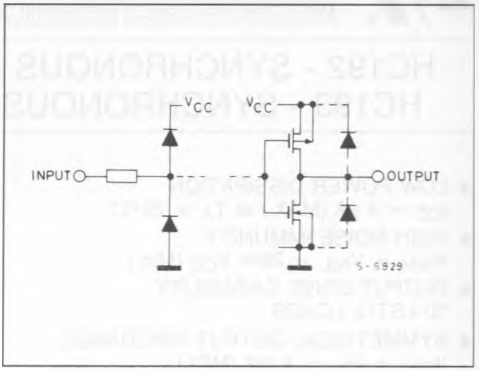
NC = No Internal Connection

TRUTH TABLE

Count Up	Count Down	$\overline{Load}$	Clear	Function
⊓	H	H	L	COUNT UP
H	⊓	H	L	NO COUNT
⊓	H	H	L	COUNT DOWN
H	⊓	H	L	NO COUNT
X	X	L	L	PRESET
X	X	X	H	RESET

X = DON'T CARE

INPUT AND OUTPUT EQUIVALENT CIRCUIT



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	− 0.5 to 7	V
V_I	DC Input Voltage	− 0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	− 0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	− 65 to 150	°C

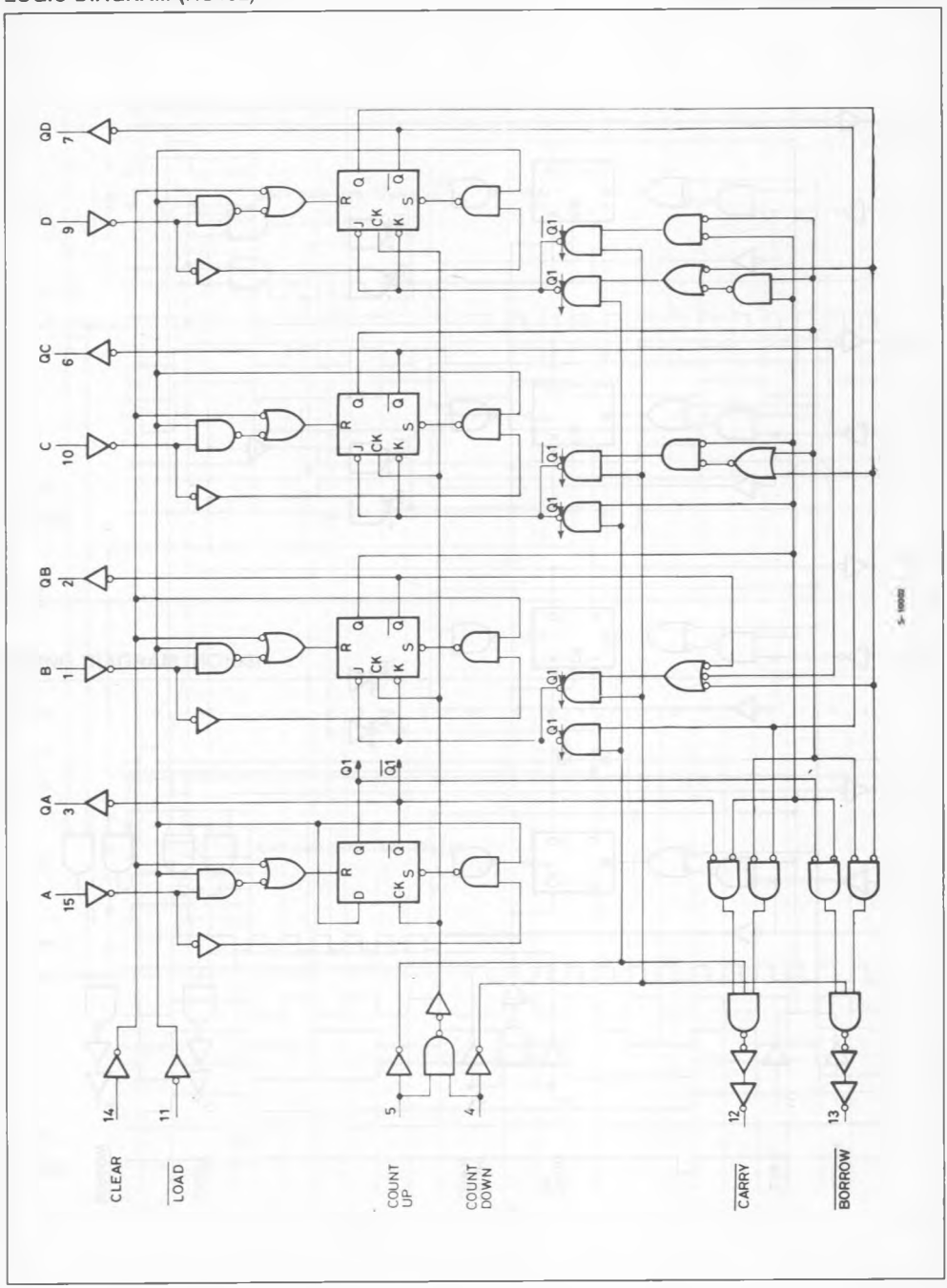
Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

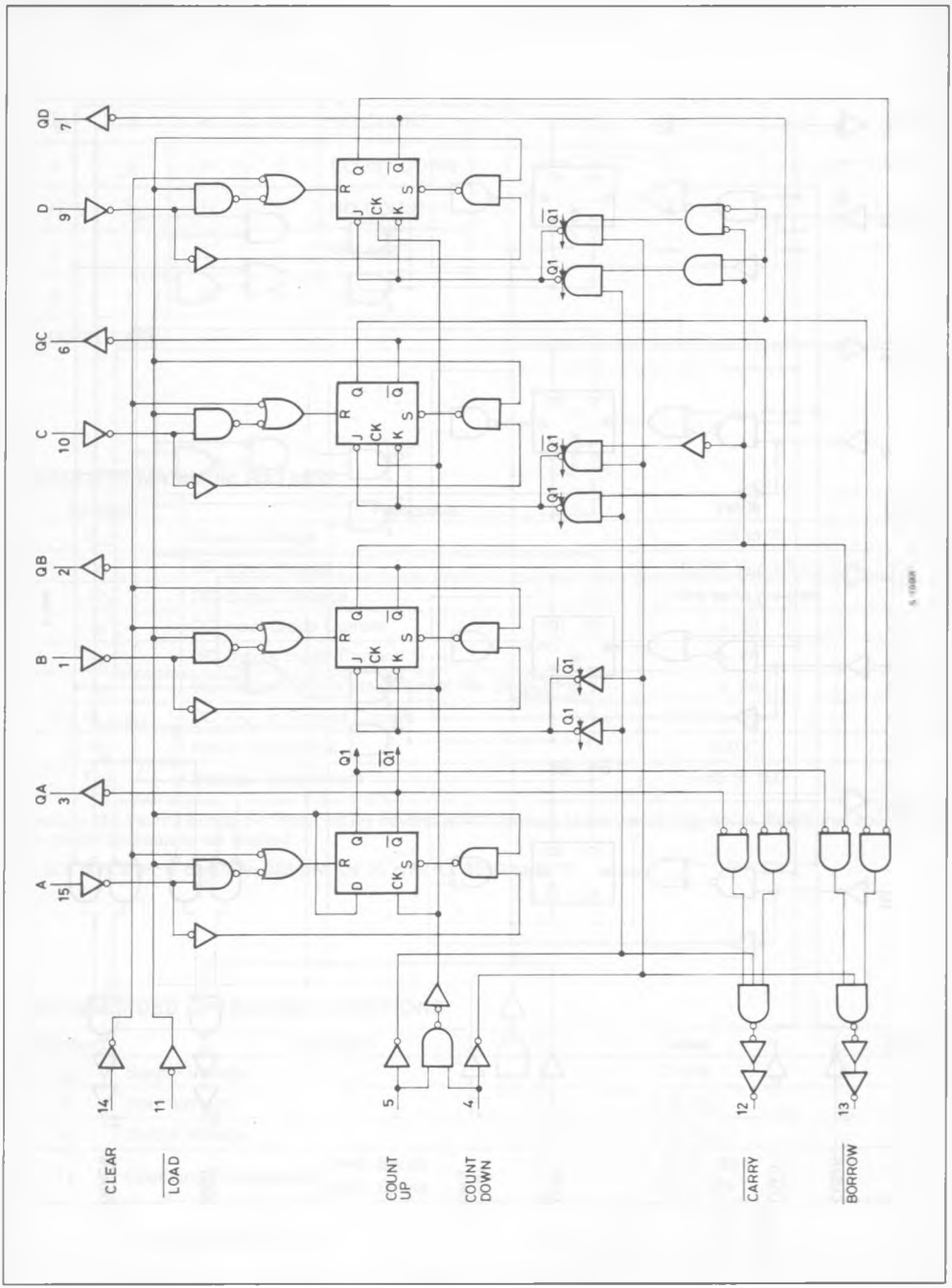
RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value		Unit
V_{CC}	Supply Voltage		2 to 6		V
V_I	Input Voltage		0 to V_{CC}		V
V_O	Output Voltage		0 to V_{CC}		V
T_A	Operating Temperature	74HC Series 54HC Series	− 40 to 85 − 55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V V_{CC} = 4.5V V_{CC} = 6 V	0 to 1000 0 to 500 0 to 400		ns

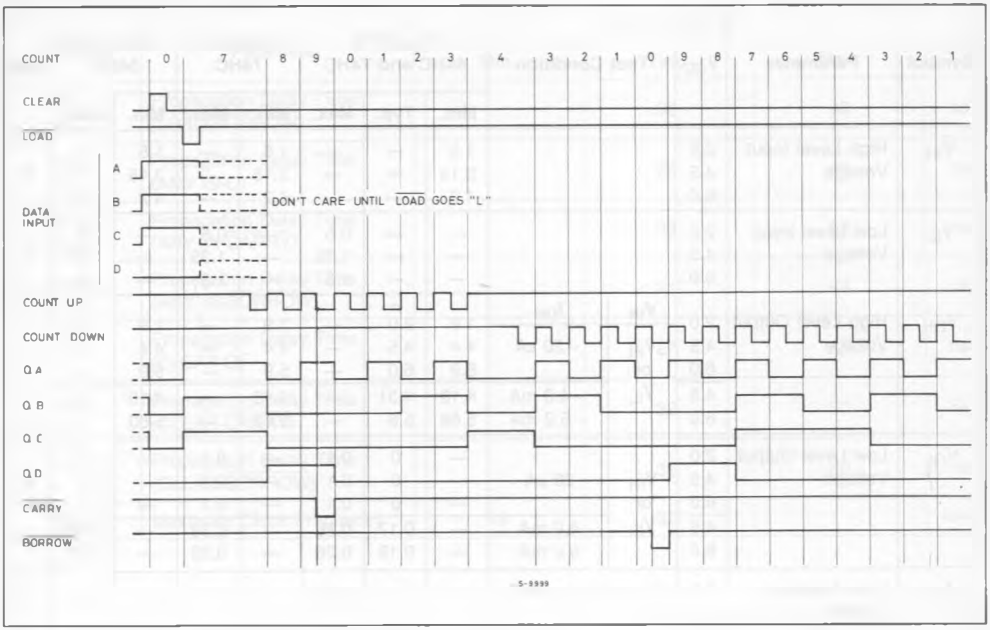
LOGIC DIAGRAM (HC192)



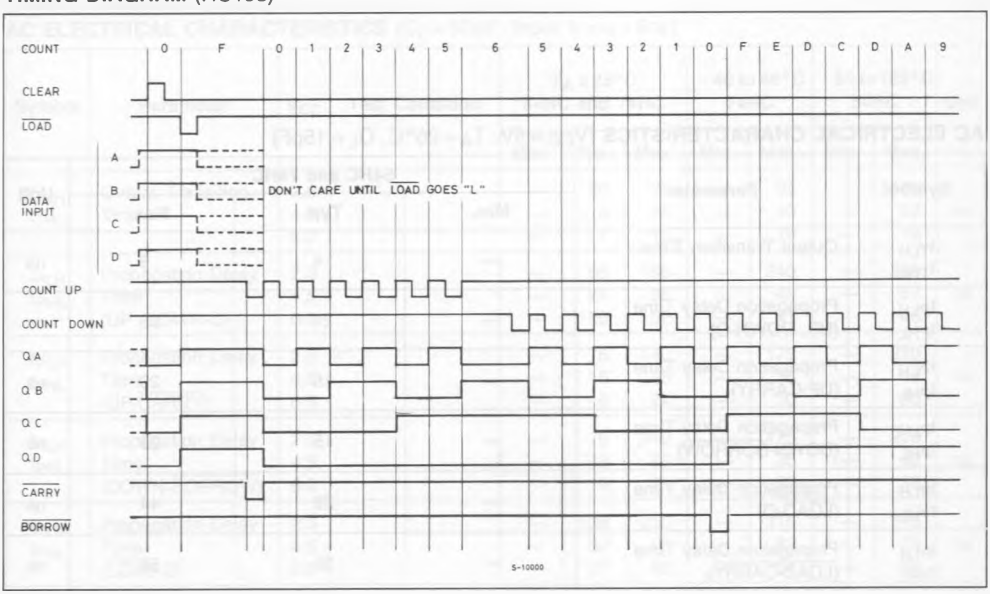
LOGIC DIAGRAM (HC193)



TIMING DIAGRAM (HC192)



TIMING DIAGRAM (HC193)



DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_{IN}	I_{OH}	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		−4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−5.2 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0	V_{IH} or V_{IL}	20 μA	—	0	0.1	—	0.1	—	0.1	V
		4.5			—	0	0.1	—	0.1	—	0.1	
		6.0			—	0	0.1	—	0.1	—	0.1	
		4.5		4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
I_{IN}	Input Leakage Current	6.0	$V_{IN} = V_{CC}$ or GND		—	—	±0.1	—	±1	—	±1	μA
I_{CC}	Quiescent Supply Current	6.0	$V_{IN} = V_{CC}$ or GND		—	—	4	—	40	—	80	

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15pF$)

Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time	—	4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time (UP, DOWN-Q)	—	21	33	ns
t_{PLH} t_{PHL}	Propagation Delay Time (UP-CARRY)	—	15	23	ns
t_{PLH} t_{PHL}	Propagation Delay Time (DOWN-$\overline{\text{BORROW}}$)	—	15	23	ns
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{\text{LOAD}}$-Q)	—	28	44	ns
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{\text{LOAD}}$-CARRY)	—	35	54	ns

AC ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{\text{LOAD}}$-$\overline{\text{BORROW}}$)		32	49	ns
t_{PLH} t_{PHL}	Propagation Delay Time (ANY IN-Q)		26	40	ns
t_{PLH} t_{PHL}	Propagation Delay Time (ANY IN-$\overline{\text{CARRY}}$)		38	58	ns
t_{PLH} t_{PHL}	Propagation Delay Time (ANY IN-$\overline{\text{BORROW}}$)		31	48	ns
t_{PHL}	Propagation Delay Time (CLEAR-Q)		27	43	ns
t_{PLH}	Propagation Delay Time (CLEAR-$\overline{\text{CARRY}}$)		32	50	ns
t_{PHL}	Propagation Delay Time (CLEAR-$\overline{\text{BORROW}}$)		32	50	ns
f_{MAX}	Maximum Clock Frequency	18	32		MHz

AC ELECTRICAL CHARACTERISTICS (C_L = 50pF, Input $t_r = t_f$ = 6ns)

Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t_{PLH} t_{PHL}	Propagation Delay Time (UP, DOWN-Q)	2.0		—	96	190	—	240	—	285	ns
		4.5		—	24	38	—	48	—	57	
		6.0		—	20	32	—	41	—	48	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{\text{UP}}$-$\overline{\text{CARRY}}$)	2.0		—	76	140	—	175	—	210	ns
		4.5		—	18	28	—	35	—	42	
		6.0		—	15	24	—	30	—	36	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{\text{DOWN}}$-$\overline{\text{BORROW}}$)	2.0		—	76	140	—	175	—	210	ns
		4.5		—	18	28	—	35	—	42	
		6.0		—	15	24	—	30	—	36	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{\text{LOAD}}$-Q)	2.0		—	128	250	—	315	—	375	ns
		4.5		—	32	50	—	63	—	75	
		6.0		—	27	43	—	54	—	64	

AC ELECTRICAL CHARACTERISTICS (Continued)

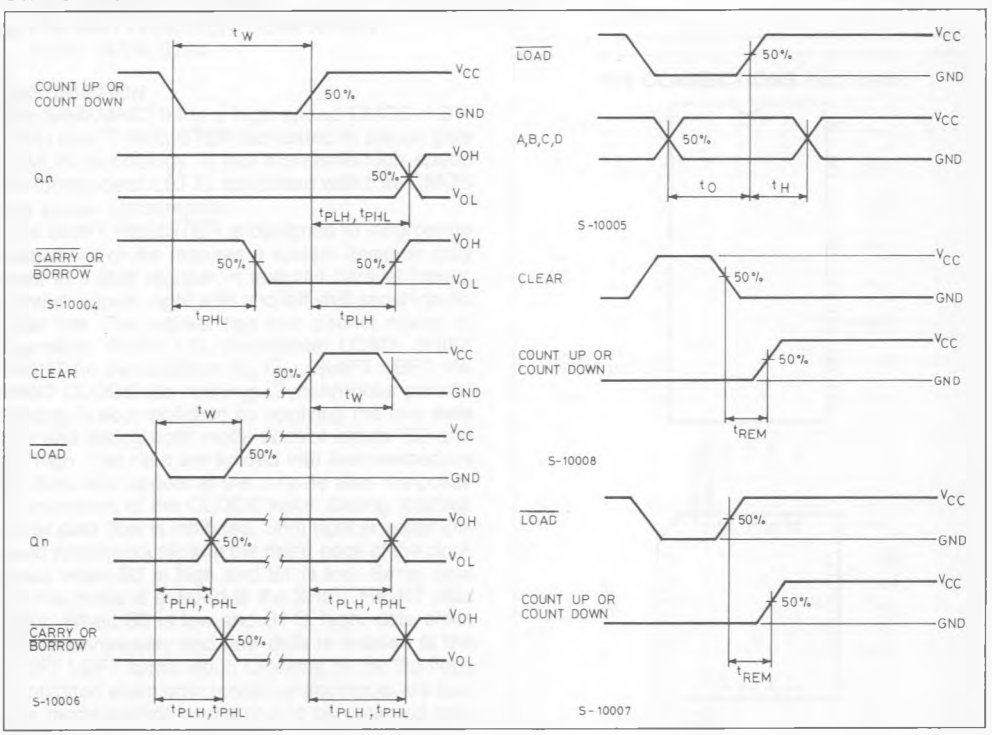
Symbol	Parameter	V_{CC}	Test Condition	$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{LOAD}$-$\overline{CARRY}$)	2.0		—	160	310	—	390	—	465	ns
		4.5		—	40	62	—	78	—	93	
		6.0		—	34	53	—	66	—	79	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{LOAD}$-$\overline{BORROW}$)	2.0		—	144	280	—	350	—	420	ns
		4.5		—	36	56	—	70	—	84	
		6.0		—	31	48	—	60	—	71	
t_{PLH} t_{PHL}	Propagation Delay Time (ANY IN-Q)	2.0		—	116	230	—	290	—	345	ns
		4.5		—	29	46	—	58	—	69	
		6.0		—	25	39	—	49	—	59	
t_{PLH} t_{PHL}	Propagation Delay Time (ANY IN-$\overline{CARRY}$)	2.0		—	172	330	—	415	—	495	ns
		4.5		—	43	66	—	83	—	99	
		6.0		—	37	56	—	71	—	84	
t_{PLH} t_{PHL}	Propagation Delay Time (ANY IN-$\overline{BORROW}$)	2.0		—	144	275	—	345	—	415	ns
		4.5		—	36	55	—	69	—	83	
		6.0		—	31	47	—	59	—	71	
t_{PHL}	Propagation Delay Time (CLEAR-Q)	2.0		—	128	245	—	305	—	370	ns
		4.5		—	32	49	—	61	—	74	
		6.0		—	27	42	—	52	—	63	
t_{PLH}	Propagation Delay Time (CLEAR-$\overline{CARRY}$)	2.0		—	148	285	—	355	—	430	ns
		4.5		—	37	57	—	71	—	86	
		6.0		—	31	48	—	60	—	73	
t_{PHL}	Propagation Delay Time (CLEAR-$\overline{BORROW}$)	2.0		—	148	285	—	355	—	430	ns
		4.5		—	37	57	—	71	—	86	
		6.0		—	31	48	—	60	—	73	
f_{MAX}	Maximum Clock Frequency	2.0		3	7	—	2.6	—	2	—	MHz
		4.5		16	29	—	13	—	11	—	
		6.0		19	34	—	15	—	13	—	
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width (CLOCK)	2.0		—	70	150	—	190	—	225	ns
		4.5		—	17	30	—	38	—	45	
		6.0		—	14	26	—	33	—	38	
$t_{W(H)}$	Minimum Pulse Width ($\overline{LOAD}$)	2.0		—	50	100	—	125	—	150	ns
		4.5		—	12	20	—	25	—	30	
		6.0		—	10	17	—	21	—	26	
$t_{W(H)}$	Minimum Pulse Width (CLEAR)	2.0		—	45	100	—	125	—	150	ns
		4.5		—	11	20	—	25	—	30	
		6.0		—	9	17	—	21	—	26	
t_{REM}	Minimum Removal Time ($\overline{LOAD}$)	2.0		—	20	75	—	95	—	110	ns
		4.5		—	5	15	—	19	—	22	
		6.0		—	4	13	—	16	—	19	
t_{REM}	Minimum Removal Time (CLEAR)	2.0		—	5	50	—	65	—	75	ns
		4.5		—	1	10	—	13	—	15	
		6.0		—	1	9	—	11	—	13	

AC ELECTRICAL CHARACTERISTICS (Continued)

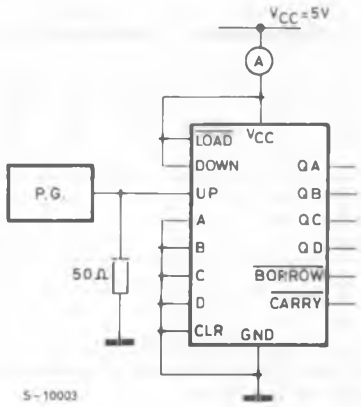
Symbol	Parameter	V_{CC}	Test Condition	$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_s	Minimum Set-up Time (DATA-$\overline{LOAD}$)	2.0		—	40	100	—	125	—	150	ns
		4.5		—	10	20	—	25	—	30	
		6.0		—	9	17	—	21	—	26	
t_h	Minimum Hold Time (DATA-$\overline{LOAD}$)	2.0		—	—	0	—	0	—	0	ns
		4.5		—	—	0	—	0	—	0	
		6.0		—	—	0	—	0	—	0	
C_{IN}	Input Capacitance			—	5	10	—	10	—	10	pF
C_{PD} (*)	Power Dissipation Capacitance			—	66	—	—	—	—	—	pF

Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit)
Average operating current is: $I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

SWITCHING CHARACTERISTICS TEST WAVEFORM



TEST CIRCUIT I_{CC} (Opr.)



TRANSITION TIME OF INPUT WAVEFORMS IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST