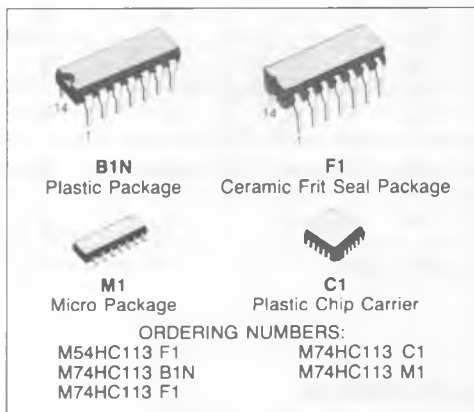


DUAL J-K FLIP FLOP WITH PRESET

- **HIGH SPEED**
 $f_{MAX} = 64 \text{ MHz (Typ.) at } V_{CC} = 5V$
- **LOW POWER DISSIPATION**
 $I_{CC} = 2 \mu A \text{ at } T_A = 25^\circ C$
- **HIGH NOISE IMMUNITY**
 $V_{NIH} = V_{NIL} = 28\% V_{CC} \text{ (MIN.)}$
- **OUTPUT DRIVE CAPABILITY**
 10 LSTTL LOADS
- **SYMMETRICAL OUTPUT IMPEDANCE**
 $|I_{OH}| = I_{OL} = 4 \text{ mA (MIN.)}$
- **BALANCED PROPAGATION DELAYS**
 $t_{PLH} = t_{PHL}$
- **WIDE OPERATING VOLTAGE RANGE**
 $V_{CC} \text{ (OPR)} = 2 \text{ to } 6V$
- **PIN AND FUNCTION COMPATIBLE**
 WITH 54/74LS113



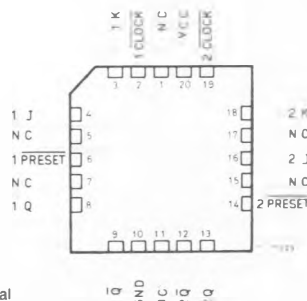
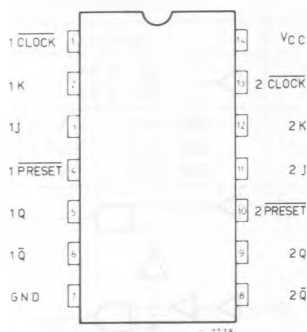
DESCRIPTION

The M54/74HC113 is a high speed CMOS DUAL J-K FLIP FLOP WITH PRESET fabricated in silicon gate C²MOS technology.

It has the same high speed performance of LSTTL combined with true CMOS low power consumption. This circuit offers individual J, K, set, and clock inputs. These monolithic dual flip-flops are designed so that when the clock pulse is HIGH, the inputs are enabled and data will be accepted. The logic level of the J and K inputs may be allowed to change when the clock pulse is HIGH and the bistable will function as shown in the truth table as long as minimum set-up times are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

All inputs are equipped with protection circuits against static discharge and transient excess voltage.

PIN CONNECTIONS (top view)

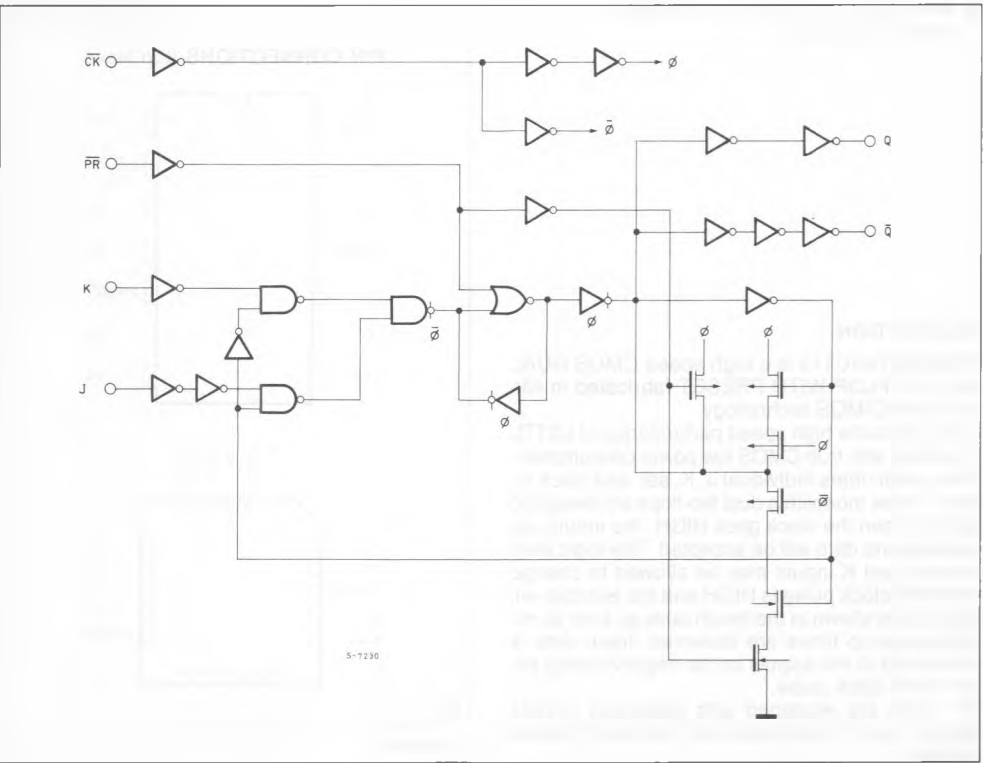


TRUTH TABLE

INPUTS				OUTPUT		FUNCTION
PR	J	K	CK	Q	Q̄	
L	X	X	X	H	L	PRESET
H	L	L	⌵	Qn	Q̄n	NO CHANGE
H	L	H	⌵	L	H	
H	H	L	⌵	H	L	
H	H	H	⌵	Q̄n	Qn	TOGGLE
H	X	X	⌶	Qn	Q̄n	NO CHANGE

X: DON'T CARE

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	- 0.5 to 7	V
V_I	DC Input Voltage	- 0.5 to $V_{CC} + 0.5$	V
V_O	DC Output Voltage	- 0.5 to $V_{CC} + 0.5$	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	- 65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

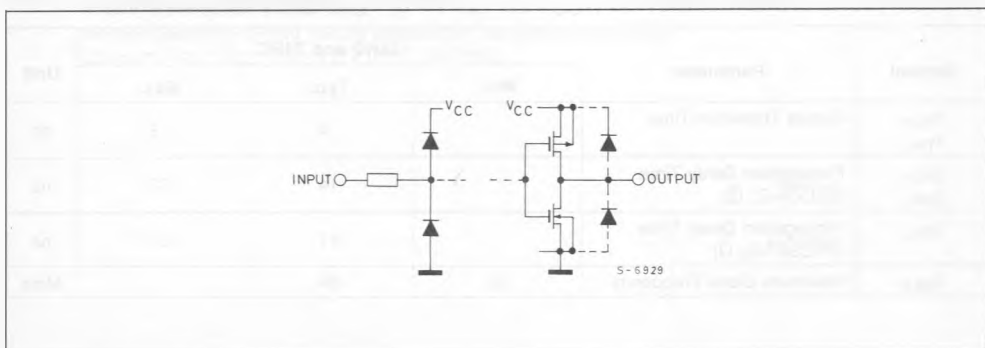
(*) 500 mW = 65° derate to 10 mW/°C from 65°C to 85°C for plastic package

(*) 500 mW = 65° derate to 12 mW/°C from 100 to 125°C for frit-seal package

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	2 to 6	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_A	Operating Temperature 74HC Series 54HC Series	- 40 to 85 - 55 to 125	°C
t_r, t_f	Input Rise and Fall Time	$V_{CC} \begin{cases} 2 \text{ V} & 0 \text{ to } 1000 \\ 4.5 \text{ V} & 0 \text{ to } 500 \\ 6 \text{ V} & 0 \text{ to } 400 \end{cases}$	ns

INPUT AND OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V _{CC}	Test Condition		T _A = 25°C 54HC and 74HC			– 40 to 85°C 74HC		– 55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V _{IH}	High Level Input Voltage	2.0 4.5 6.0			1.5 3.15 4.2	— — —	— — —	1.5 3.15 4.2	— — —	1.5 3.15 4.2	— — —	V
V _{IL}	Low Level Input Voltage	2.0 4.5 6.0			— — —	— — —	0.5 1.35 1.8	— 1.35 1.8	0.5 1.35 1.8	— 1.35 1.8	0.5 1.35 1.8	V
V _{OH}	High Level Output Voltage	2.0	V _I	I _O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V _{IH} or V _{IL}	– 20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5 6.0		– 4.0 mA – 5.2 mA	4.18 5.68	4.31 5.8	— —	4.13 5.63	— —	4.10 5.60	— —	
V _{OL}	Low Level Output Voltage	2.0	V _{IH} or V _{IL}	20 μA	—	0.0	0.1	—	0.1	—	0.1	V
		4.5			—	0.0	0.1	—	0.1	—	0.1	
		6.0			—	0.0	0.1	—	0.1	—	0.1	
		4.5 6.0			—	0.17 0.18	0.26 0.26	— —	0.33 0.33	— —	0.40 0.40	
I _I	Input Leakage Current	6.0	V _I = V _{CC} or GND		—	—	±0.1	—	±1.0	—	±1.0	μA
I _{CC}	Quiescent Supply Current	6.0	V _I = V _{CC} or GND		—	—	2	—	20	—	40	μA

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V, T_A = 25°C, C_L = 15pF, Input t_r = t_f = 6ns)

Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t _{TLH} t _{THL}	Output Transition Time		4	8	ns
t _{PLH} t _{PHL}	Propagation Delay Time (CLOCK-Q, $\bar{Q}$)		14	23	ns
t _{PHL}	Propagation Delay Time (PRESET-Q, $\bar{Q}$)		17	27	ns
f _{MAX}	Maximum Clock Frequency	35	64		MHz

AC ELECTRICAL CHARACTERISTICS ($C_L = 50\text{pF}$, Input $t_r = t_f = 6\text{ns}$)

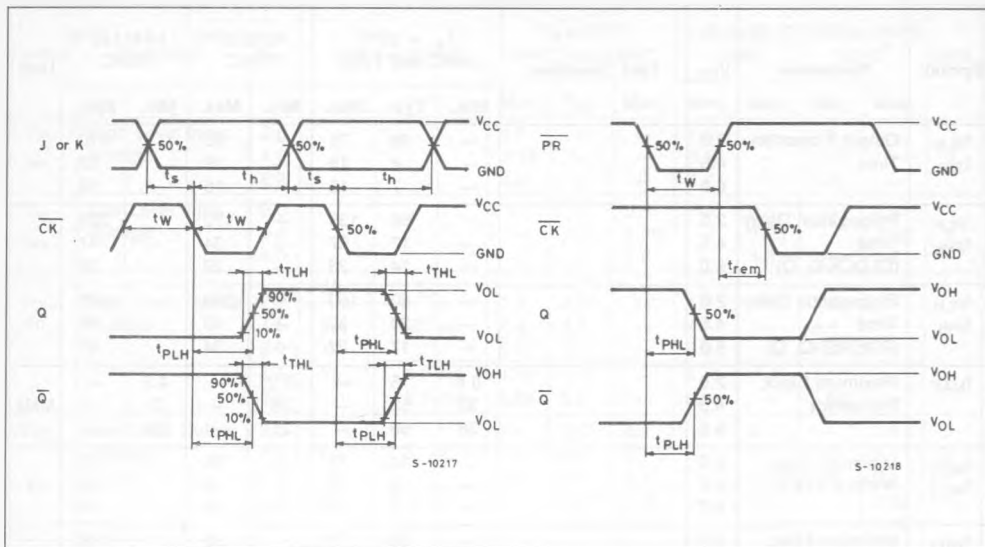
Symbol	Parameter	V_{CC}	Test Condition	$T_A = 25^\circ\text{C}$ 54HC and 74HC			-40 to 85°C 74HC		-55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0 4.5 6.0		— — —	30 8 7	75 15 13	— — —	95 19 16		110 22 19	ns
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK-Q, $\bar{Q}$)	2.0 4.5 6.0		— — —	68 17 14	135 27 23	— — —	170 34 29		205 41 35	ns
t_{PLH} t_{PHL}	Propagation Delay Time (PRESET-Q, $\bar{Q}$)	2.0 4.5 6.0		— — —	80 20 17	160 32 27	— — —	200 40 34		240 48 41	ns
f_{MAX}	Maximum Clock Frequency	2.0 4.5 6.0		6.4 32 38	15 58 68	— — —	5.2 26 31	— — —	4.2 21 25	— — —	MHz
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width (CLOCK)	2.0 4.5 6.0		— — —	30 8 7	75 15 13	— — —	95 19 16		110 22 19	ns
$t_{W(L)}$	Minimum Pulse Width PRESET	2.0 4.5 6.0		— — —	30 8 7	75 15 13	— — —	95 19 16		110 22 19	ns
t_s	Minimum Set-up Time J, K	2.0 4.5 6.0		— — —	25 5 4	75 15 13	— — —	95 19 16		110 22 19	ns
t_h	Minimum Hold Time J, K	2.0 4.5 6.0		— — —	— — —	0 0 0	— — —	0 0 0	— — —	0 0 0	ns
t_{REM}	Minimum Removal Time (PRESET)	2.0 4.5 6.0		— — —	0 0 0	0 0 0	— — —	0 0 0	— — —	0 0 0	ns
C_{IN}	Input Capacitance			—	5	10	—	10		10	pF
$C_{PD} (*)$	Power Dissipation Capacitance			—	38	—	—	—			pF

Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the following equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2 \text{ (for 1 Flip/Flop).}$$

SWITCHING CHARACTERISTICS TEST WAVEFORM

TEST CIRCUIT I_{CC} (Opr.)