MOS INTEGRATED CIRCUIT

M 5912

ADVANCE DATA

PCM TRANSMIT/RECEIVE FILTERS

- MONOLITHIC DEVICE INCLUDES BOTH TRANSMIT AND RECEIVE FILTERS
- CCITT G712 AND AT&T D3/D4 COMPATIBLE
- TRANSMIT FILTER INCLUDES 50/60 Hz REJECTION
- RECEIVE FILTER INCLUDES SIN X/X COMPENSATION
- EXTERNAL GAIN ADJUSTMENT, BOTH TRANSMIT AND RECEIVE FILTERS
- LOW POWER CONSUMPTION: 20 mW TYPICAL WITHOUT POWER AMPLIFIERS
  < 1 mW TYPICAL IN POWER-DOWN MODE
- DIRECT INTERFACE WITH TRANSFORMER OR ELECTRONIC TELEPHONE HYBRIDS
- ± 5% POWER SUPPLIES; +5V, -5V
- STANDARD 16-PIN PACKAGE
- PIN-FOR-PIN COMPATIBLE WITH THE 2912 PCM FILTER

The M5912 is a monolithic device containing the two filters of a PCM line or trunk termination and is designed to minimize power dissipation, maximize reliability and provide a low-cost alternative to hybrid filters. The device consists of two switched-capacitor filters, transmit and receive, and power amplifiers which may be used to drive a transformer hybrid (2-to-4 wire converter) or an electronic hybrid (SLIC). If an electronic hybrid is used, the power amplifiers are not needed and may be deactivated to minimize power dissipation. The transmit filter is a band-pass filter which will pass frequencies between 300 Hz and 3200 Hz and provides rejection of the 50/60 Hz power line frequency as well as the anti-aliasing needed in an 8 kHz sampling system. The receive filter is a low-pass filter which smooths the voltage steps present in the CODEC output waveform and provides the sin x/x correction necessary to give unity gain in the passband for the CODEC-decoder-and-receive-filter pair.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage with Respect to V_{BB}	-0.3 to +14.0	V
All Input and Output Voltages with Respect to V_{BB}	-0.3 to +14.0	V
All Output Currents	± 50	mA
Temperature Under Bias	-10 to +80	°C
Storage Temperature range	-65 to +150	°C
Package Dissipation at 25°C (Derated 9 mW/°C when soldered into PCB)	500	mW

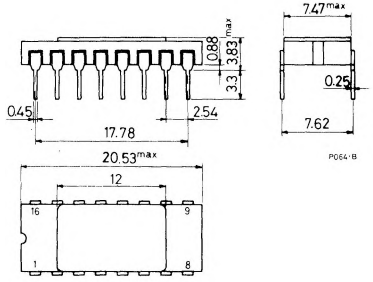
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING NUMBERS:

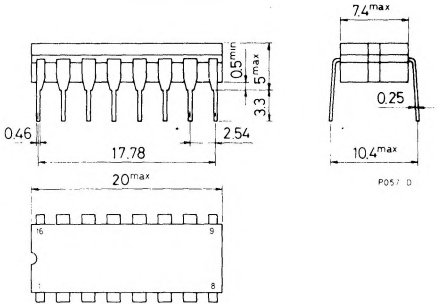
M5912 D1 for dual in-line ceramic package, metal seal
M5912 F1 for dual in-line ceramic package, frit seal

MECHANICAL DATA (dimensions in mm)

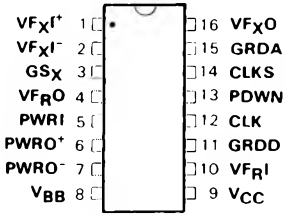
Dual in-line ceramic package metal-seal



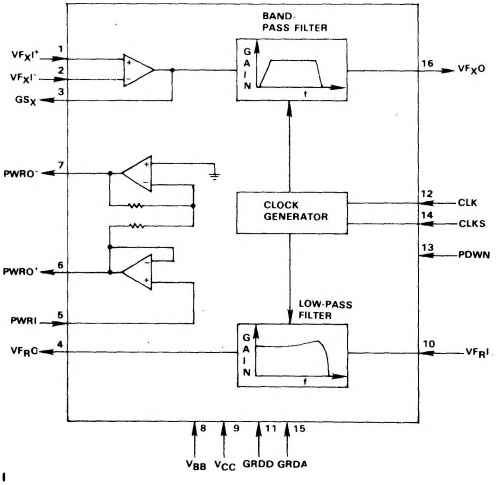
Dual in-line ceramic package frit-seal



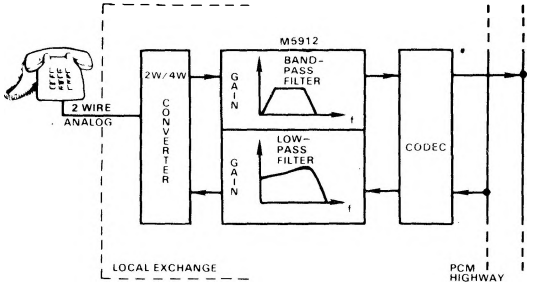
PIN CONNECTIONS



BLOCK DIAGRAM



TYPICAL LINE TERMINATION



POWER DISSIPATION

Parameter		Test conditions	Values			Unit
			Min.	Typ.	Max.	
I_{CC0}	V_{CC} Standby Current	PDWN = V_{IH} min			100	µA
I_{BB0}	V_{BB} Standby Current	PDWN = V_{IH} min			100	µA
I_{CC1}	V_{CC} Operating Current, Power Amplifiers Inactive	PWRI = V_{BB}			6	mA
I_{BB1}	V_{BB} Operating Current, Power Amplifiers Inactive	PWRI = V_{BB}			6	mA
I_{SCPA}	Short Circuit Output Current (Power Amplifier)	Either power amplifier to ground			20	mA

DC AND OPERATING CHARACTERISTICS (T_{amb}= 0°C to +70°C, V_{CC}= +5V ± 5%, V_{BB}= -5V ± 5%, GRDA= 0V, GRDD = 0V, unless otherwise specified)

DIGITAL INTERFACE

Parameter		Test conditions	Values			Unit
			Min.	Typ.	Max.	
I_{LIC}	Input Load Current	V_{IN} = V_{IL} min to V_{IH} max			10	µA
I_{LIO}	Input Load Current, CLKS	V_{IN} = V_{BB} to V_{IH} max			50	µA
I_{LIP}	Input Load Current, PDWN	V_{IN} = V_{IL} min to V_{IH} max			-40	µA
V_{IL}	Input Low Voltage (except CLKS)				0.8	V
V_{IH}	Input High Voltage (except CLKS)		2.2			V
V_{ILO}	Input Low Voltage, CLKS		V_{BB}		V_{BB}+0.5	V
V_{IIO}	Input Intermediate Voltage, CLKS		GRDD-0.5		0.2	V
V_{IHO}	Input High Voltage, CLKS		V_{CC}-0.5		V_{CC}	V

ANALOG INTERFACE, TRANSMIT FILTER GAIN SETTING AMPLIFIER

I_{BXI}	Input Leakage Current, VF_XI^+, VF_XI^-	-3.2V < V_{IN} < 3.2V			100	nA
R_{IXI}	Input Resistance, VF_XI^- VF_XI^+		10			MΩ
V_{OSXI}	Input Offset Voltage, VF_XI^+, VF_XI^-	-3.2V < V_{IN} < 3.2V			25	mV
$PSRR_1$	Power Supply Rejection, GS_X		60			dB

DC AND OPERATING CHARACTERISTICS (continued)

ANALOG INTERFACE, TRANSMIT FILTER GAIN SETTING AMPLIFIER

Parameter		Test conditions	Values			Unit
			Min.	Typ.	Max.	
CMRR	Common Mode Rejection, VF_XI^+, VF_XI^-	$-3.2V < V_{IN} < 3.2V$	60			dB
A_{VOL}	DC Open Loop Voltage Gain, GS_X		2000			
f_C	Open Loop Unity Gain Bandwidth, GS_X			2		MHz
V_{OXI}	Output Voltage Swing, GS_X	$R_L \geq 10\ k\Omega$	± 2.5			V
C_{LXI}	Load Capacitance, GS_X				20	pF
R_{LXI}	Minimum Load Resistance, GS_X	Minimum R_L	10			kΩ

ANALOG INTERFACE, TRANSMIT FILTER

R_{OX}	Output Resistance, VF_XO				100	Ω
V_{OSX}	Output DC Offset, VF_XO	VF_XI^+ Connected to GRDA, Input Op amp at Unity Gain			200	mV
$PSRR_2$	Power Supply Rejection of V_{CC} at 1 kHz, VF_XO		35	40		dB
$PSRR_3$	Power Supply Rejection of V_{BB} at 1 kHz, VF_XO		25	30		dB
C_{LX}	Load Capacitance, VF_XO				20	pF
R_{LX}	Minimum Load Resistance, VF_XO	Minimum R_L	3			kΩ
V_{OX}	Output Voltage Swing, 1 kHz, VF_XO	$R_L \geq 10\ k\Omega$		± 3.2		V
		$R_L \geq 3\ k\Omega$	± 2.5			

ANALOG INTERFACE, RECEIVE FILTER

I_{BR}	Input Leakage Current, VF_RI	$-3.2V < V_{IN} < 3.2V$			1	μA
RIR	Input Resistance, VF_RI		2			MΩ
R_{OR}	Output Resistance, VF_RO				100	Ω
V_{OSR}	Output DC Offset, VF_RO	VF_RI Connected to GRDA			200	mV
$PSRR_4$	Power Supply Rejection of V_{CC} at 1 kHz, VF_RO		30	35		dB
$PSRR_5$	Power Supply Rejection of V_{BB} at 1 kHz, VF_RO		30	35		dB
C_{LR}	Load Capacitance, VF_RO				20	pF
R_{LR}	Minimum Load Resistance, VF_RO	Minimum R_L	10			kΩ
V_{OR}	Output Voltage Swing, VF_RO	$R_L = 10\ k\Omega$	± 3.2			V

DC AND OPERATION CHARACTERISTICS (continued)

ANALOG INTERFACE, RECEIVE FILTER DRIVER AMPLIFIER STAGE

Parameter		Test conditions	Values			Unit
			Min.	Typ.	Max.	
I_{BRA}	Input Leakage Current, PWRI	$-3.2C < V_{IN} < 3.2V$			3	µA
R_{IRA}	Input Resistance, PWRI		10			MΩ
R_{ORA}	Output Resistance, PWRO+, PWRO−	$\|I_{OUT}\| < 10$ mA $-3.2V < V_{OUT} < 3.2V$			1	Ω
V_{OSRA}	Output DC offset, PWRO+, PWRO−	PWRI Connected to GRDA			50	mV
C_{LRA}	Lead Capacitance, PWRO+, PWRO−				100	pF
V_{ORA1}	Output Voltages Swing Across R_L, PWRO+, PWRO− Single Ended Connection	$R_L \geq 300\Omega$ R_L Connected to GRDA	± 3.2			V
V_{ORA2}	Output Voltage Swing, PWRO+, PWRO− Balanced Output Connection	$R_L \geq 600\Omega$ R_L Connected between PWRO+ and PWRO−	± 6.4			V

AC CHARACTERISTICS (T_{amb} = 0°C to +70°C, V_{CC} = +5V ± 5%, V_{BB} = -5V ± 5%, GRDA = 0V, GRDD = 0V, unless otherwise specified).

Clock Input Frequency: CLK = 1.536 MHz ± 0.1%, CLKS = V_{ILO} (Tied to V_{BB})
CLK = 1.544 MHz ± 0.1%, CLKS = V_{IIO} (Tied to GRDD)
CLK = 2.048 MHz ± 0.1%, CLKS = V_{IHO} (Tied to V_{CC})
CLK = 2.560 MHz ± 0.1%, CLKS = Open Circuit

TRANSMIT FILTER TRANSFER CHARACTERISTICS

Parameter		Test conditions	Values			Unit
			Min.	Typ.	Max.	
G_{RX}	Gain Relative to Gain at 1 kHz	OdBmO Input Signal Gain Setting Op Amp at Unit Gain				
	Below 50 Hz					dB
	50 Hz				-35	dB
	60 Hz		-26		-30	dB
	200 Hz	OdBmO Signal = 1.2 V_{RMS}, Input at VF_XI^-	-1.8		-0.125	dB
	300 Hz to 3000 Hz		-0.125		+0.125	dB
	3300 Hz		-0.65		0.03	dB
	3400 Hz	Output at VF_XO is ≈ 1.73 V_{RMS}	-1.4		-0.1	dB
	4000 Hz				-14.5	dB
	4600 Hz and Above				-33	dB

AC CHARACTERISTICS (continued)

TRANSMIT FILTER TRANSFER CHARACTERISTICS

Parameter		Test conditions	Values			Unit
			Min.	Typ.	Max.	
G_{AX}	Absolute Passband Gain at 1 kHz, VF_XO		2.9	3.0	3.1	dB
G_{AXT}	Gain Variation with Temperature at 1 kHz	OdBmO Signal Level		0.0005		dB/°C
G_{AXS}	Gain Variation with Supplies at 1 kHz	OdBmO Signal Level, Supplies ± 5%		0.05		dB/V
CT_{RT}	Cross Talk, Receive to Transmit, Measured at VF_XO	VF_RI = 1.2 V_{RMS}, 1 kHz Input VF_XI^+, VF_XI^- Connected to GS_X, GS_X Connected through 10 kΩ to GRDA			-60	dB
N_{CX1}	Total C Message Noise at Output, VF_XO	Gain Setting Op Amp at Unity Gain		6		dBrncO
N_{CX2}	Total C Message Noise at Output, VF_XO	Gain Setting Op Amp at 20 dB Gain		10		dBrncO
D_{DX}	Differential Envelope Delay, VF_XO 1 kHz to 2.6 kHz				40	µs
D_{AX}	Absolute Delay at 1 kHz, VF_XO				195	µs
DP_{X1}	Single Frequency Distortion Products	OdBm Input Signal at 1 kHz			-50	dB
DP_{X2}	Single Frequency Distortion Products at Maximum Signal Level of +3 dBmO at VF_XO	Gain Setting Op Amp at 20 dB Gain. The +3 dBmO signal at VF_XO is 1.73 V_{RMS}			-45	dB

AC CHARACTERISTICS (T_{amb} = 0°C to +70°C, V_{CC} = +5V ± 5%, V_{BB} = -5V ± 5%, GRDA = 0V, GRDD = 0V, unless otherwise specified).

Clock Input Frequency:
CLK = 1.536 MHz ± 0.1%, CLKS = V_{ILO} (Tied to V_{BB})
CLK = 1.544 MHz ± 0.1%, CLKS = V_{IIO} (Tied to GRDD)
CLK = 2.048 MHz ± 0.1%, CLKS = V_{IHO} (Tied to V_{CC})
CLK = 2.560 MHz ± 0.1%, CLKS = Open Circuit

RECEIVE FILTER TRANSFER CHARACTERISTICS

Parameter		Test conditions	Values			Unit
			Min.	Typ.	Max.	
G_{RR}	Gain Relative to Gain at 1 kHz with sinx/x Correction	OdBmO Input Signal				
	Below 200 Hz	OdBmO Signal ≅ 1.2 V_{RMS}X			0.125	dB
	200 Hz		-0.125		0.125	dB
	300 Hz to 3000 Hz	$\left(\text{Sin}\frac{\pi f}{(8000)} / \frac{\pi f}{(8000)}\right)$, Input at VF_RI	-0.125		0.125	dB
	3300 Hz		-0.65		0.03	dB
	3400 Hz		-1.4		-0.1	dB

AC CHARACTERISTICS (continued)

RECEIVE FILTER TRANSFER CHARACTERISTICS

Parameter		Test conditions	Values			Unit
			Min.	Typ.	Max.	
G_{RR}	4000 Hz				-14.5	dB
	4600 Hz and Above				-32	dB
G_{AR}	Absolute Passband Gain at 1 kHz, VF_RO		-0.1	0	+0.1	dB
G_{ART}	Gain Variation with Temperature at 1 kHz	0dBmO Signal Level		0.0005		dB/°C
G_{ARS}	Gain Variation with Supplies at 1 kHz	0dBmO Signal Level, Supplies ± 5%		0.05		dB/V
CT_{TR}	Cross Talk, Transmit to Receive, Measured at VF_RO	VF_XO = 1.73 V_{RMS}, 1 kHz Output. VF_RI Connected to GRDA			-60	dB
N_{CR}	Total C Message Noise at Output, VF_RO	VF_RO Output or $PWRO^+$ and $PWRO^-$ Connected with Unity Gain		6		dBrnc0
D_{DR}	Differential Envelope Delay, VF_RO, 1 kHz to 2.6 kHz				120	µs
D_{AR}	Absolute Delay at 1 kHz, VF_RO				125	µs
DP_{R1}	Single Frequency Distortion Products	0dBm Input Signal at 1 kHz			-50	dB
DP_{R2}	Single Frequency Distortion Products at Maximum Signal Level of +3 dBmO at VF_RO	+3 dBmO Signal Level of 1.73 V_{RMS}, 1 kHz Input at VF_RO			-45	dB

FUNCTIONAL DESCRIPTION

Pin 1 – VF_XI^+

Pin 1 is the non-inverting input of the gain adjustment op amp in the transmit filter seciton. The signal applied to this pin typically comes from the transmit leg of a 2-to-4 wire hybrid. This input may be AC or DC coupled. This signal passes through the op amp to the transmit (band-pass) switched-capacitor filter which will pass frequencies between 300 and 3200 Hz, provide rejection of the 50/60 Hz power line frequency and provide antialiasing for an 8 kHz sampling system. This filter exceeds AT&T D3 and D4 specifications and is compatible with the CCITT G712 recommendations. Its specifications meet the digital class 5 central office switching systems requirements. The transmit filter transfer characteristics and specifications are shown in Figure 1.

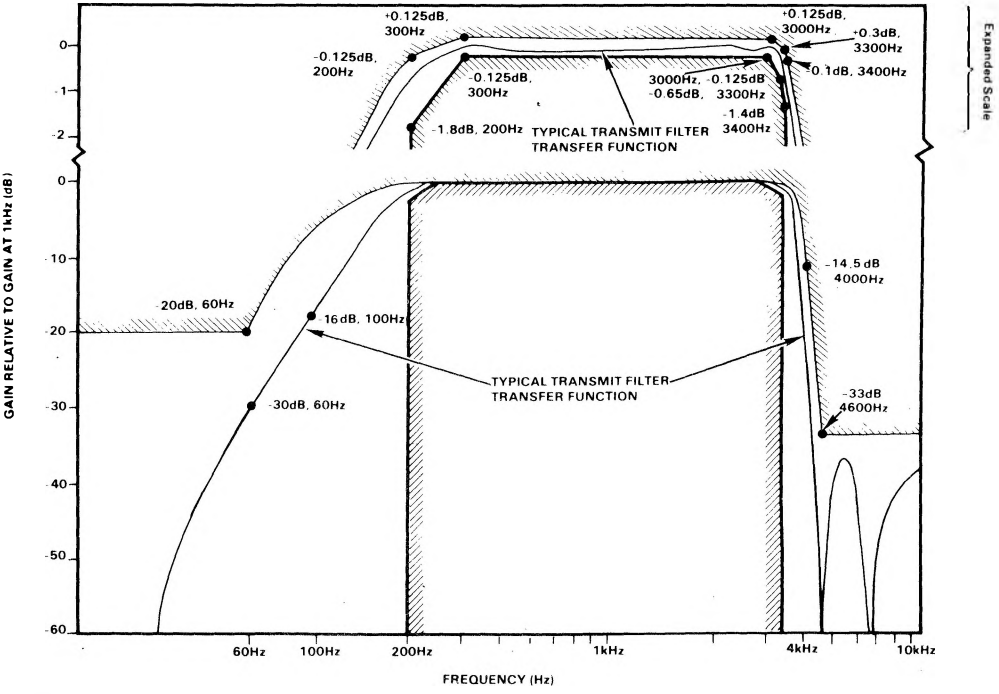
Pin 2 – VF_XI^-

Pin 2 is the inverting input of the gain adjustment op amp on the transmit filter. A return path for the op-amp output is provided by GS_X, Pin 3. Pins 2 and 3 may be used to provide gain up to 20 dB without degrading the noise performance of the filters.

This op amp has a common mode range of ± 2.5V, low DC offset (2.5 mV typ.) and can provide a voltage gain greater than 2000. The unity gain bandwidth is approximately 2 MHz. The transmit filter, excluding the input op amp, provides a gain of +3 dB in the passband.

FUNCTIONAL DESCRIPTION (continued)

Fig. 1 - Transmit filter transfer characteristics



Pin 3 – GS_X

Pin 3 is connected to the output of the gain-adjustment op amp in the transmit filter section. For proper operation, the load impedance connected to the GS_X output should be greater than 10 KΩ in parallel with 20 pF (Refer to Figure 2).

Pin 4 – VF_RO

Pin 4 is the output of the receive (low-pass) filter and is capable of driving high impedance electronic hybrids. The gain of the receive signal may be attenuated by using a resistor divider as shown in Figure 2. The resistive load connected to VF_RO should be greater than 10 KΩ.
If the receive filter is to drive a transformer hybrid, VF_RO should be connected to PWRI (Pin 5) as shown in Figure 3.

Pin 5 – PWRI

Pin 5 provides the input to the power driver amplifiers which interface the receive filter to a transformer hybrid. PWRI is a high impedance input which can be driven by VF_RO directly. The input voltage range is ± 3.2V and the gain for a bridged output is 6 dB. The power amplifiers may be deactivated when not being utilized by tying PWRI to V_{BB}.

FUNCTIONAL DESCRIPTION (continued)

Fig. 2 - Transmit and receive gain adjustment

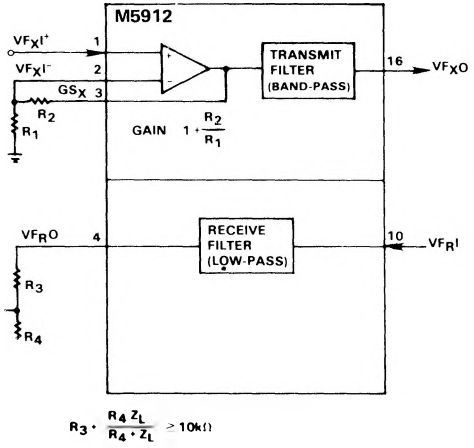
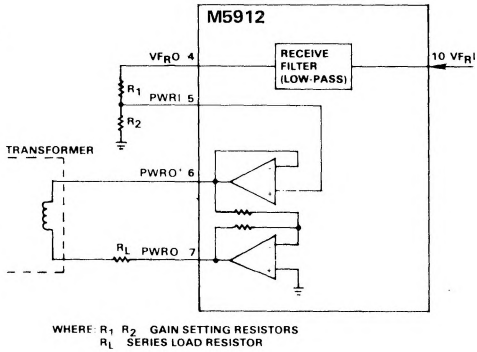


Fig. 3 - Typical connection of the output power amplifier stage



nd 7 — PWRO+ and PWRO−

nced differential-output amplifier stage is provided to drive low impedance loads directly. The ıe receive signal may be adjusted by a voltage divider as shown in Figure 3. The series impedance d resistor and the bybrid transformer should present an AC load resistance of 600Ω (min.) to ..ıe amplifiers in a bridged configuration. With a 600Ω load between pins 6 and 7, the maximum voltage swing across the loads is ±6.4 volts. These may also be used to drive loads which are connected to ground. If the power amplifiers are not required in a particular application they should be deactivated by typing PWRI to V_{BB}.

Pin 8 — V_{BB}

Pin 8 is the negative supply pin. The voltage supplied to this pin should be -5V ± 5%.

Pin 9 — V_{CC}

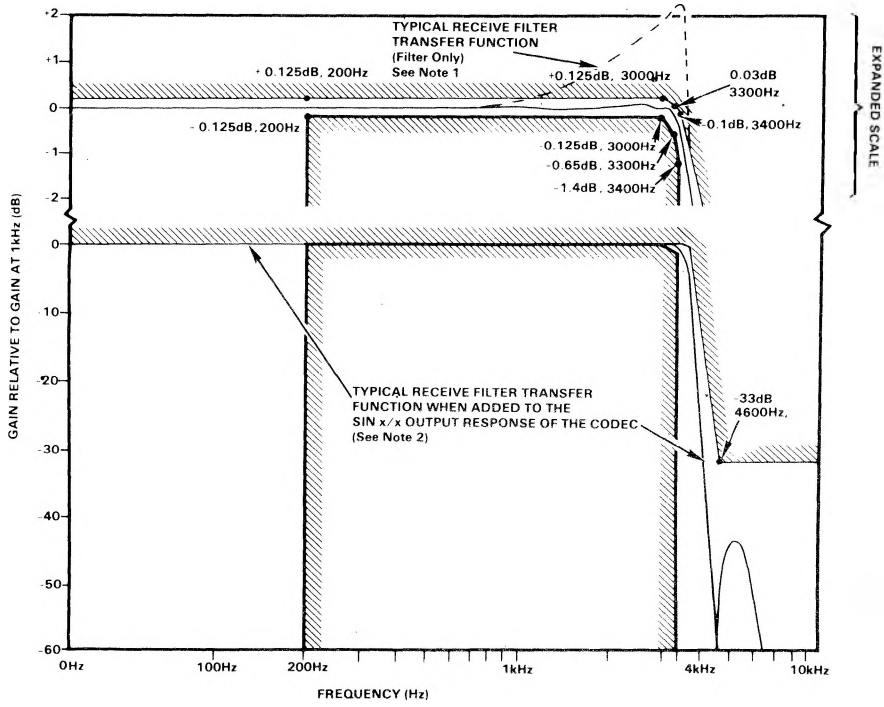
Pin 9 is the positive supply pin. The voltage supplied to this pin should be +5V ± 5%.

Pin 10 — VF_{RI}

Pin 10 is the analog input to the receive filter. The receive signal is typically generated by the decoder section of a μ or A law companding Codec. The receive filter is a low-pass switched-capacitor filter which will pass frequencies up to 3200 Hz and provides the sin x/x correction needed to give the Codec decoder and receive filter pair unity gain over the passband. This filter exceeds the AT&T D3/D4 specifications and is compatible with the CCITT G712 recommendation.
The receive filter transfer characteristics and specifications, including the sinx/x response introduced by the decoder, are shown in Figure 4.

FUNCTIONAL DESCRIPTION (continued)

Fig. 4 - Receive filter transfer characteristics



NOTES:

1. The broken line shows the x/sinx response of the filter only. This response corrects the sinx/x response of the sample and hold output of the codec and provides unity gain in the passband.
2. The Typical filter transfer function shown is the combined response of the codec and the receive filter. The combined response meets the stated specifications.

Pin 11 – GRDD

Pin 11 serves as the digital ground return for the internal clock. The digital ground is not internally connected to the analog ground. The digital and analog grounds should be tied together as close as practical to the system supply ground.

Pin 12 – CLK

The digital clock signal should be supplied to Pin 12. Four clock frequencies (1.536 MHz, 1.544 MHz, 2.048 MHz, or 2.560 MHz) may be used. The desired clock frequency is selected by the CLKS input (Refer to Table 1). For proper operation this clock should be tied to the receive clock of the Codec.

Pin 13 – PDWN

This control input is used to place the M5912 in the standby power-down mode. Power down occurs when the signal on this input is pulled high. Standard TTL levels may be used. An internal pull up to the positive supply is provided. A settling time of 15 ms (typ) should be allowed after power is restored.

Pin 14 – CLKS

The voltage level on this pin will select the desired clock frequency to drive Pin 12. Table 1 defines the clock selection. When using the open circuit (2.560 MHz clock frequency) mode, the capacitance to adjacent signal lines should be minimized.

Table 1 – Input Clock Select

CODEC Clock	Clock Bits/ Frame	M5912 CLK Input Pin 12	M5912 CLKS Input Pin 14
1.536 MHz	192	1.536 MHz	V_{BB}, -5V
1.544 MHz	193	1.544 MHz	GRDD
2.048 MHz	256	2.046 MHz	V_{CC}, +5V
2.560 MHz	320	2.560 MHz	Open Circuit

Pin 15 – GRDA

Pin 15 serves as the ground return for the analog circuits of the transmit and receive sections. The analog ground is not internally connected to the digital ground. The digital and analog ground should be tied together as close as practical to the system supply ground.

Pin 16 – VF_XO

Pin 16 is the analog output of the transmit filter. The output voltage range is ± 3.2 volts and the DC offset is less than 200 mV. This output should be AC coupled to the transmit (encoder) section of the Codec.

DECOUPLING RECOMMENDATIONS

PC board decoupling should be sufficient to prevent power supply transients (including turn on and turn on and turn off) from exceeding the absolute maximum rating of the device. A minimum of 1 μF is recommended for each power supply.
A 0.05 μF bypassing capacitor should also be connected from each power supply to GRDA at the M5912 device. However, this decoupling may be reduced depending on board design and performance.