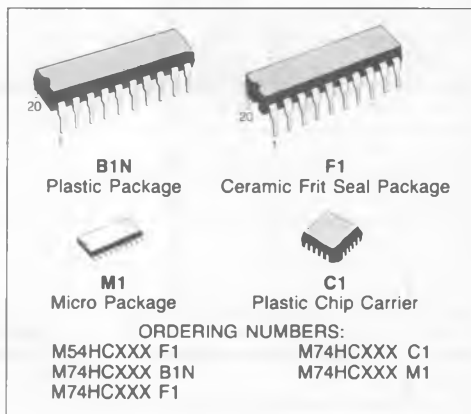


HC698 U/D DECADE COUNTER/REGISTER (3-STATE) HC699 U/D 4-BIT BINARY COUNTER/REGISTER (3-STATE)

- **HIGH SPEED**
 $f_{MAX} = 33\text{MHz (TYP.) at } V_{CC} = 5\text{V}$
- **LOW POWER DISSIPATION**
 $I_{CC} = 4\text{ }\mu\text{A (MAX.) at } T_A = 25^\circ\text{C}$
- **HIGH NOISE IMMUNITY**
 $V_{NIH} = V_{NIL} = 28\% V_{CC} \text{ (MIN.)}$
- **OUTPUT DRIVE CAPABILITY**
 15 LSTTL LOADS (FOR Q_A to Q_D)
 10 LSTTL LOADS (FOR RCO)
- **SYMMETRICAL OUTPUT IMPEDANCE**
 $|I_{OH}| = I_{OL} = 6\text{ mA (MIN.) FOR } Q_A \text{ to } Q_D$
OUTPUT
 $|I_{OH}| = I_{OL} = 4\text{ mA (MIN.) FOR RCO OUTPUT}$
- **BALANCED PROPAGATION DELAYS**
 $t_{PLH} = t_{PHL}$
- **WIDE OPERATING VOLTAGE RANGE**
 $V_{CC(OPR)} = 2\text{V to } 6\text{V}$
- **PIN AND FUNCTION COMPATIBLE WITH LSTTL 54/74LS698/699**

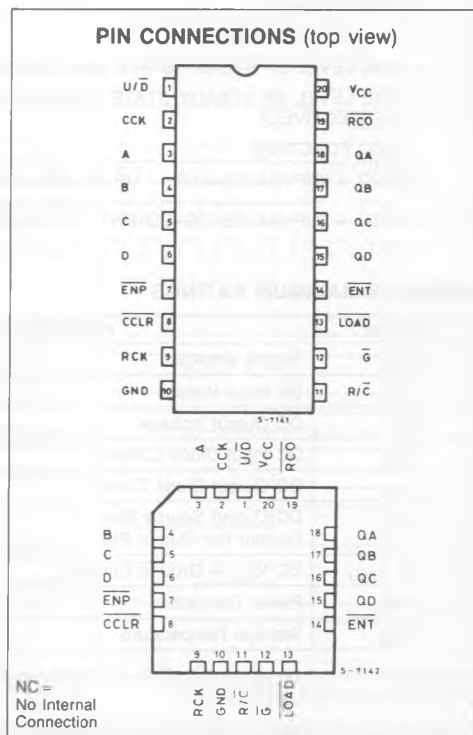


DESCRIPTION

The HC698/699 are high speed CMOS 4-BIT BINARY/DECADE COUNTER/REGISTER 3-STATE fabricated in silicon gate CMOS technology.

It has the same high speed performance of LSTTL combined with true CMOS low power consumption. These devices incorporate a synchronous up/down counter, a four-bit D-type register, and quadruple two-line to one-line multiplexers with three-state outputs in a single 20-pin package. The up/down counter is programmable from the data inputs and features enable P and enable T and a ripple-carry output for easy expansion. The register/counter select input, R/C, selects the counter when low or the register when high for the three-state outputs, Q_A , Q_B , Q_C , and Q_D .

Both the counter clock CCK and register clock RCK are positive-edge triggered. The counter clear CCLR is active low and is synchronous. All inputs are equipped with protection circuits against static discharge and transient excess voltage.



TRUTH TABLE

INPUTS									OUTPUTS				FUNCTION
CCLR	LOAD	ENP	ENT	CCK	U/D	RCK	R/C	G	QA	QB	QC	QD	
X	X	X	X	X	X	X	X	H	Z	Z	Z	Z	HIGH IMPEDANCE
L	X	X	X		X	X	L	L	L	L	L	L	CLEAR COUNTER
H	L	X	X		X	X	L	L	a	b	c	d	LOAD COUNTER
H	H	H	X		X	X	L	L	NO CHANGE				NO COUNT
H	H	X	H		X	X	L	L	NO CHANGE				NO COUNT
H	H	L	L		H	X	L	L	COUNT UP				COUNT UP
H	H	L	L		L	X	L	L	COUNT DOWN				COUNT DOWN
X	X	X	X		X	X	L	L	NO CHANGE				NO COUNT
X	X	X	X	X	X		H	L	a'	b'	c'	d'	LOAD REGISTER
X	X	X	X	X	X		H	L	NO CHANGE				NO LOAD

X : DON'T CARE

Z : HIGH IMPEDANCE

a-d : THE LEVEL OF STEADY STATE INPUT AT INPUTS A THROUGH D RESPECTIVELY.

a'-d' : THE LEVEL OF STEADY STATE OUTPUTS AT INTERNAL COUNTER OUTPUTS QA' THROUGH QD' RESPECTIVELY.

RCO FUNCTION:

$$\overline{\text{RCO}} = (\text{UP} \cdot \text{QA} \cdot \text{QD} \cdot \text{ENT} + \overline{\text{UP}} \cdot \overline{\text{QA}} \cdot \overline{\text{QB}} \cdot \overline{\text{QC}} \cdot \overline{\text{QD}} \cdot \text{ENT}) \text{ (HC698)}$$

$$\overline{\text{RCO}} = (\text{UP} \cdot \text{QA} \cdot \text{QB} \cdot \text{QC} \cdot \text{QD} \cdot \text{ENT} + \overline{\text{UP}} \cdot \overline{\text{QA}} \cdot \overline{\text{QB}} \cdot \overline{\text{QC}} \cdot \overline{\text{QD}} \cdot \text{ENT}) \text{ (HC699)}$$

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{CC}	Supply Voltage	- 0.5 to 7	V
V _I	DC Input Voltage	- 0.5 to V _{CC} + 0.5	V
V _O	DC Output Voltage	- 0.5 to V _{CC} + 0.5	V
I _{IK}	DC Input Diode Current	± 20	mA
I _{OK}	DC Output Diode Current	± 20	mA
I _O	DC Output Source Sink Current Per Output Pin (RCO) (QA to QD)	± 20 ± 35	mA
I _{CC} or I _{GND}	DC V _{CC} or Ground Current	± 70	mA
P _D	Power Dissipation	500 (*)	mW
T _{stg}	Storage Temperature	- 65 to 150	°C

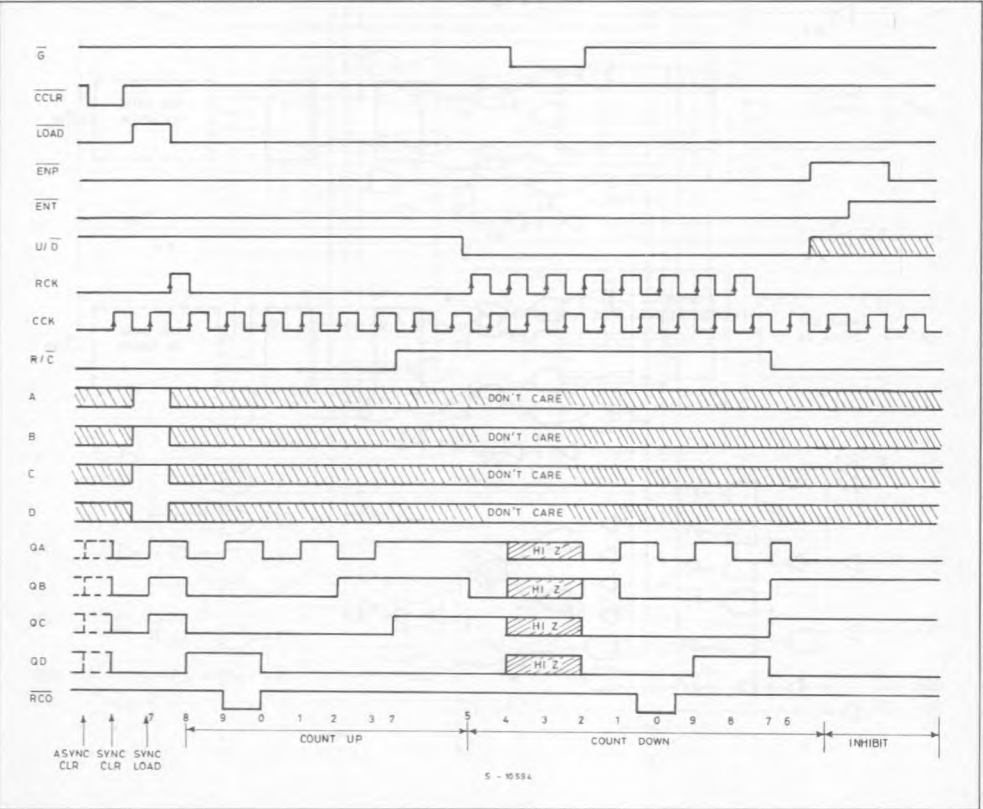
Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≡ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

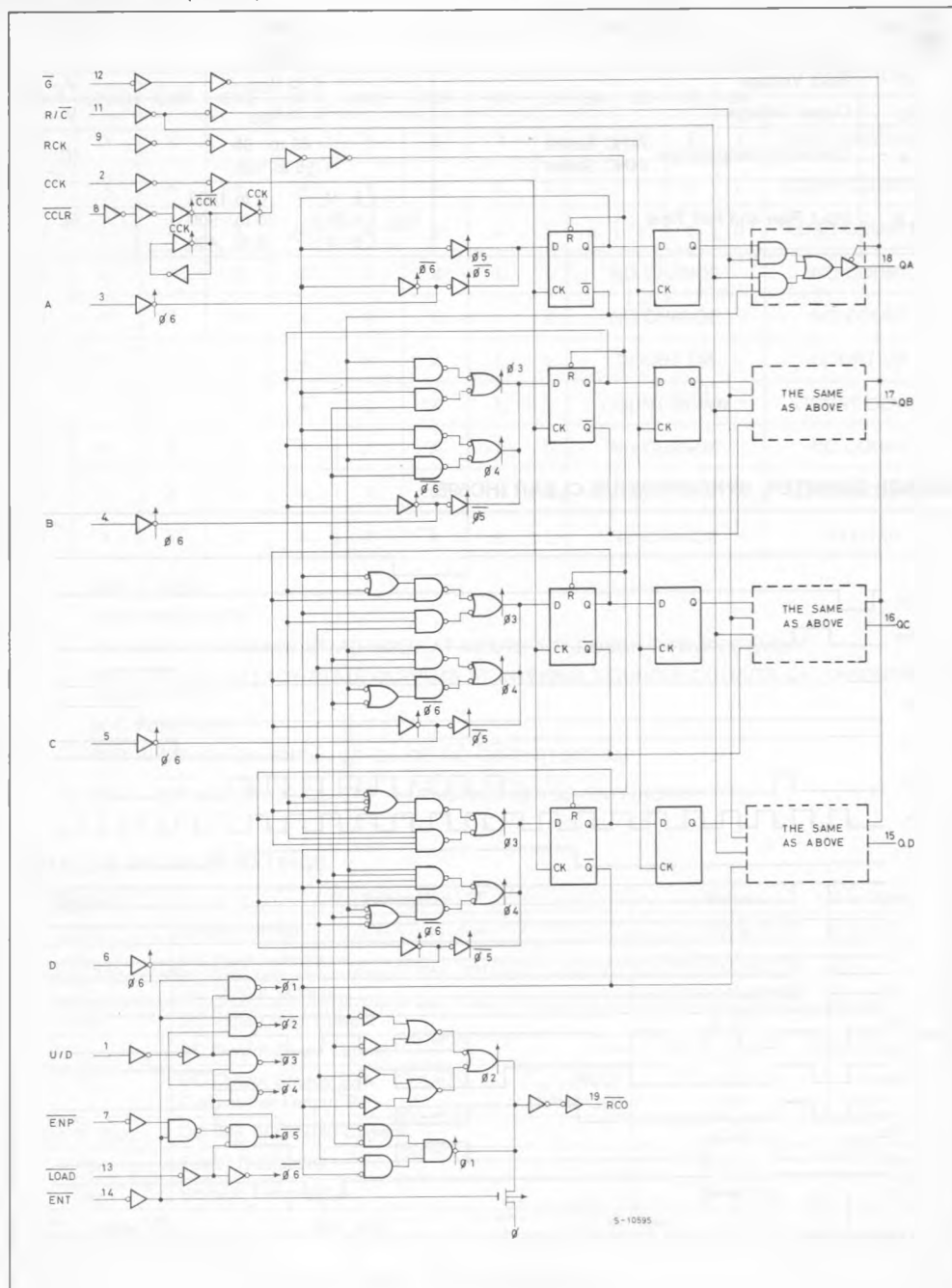
RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	2 to 6	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_A	Operating Temperature	74HC Series 54HC Series - 40 to 85 - 55 to 125	°C
t_r, t_f	Input Rise and Fall Time	$V_{CC} \begin{cases} 2 \text{ V} & 0 \text{ to } 1000 \\ 4.5 \text{ V} & 0 \text{ to } 500 \\ 6 \text{ V} & 0 \text{ to } 400 \end{cases}$	ns

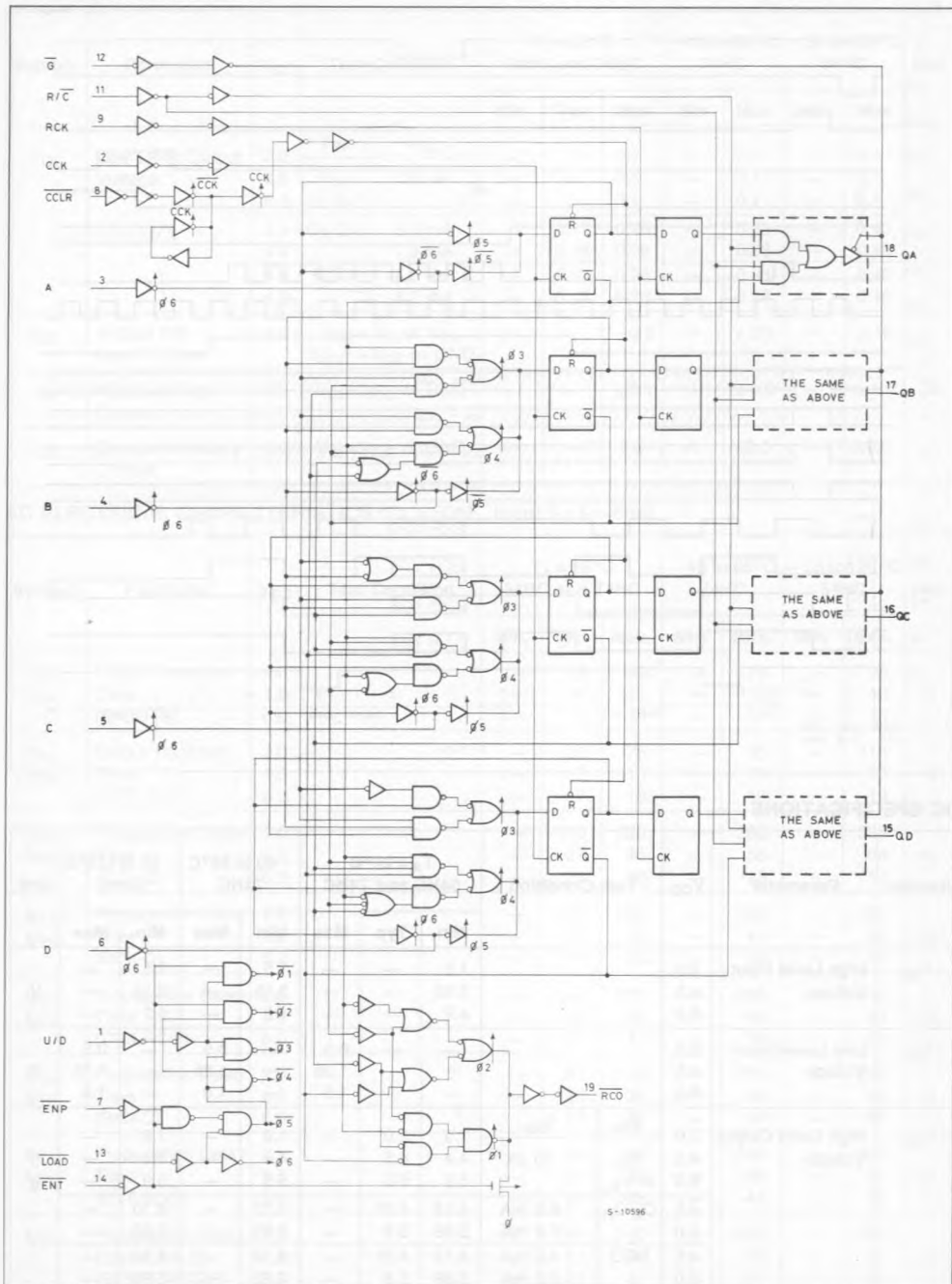
DECADE COUNTER, SYNCHRONOUS CLEAR (HC698)



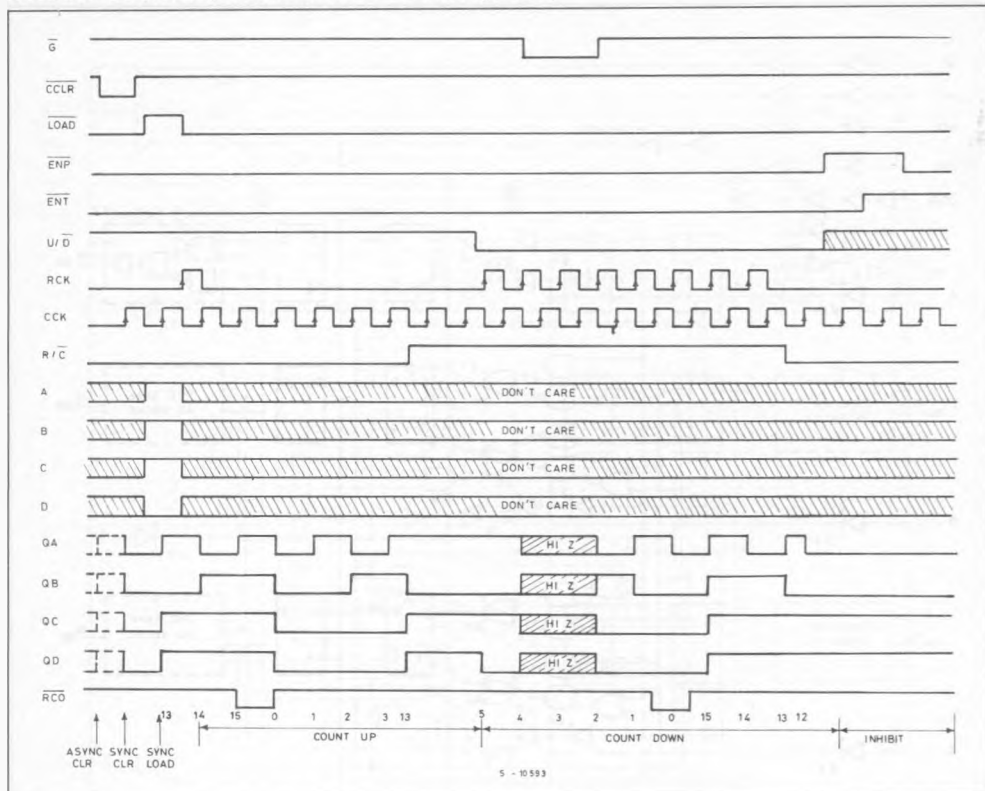
LOGIC DIAGRAM (HC698)



LOGIC DIAGRAM (HC699)



BYNARY COUNTER, SYNCHRONOUS CLEAR (HC699)



DC SPECIFICATIONS

Symbol	Parameter	V _{CC}	Test Condition	T _A = 25°C 54HC and 74HC			- 40 to 85°C 74HC		- 55 to 125°C 54HC		Unit
				Min	Typ	Max	Min	Max	Min	Max	
V _{IH}	High Level Input Voltage	2.0 4.5 6.0		1.5 3.15 4.2	— — —	— — —	1.5 3.15 4.2	— — —	1.5 3.15 4.2	— — —	V
V _{IL}	Low Level Input Voltage	2.0 4.5 6.0		— — —	— — —	0.5 1.35 1.8	— 1.35 1.8	0.5 1.35 1.8	— — —	0.5 1.35 1.8	V
V _{OH}	High Level Output Voltage	2.0	V _{IN}	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V _{IH}	4.4	4.5	—	4.4	—	4.4	—	
		6.0	V _{IH} or V _{IL}	5.9	6.0	—	5.9	—	5.9	—	
		4.5	Q _A -Q _H	4.18	4.31	—	4.13	—	4.10	—	
		6.0		5.68	5.8	—	5.63	—	5.60	—	
		4.5	RCO	4.18	4.31	—	4.13	—	4.10	—	
		6.0		5.68	5.8	—	5.63	—	5.60	—	

DC SPECIFICATIONS (Continued)

Symbol	Parameter	V _{CC}	Test Condition	T _A = 25°C 54HC and 74HC			– 40 to 85°C 74HC		– 55 to 125°C 54HC		Unit
				Min	Typ	Max	Min	Max	Min	Max	
V _{OL}	Low Level Output Voltage	2.0	V _{IN}	—	0	0.1	—	0.1	—	0.1	V
		4.5	V _{IH}	—	0	0.1	—	0.1	—	0.1	
		6.0	or V _{IL}	—	0	0.1	—	0.1	—	0.1	
		4.5	Q _A -Q _H	—	0.17	0.26	—	0.33	—	0.40	
		6.0		—	0.18	0.26	—	0.33	—	0.40	
		4.5	RCO	—	0.17	0.26	—	0.33	—	0.40	
		6.0		—	0.18	0.26	—	0.33	—	0.40	
I _{OZ}	3-State Off Leak Current	6.0	V _{IN} = V _{IL} or V _{IH} V _{OUT} = V _{CC} or GND	—	—	±0.5	—	±0.5	—	±10	μA
I _{IN}	Input Leakage Current	6.0	V _{IN} = V _{CC} or GND	—	—	±0.1	—	±1.0	—	±1.0	
I _{CC}	Quiescent Supply Current	6.0	V _{IN} = V _{CC} or GND	—	—	4.0	—	40.0	—	80.0	

AC ELECTRICAL CHARACTERISTICS (C_L = 50pF, Input t_r = t_f = 6ns)

Symbol	Parameter	V _{CC}	Test Condition	T _A = 25°C 54HC and 74HC			– 40 to 85°C 74HC		– 55 to 125°C 54HC		Unit
				Min	Typ	Max	Min	Max	Min	Max	
t _{TLH} t _{THL}	Output Transition Time (Q OUTS)	2.0		—	25	60	—	75	—	90	ns
		4.5		—	7	12	—	15	—	18	
		6.0		—	6	10	—	13	—	15	
t _{TLH} t _{THL}	Output Transition Time (RCO OUT)	2.0		—	30	75	—	95	—	113	ns
		4.5		—	8	15	—	19	—	23	
		6.0		—	7	13	—	16	—	19	
t _{PLH} t _{PHL}	Propagation Delay Time (CCK-Q)	2.0		—	116	225	—	280	—	338	ns
		4.5		—	29	45	—	56	—	68	
		6.0		—	25	38	—	48	—	57	
t _{PLH} t _{PHL}	Propagation Delay Time (RCK-Q)	2.0		—	100	195	—	245	—	293	ns
		4.5		—	25	39	—	49	—	59	
		6.0		—	21	33	—	42	—	50	
t _{PLH} t _{PHL}	Propagation Delay Time (CCK-RCO)	2.0		—	144	275	—	345	—	413	ns
		4.5		—	36	55	—	69	—	83	
		6.0		—	31	47	—	59	—	70	
t _{PLH} t _{PHL}	Propagation Delay Time (R/C/-Q)	2.0		—	92	175	—	220	—	263	ns
		4.5		—	23	35	—	44	—	53	
		6.0		—	20	30	—	37	—	45	
t _{PLH} t _{PHL}	Propagation Delay Time (ENT-RCO)	2.0		—	96	190	—	240	—	285	ns
		4.5		—	24	38	—	48	—	57	
		6.0		—	20	32	—	41	—	48	
t _{PHL}	Propagation Delay Time (CCK-Q) [RESET MODE]	2.0		—	124	240	—	300	—	360	ns
		4.5		—	31	48	—	60	—	72	
		6.0		—	26	41	—	51	—	61	

AC ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Parameter	V _{CC}	Test Condition	T _A = 25°C 54HC and 74HC			- 40 to 85°C 74HC		- 55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
f _{MAX}	Maximum Clock Frequency (CCK & RCK)	2.0 4.5 6.0		3.5 18 21	7 28 33	—	2.8 14 16	—	2.4 12 14	—	MHz
t _{W(L)} t _{W(H)}	Minimum Pulse Width (CCK-RCK)	2.0 4.5 6.0		— — —	44 11 9	100 20 17	— — —	125 25 21	— — —	150 30 26	ns
t _s	Minimum Set-Up Time (ENP, ENT, LOAD)	2.0 4.5 6.0		— — —	84 21 18	200 40 34	— — —	250 50 43	— — —	300 60 51	ns
t _s	Minimum Set-Up Time (A, B, C, D)	2.0 4.5 6.0		— — —	16 4 3	50 10 9	— — —	60 12 11	— — —	75 15 13	ns
t _s	Minimum Set-Up Time (CCLR)	2.0 4.5 6.0		— — —	12 3 2.5	50 10 9	— — —	60 12 11	— — —	75 15 13	ns
t _{s(W)}	Minimum Set-Up Time inactive (CCLR)	2.0 4.5 6.0		— — —	12 3 2.5	50 10 9	— — —	60 12 11	— — —	75 15 13	ns
t _s	Minimum Set-Up Time (RCK)	2.0 4.5 6.0		— — —	48 12 10	125 25 21	— — —	160 32 27	— — —	188 38 32	ns
t _s	Minimum Set-Up Time (UD)	2.0 4.5 6.0		— — —	60 15 13	150 30 26	— — —	190 38 32	— — —	225 45 38	ns
t _h	Minimum Hold Time (ALL INPUTS)	2.0 4.5 6.0		— — —	— — —	5 5 5	— — —	5 5 5	— — —	5 5 5	ns
t _{PZL} t _{PHZ}	3-State Outputs Enable Time	2.0 4.5 6.0	R _L = 1kΩ	— — —	56 14 12	110 22 19	— — —	140 28 24	— — —	165 33 28	ns
t _{PLZ} t _{PHZ}	3-State Outputs Disable Time	2.0 4.5 6.0	R _L = 1kΩ	— — —	80 20 17	145 29 25	— — —	180 36 21	— — —	221 44 37	ns
C _{IN}	Input Capacitance			—	5	10	—	10	—	10	pF
C _{PD}	Power Dissipation Capacitance			—	—	113	—	—	—	—	pF