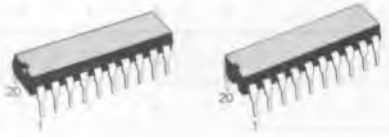
SGS-THOMSON MICROELECTRONICS

M54/74HC690
M54/74HC691

HC690 DECADE COUNTER/REGISTER (3-STATE)
HC691 4-BIT BINARY COUNTER/REGISTER (3-STATE)

- HIGH SPEED
  f_{MAX} = 33MHz (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  V_{NIH} = V_{NIL} = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  15 LSTTL LOADS (FOR Q_A to Q_D)
  10 LSTTL LOADS (FOR RCO)
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}|$ = I_{OL} = 6 mA (MIN.) FOR Q_A to Q_D OUTPUT
  $|I_{OH}|$ = I_{OL} = 4 mA (MIN.) FOR RCO OUTPUT
- BALANCED PROPAGATION DELAYS
  t_{PLH} = t_{PHL}
- WIDE OPERATING VOLTAGE RANGE
  V_{CC}(OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE WITH LSTTL 54/74LS690/691



B1N
Plastic Package

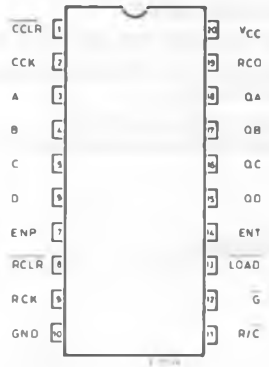
F1
Ceramic Frit Seal Package

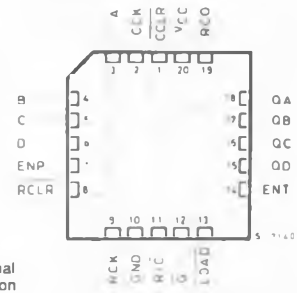
M1
Micro Package

C1
Plastic Chip Carrier

ORDERING NUMBERS:
M54HCXXX F1
M74HCXXX B1N
M74HCXXX F1
M74HCXXX C1
M74HCXXX M1

PIN CONNECTIONS (top view)





NC = No Internal Connection

DESCRIPTION

The HC690/691 are high speed CMOS COUNTER/REGISTER fabricated in silicon gate C²MOS technology.
They have the same high speed performance of LSTTL combined with true CMOS low power consumption.
The internal circuit is composed of 3 stages including buffer output, which offers high noise immunity and stable output.
These devices incorporate a synchronous counter, four-bit D-type register, and quadruple two-line to one-line multiplexers with three-state outputs in a single 20-pin package. The counter can be programmed from the data inputs and have enable P and enable T inputs and a ripple-carry output for easy expansion. The register/counter select input, R/C, selects the counter when low or the register when high for the three-state outputs, QA, QB, QC, and QD.
Individual clock and clear inputs are provided for both the counter and the register. Both clock inputs are positive-edge triggered. The clear lines are active low and is synchronous.
All inputs are equipped with protection circuits against static discharge and transient excess voltage.

TRUTH TABLE

INPUTS									OUTPUTS				FUNCTION
$\overline{CCLR}$	$\overline{LOAD}$	ENP	ENT	CCK	$\overline{RCLR}$	RCK	R/$\overline{C}$	$\overline{G}$	QA	QB	QC	QD	
X	X	X	X	X	X	X	X	H	Z	Z	Z	Z	HIGH IMPEDANCE
L	X	X	X	X	X	X	L	L	L	L	L	L	CLEAR COUNTER
H	L	X	X	↑	X	X	L	L	a	b	c	d	LOAD COUNTER
H	H	L	X	↑	X	X	L	L	NO CHANGE				NO COUNT
H	H	X	L	↑	X	X	L	L	NO CHANGE				NO COUNT
H	H	H	H	↑	X	X	L	L	COUNT UP				COUNT UP
H	X	X	X	↓	X	X	L	L	NO CHANGE				NO COUNT
X	X	X	X	X	L	X	H	L	L	L	L	L	CLEAR REGISTER
X	X	X	X	X	H	↑	H	L	a'	b'	c'	d'	LOAD REGISTER
X	X	X	X	X	H	↓	H	L	NO CHANGE				NO LOAD

X : DON'T CARE

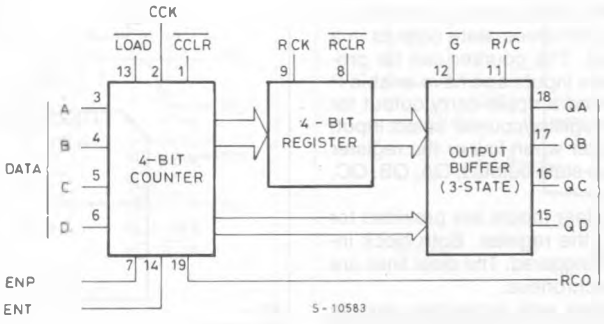
Z : HIGH IMPEDANCE

a-d : THE LEVEL OF STEADY STATE INPUTS AT INPUTS A THROUGH D RESPECTIVELY.

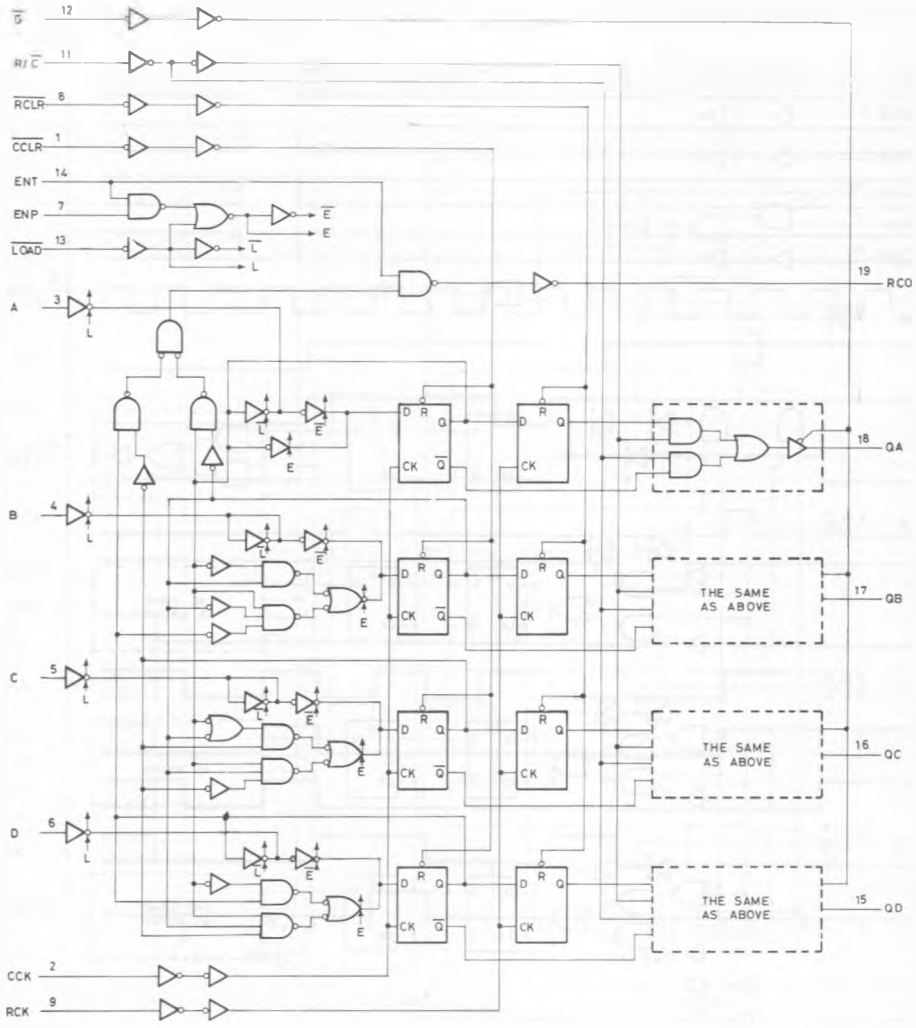
a'-d' : THE LEVEL OF STEADY STATE OUTPUTS AT INTERNAL COUNTER OUTPUTS QA' THROUGH QD' RESPECTIVELY.

HC690 RCO = QA•QD•ENT
HC691 RCO = QA•QB•QC•QD•ENT

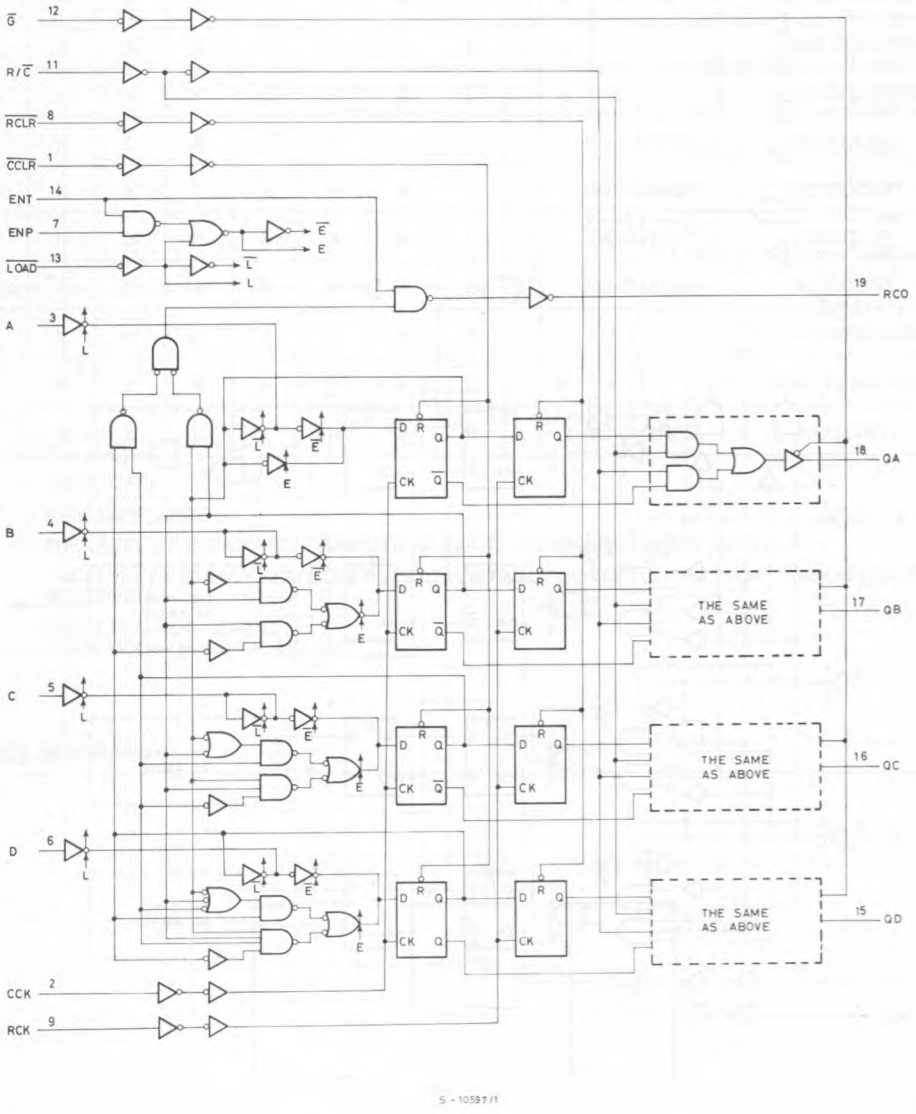
BLOCK DIAGRAM



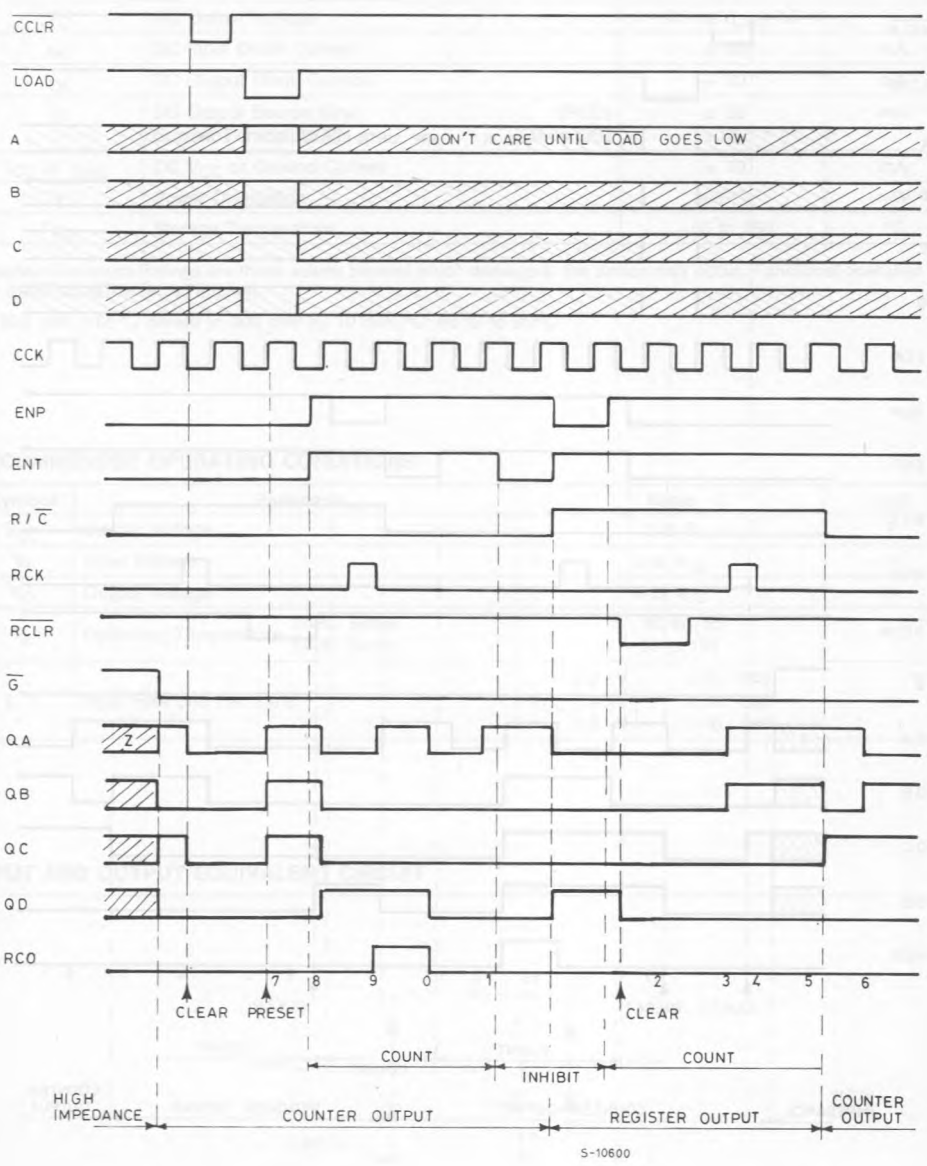
LOGIC DIAGRAM (HC690)



LOGIC DIAGRAM (HC691)



TIMING CHART (HC690)



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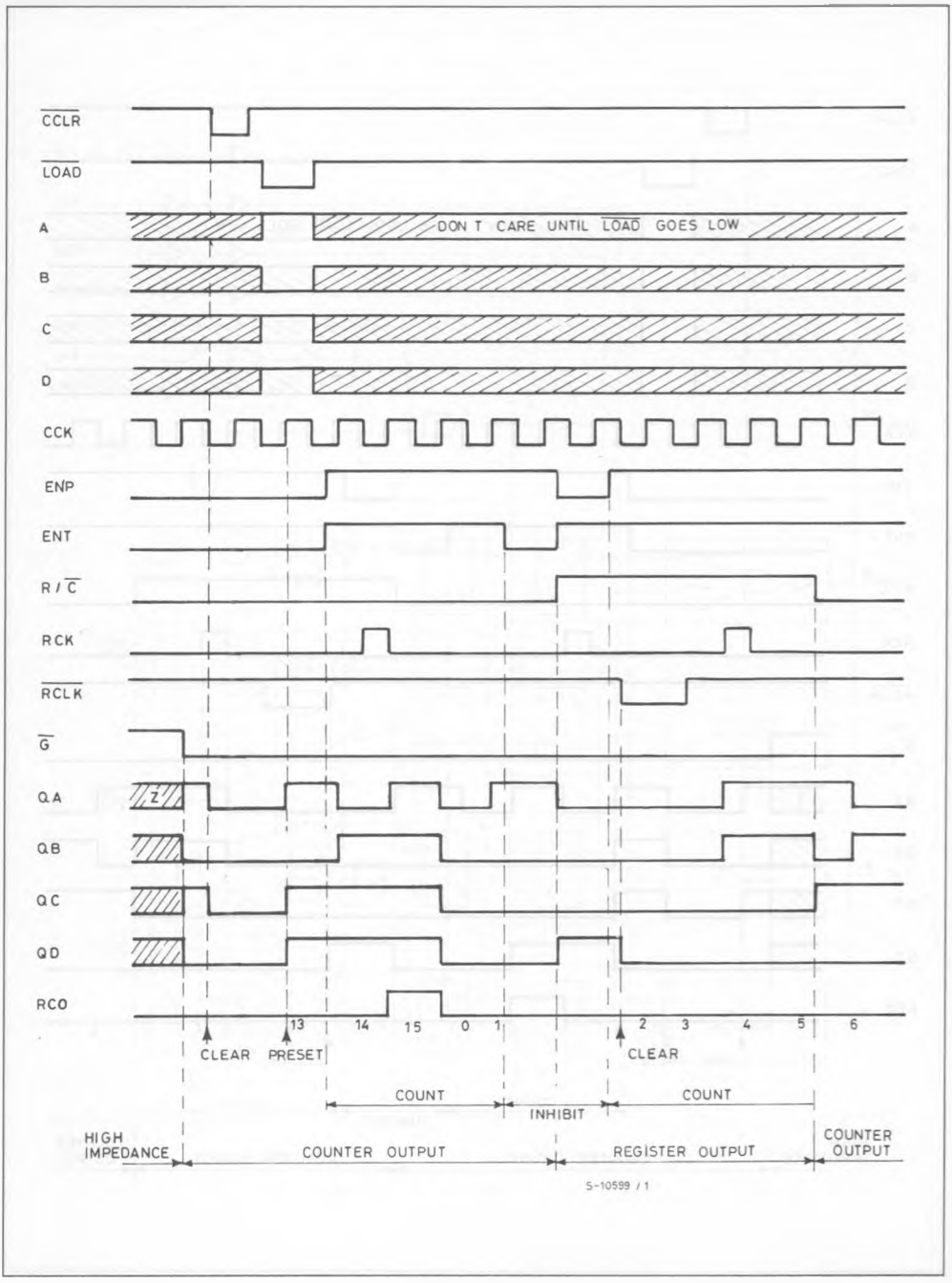


ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin (RCO) (QA to QD)	± 25 ±35	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 70	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

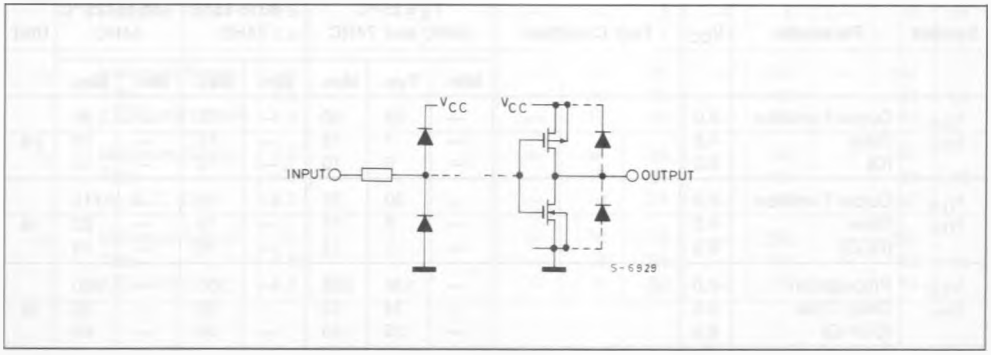
Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value		Unit
V_{CC}	Supply Voltage		2 to 6		V
V_I	Input Voltage		0 to V_{CC}		V
V_O	Output Voltage		0 to V_{CC}		V
T_A	Operating Temperature	74HC Series 54HC Series	− 40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V V_{CC} = 4.5V V_{CC} = 6 V	0 to 1000 0 to 500 0 to 400		ns

INPUT AND OUTPUT EQUIVALENT CIRCUIT



DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min	Typ	Max	Min	Max	Min	Max	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_{IN}	I_{OH}	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5	Q_A-Q_D	−6.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−7.8 mA	5.68	5.8	—	5.63	—	5.60	—	
		4.5	RCO	−4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−5.2 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0	V_{IN}	I_{OL}	—	0	0.1	—	0.1	—	0.1	V
		4.5	V_{IH} or V_{IL}	20 μA	—	0	0.1	—	0.1	—	0.1	
		6.0			—	0	0.1	—	0.1	—	0.1	
		4.5	Q_A-Q_D	6.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		7.8 mA	—	0.18	0.26	—	0.33	—	0.40	
		4.5	RCO	4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
I_{OZ}	3-State Off-State Current	6.0	$V_{IN} = V_{IL}$ or V_{IH} $V_{OUT} = V_{CC}$ or GND		—	—	±0.5	—	±5.0	—	±10	μA
I_{IN}	Input Leakage Current	6.0	$V_{IN} = V_{CC}$ or GND		—	—	±0.1	—	±1.0	—	±1.0	
I_{CC}	Quiescent Supply Current	6.0	$V_{IN} = V_{CC}$ or GND		—	—	4.0	—	40.0	—	80.0	

AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	V_{CC}	Test Condition	$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time (Q)	2.0		—	25	60	—	75	—	90	ns
		4.5		—	7	12	—	15	—	18	
		6.0		—	6	10	—	13	—	15	
t_{TLH} t_{THL}	Output Transition Time (RCO)	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t_{PLH} t_{PHL}	Propagation Delay Time (CCK-Q)	2.0		—	136	265	—	335	—	400	ns
		4.5		—	34	53	—	66	—	80	
		6.0		—	29	45	—	56	—	68	

AC ELECTRICAL CHARACTERISTICS (Continued)

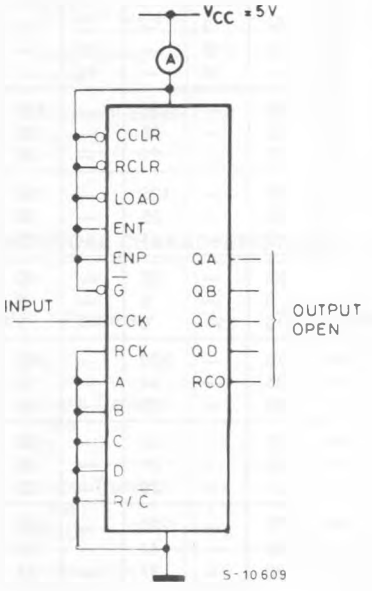
Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{PLH} t_{PHL}	Propagation Delay Time (RCK-Q)	2.0		—	148	285	—	355	—	430	ns
		4.5		—	37	57	—	71	—	86	
		6.0		—	31	48	—	60	—	73	
t_{PLH} t_{PHL}	Propagation Delay Time (CCK-RCO)	2.0		—	128	250	—	315	—	375	ns
		4.5		—	32	50	—	63	—	75	
		6.0		—	27	43	—	54	—	64	
t_{PLH} t_{PHL}	Propagation Delay Time ($R/\overline{C}$-Q)	2.0		—	104	200	—	250	—	300	ns
		4.5		—	26	40	—	50	—	60	
		6.0		—	22	34	—	43	—	51	
t_{PLH} t_{PHL}	Propagation Delay Time (ENT-RCO)	2.0		—	56	110	—	140	—	165	ns
		4.5		—	14	22	—	28	—	33	
		6.0		—	12	19	—	24	—	28	
t_{PHL}	Propagation Delay Time ($\overline{CCLR}$-Q)	2.0		—	160	305	—	385	—	460	ns
		4.5		—	40	61	—	77	—	92	
		6.0		—	12	52	—	66	—	78	
t_{PLH}	Propagation Delay Time ($\overline{CCLR}$-RCO)	2.0		—	132	255	—	320	—	385	ns
		4.5		—	33	51	—	64	—	77	
		6.0		—	28	43	—	54	—	65	
t_{PHL}	Propagation Delay Time ($\overline{RCLR}$-Q)	2.0		—	148	285	—	355	—	430	ns
		4.5		—	37	57	—	71	—	86	
		6.0		—	31	48	—	60	—	73	
f_{MAX}	Maximum Clock Frequency	2.0		4	8	—	3	—	3	—	MHz
		4.5		20	30	—	16	—	13	—	
		6.0		24	35	—	19	—	15	—	
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width (CCK, RCK)	2.0		—	40	100	—	125	—	150	ns
		4.5		—	10	20	—	25	—	30	
		6.0		—	9	17	—	21	—	26	
$t_{W(L)}$	Mimum Pulse Width ($\overline{CCLR}$, $\overline{RCLR}$)	2.0		—	44	100	—	125	—	150	ns
		4.5		—	11	20	—	25	—	30	
		6.0		—	9	17	—	21	—	26	
t_{REM}	Minimum Removal Time	2.0		—	—	25	—	30	—	40	ns
		4.5		—	—	5	—	6	—	8	
		6.0		—	—	5	—	6	—	7	
t_s	Minimum Set-up Time ($\overline{LOAD}$,ENT,ENP)	2.0		—	80	175	—	220	—	265	ns
		4.5		—	20	35	—	44	—	53	
		6.0		—	17	30	—	37	—	45	
t_s	Minimum Set-up Time (A, B, C, D)	2.0		—	48	125	—	155	—	190	ns
		4.5		—	12	25	—	31	—	38	
		6.0		—	10	21	—	26	—	32	
t_s	Minimum Set-up Time (CCK-RCK)	2.0		—	76	175	—	220	—	265	ns
		4.5		—	19	35	—	44	—	53	
		6.0		—	16	30	—	37	—	45	

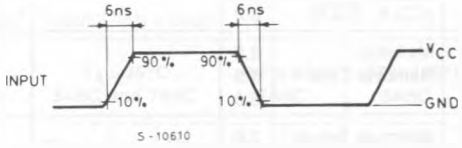
AC ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			− 40 to 85°C 74HC		− 55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_h	Minimum Hold Time	2.0		—	—	0	—	0	—	0	ns
		4.5		—	—	0	—	0	—	0	
		6.0		—	—	0	—	0	—	0	
t_{PZL} t_{PZH}	3-State Output Enable Time	2.0	R_L = 1kΩ	—	72	145	—	180	—	220	ns
		4.5		—	18	29	—	36	—	44	
		6.0		—	15	25	—	31	—	38	
t_{PLZ} t_{PHZ}	3-State Output Disable Time	2.0	R_L = 1kΩ	—	92	170	—	215	—	255	ns
		4.5		—	23	34	—	43	—	51	
		6.0		—	20	29	—	37	—	43	
C_{IN}	Input Capacitance			—	5	10	—	10	—	10	pF
C_{PD} (*)	Power Dissipation Capacitance			—	80	—	—	—	—	—	

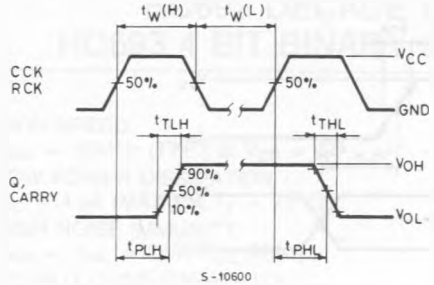
Note (*) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test circuit).
Average operating current can be obtained from the equation:
$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

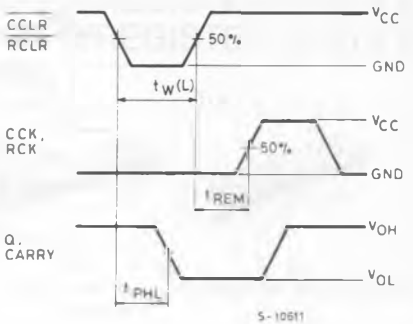
TEST CIRCUIT I_{CC} (Opr.)

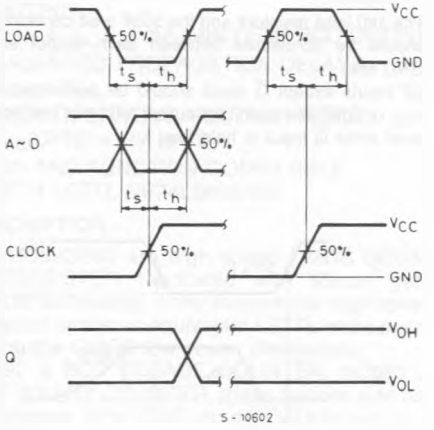




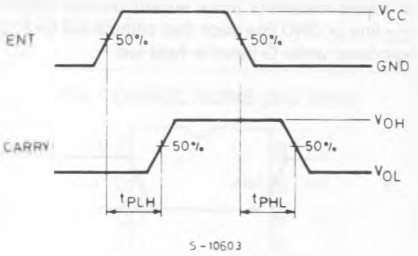
SWITCHING CHARACTERISTICS TEST WAVEFORM

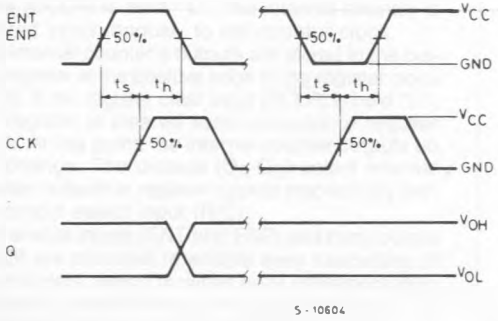


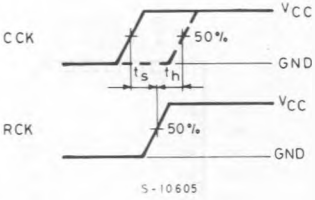




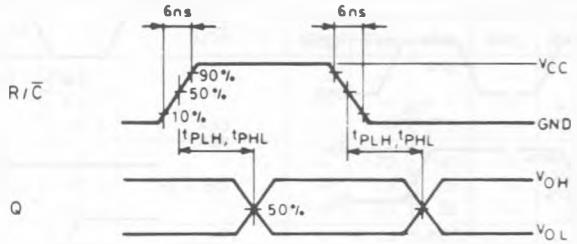
(Fix Maximum Count)







SWITCHING CHARACTERISTICS (Continued)



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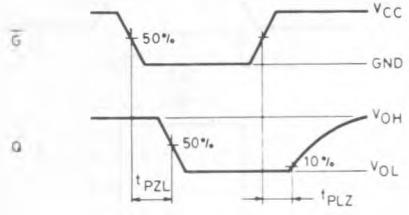
t_{PLZ}, t_{PZL}

The 1kΩ load resistors should be connected between outputs and V_{CC} line and the 50pF load capacitors should be connected between outputs and GND line. All inputs except $\overline{G}$ input should be connected to V_{CC} line or GND line such that outputs will be in low logic level while $\overline{G}$ input is held low.

t_{PHZ}, t_{PZH}

The 1kΩ load resistors and the 50pF load capacitors should be connected between each output and GND line.
All inputs except $\overline{G}$ input should be connected to V_{CC} or GND line such that output will be in low logic level while $\overline{G}$ input is held low.



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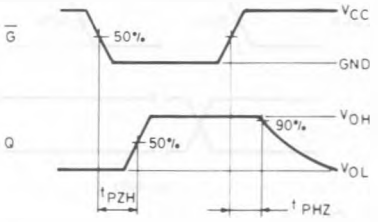

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