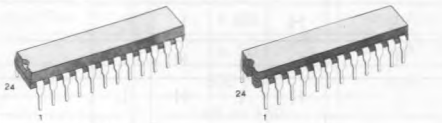
SGS-THOMSON MICROELECTRONICS

M54/74HC4514
M54/74HC4515

HC4514 4-TO-16 LINE DECODER/LATCH
HC4515 4-TO-16 LINE DECODER/LATCH (INV.)

- HIGH SPEED
  t_{PD} = 24 ns (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 4514B/4515B



B1N
Plastic Package

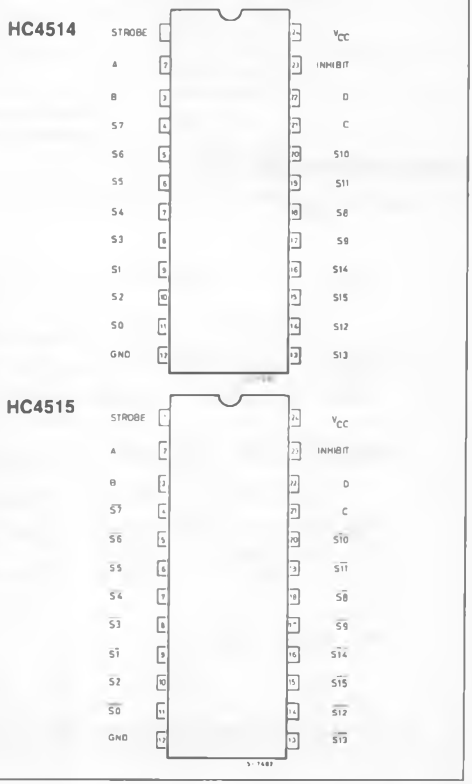
F1
Ceramic Frit Seal Package

M1
Micro Package

ORDERING NUMBERS:

M54HCXXXF1
M74HCXXXB1N
M74HCXXXM1
M74HCXXXF1

PIN CONNECTIONS (top view)



DESCRIPTION

The M54/74HC4514 and the M54/74HC4515 are high speed CMOS 4-LINE TO 16-LINE DECODERS WITH LATCHED INPUTS fabricated in silicon gate C²MOS technology. They have the same high speed performance of LSTTL combined with true CMOS low power consumption.

A binary code stored in the four input latches (A to D) provides a high level (HC4514) or a low level (HC4515) at the selected one of sixteen outputs excluding the other fifteen outputs, when the inhibit input (INHIBIT) is held low. When the inhibit input is held high, all outputs are kept low level (HC4514) or high level (HC4515), while the latch function is available. The data applied to the data inputs are transfered to the Q outputs of latches when the strobe input is held high. When the strobe input is taken low, the information data applied to the data input at a time is retained at the output of the latches. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

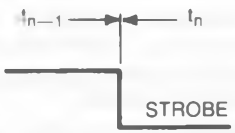
TRUTH TABLE

INPUTS					SELECT OUTPUT HC4514 — 'H' (HC4515 — 'L')
INHIBIT	A	B	C	D	
L	L	L	L	L	S0 ($\overline{S0}$)
L	H	L	L	L	S1 ($\overline{S1}$)
L	L	H	L	L	S2 ($\overline{S2}$)
L	H	H	L	L	S3 ($\overline{S3}$)
L	L	L	H	L	S4 ($\overline{S4}$)
L	H	L	H	L	S5 ($\overline{S5}$)
L	L	H	H	L	S6 ($\overline{S6}$)
L	H	H	H	L	S7 ($\overline{S7}$)
L	L	L	L	H	S8 ($\overline{S8}$)
L	H	L	L	H	S9 ($\overline{S9}$)
L	L	H	L	H	S10 ($\overline{S10}$)
L	H	H	L	H	S11 ($\overline{S11}$)
L	L	L	H	H	S12 ($\overline{S12}$)
L	H	L	H	H	S13 ($\overline{S13}$)
L	L	H	H	H	S14 ($\overline{S14}$)
L	H	H	H	H	S15 ($\overline{S15}$)
H	X	X	X	X	HC4514 — ALL OUTPUTS 'L' (HC4515 — ALL OUTPUTS 'H')

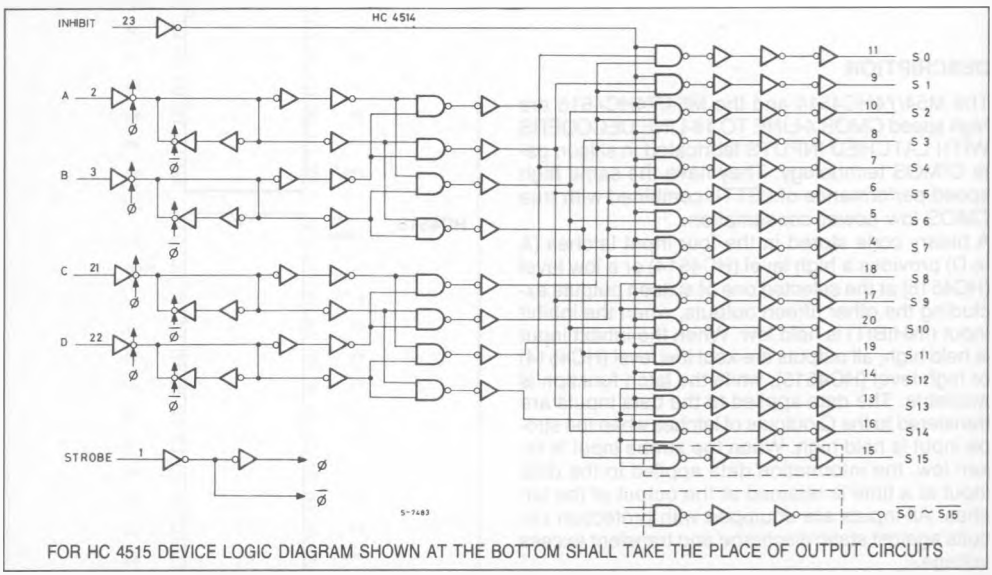
X: DON'T CARE

STROBE = 'H'
REFER TO TRUTH TABLE

STROBE = 'L'
DATA AT THE NEGATIVE GOING TRANSITION OF STROBE SHALL BE PROVIDED ON THE EACH OUPTUT WHILE STROBE IS HELD LOW.



LOGIC DIAGRAM (HC4514)



FOR HC 4515 DEVICE LOGIC DIAGRAM SHOWN AT THE BOTTOM SHALL TAKE THE PLACE OF OUTPUT CIRCUITS

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC}+0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC}+0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value		Unit
V_{CC}	Supply Voltage		2 to 6		V
V_I	Input Voltage		0 to V_{CC}		V
V_O	Output Voltage		0 to V_{CC}		V
T_A	Operating Temperature	74HC Series 54HC Series	− 40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V V_{CC} = 4.5V V_{CC} = 6 V	0 to 1000 0 to 500 0 to 400		ns

DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		T_A = 25°C 54HC and 74HC			− 40 to 85°C 74HC		− 55 to 125°C 54HC		Unit
			V_I	I_O	Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_{IH} or V_{IL}	−20 μA	1.9	2.0	—	1.9	—	1.9	—	V
		4.5			4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		−4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−5.2 mA	5.68	5.8	—	5.63	—	5.60	—	

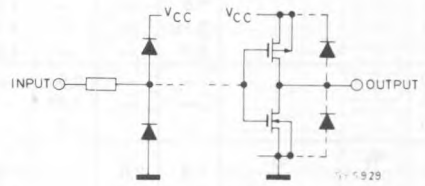
DC SPECIFICATIONS (Continued)

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{OL}	Low Level Output Voltage	2.0	V_I	I_O	—	0	0.1	—	0.1	—	0.1	V
		4.5	V_{IH} or V_{IL}	20 μA	—	0	0.1	—	0.1	—	0.1	
		6.0			—	0	0.1	—	0.1	—	0.1	
		4.5		4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
I_I	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND		—	—	±0.1	—	±1	—	±1	μA
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND		—	—	4	—	40	—	80	μA

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time (Data - Sn, $\overline{Sn}$)		24	37	ns
t_{PLH} t_{PHL}	Propagation Delay Time (STROBE - Sn, $\overline{Sn}$)		27	44	ns
t_{PLH} t_{PHL}	Propagation Delay Time (INHIBIT - Sn, $\overline{Sn}$)		19	30	ns

INPUT AND OUTPUT EQUIVALENT CIRCUIT

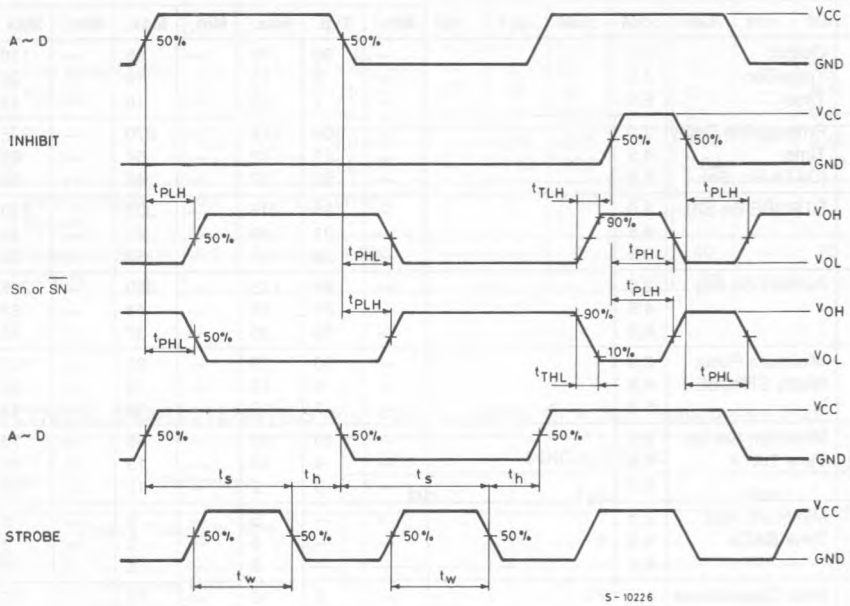


AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

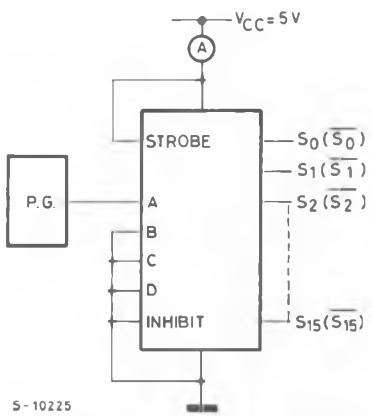
Symbol	Parameter	V_{CC}	Test Condition	$T_A = 25°C$ 54HC and 74HC			− 40 to 85°C 74HC		− 55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} T_{THL}	Output Transition Time	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t_{PLH} t_{PHL}	Propagation Delay Time (DATA-Sn, $\overline{Sn}$)	2.0		—	108	215	—	270	—	325	ns
		4.5		—	27	43	—	54	—	65	
		6.0		—	23	37	—	46	—	55	
t_{PLH} t_{PHL}	STROBE-Sn $\overline{Sn}$)	2.0		—	124	245	—	305	—	370	ns
		4.5		—	31	49	—	61	—	74	
		6.0		—	26	42	—	52	—	63	
t_{PLH} t_{PHL}	INHIBIT-Sn $\overline{Sn}$)	2.0		—	88	175	—	220	—	265	ns
		4.5		—	22	35	—	44	—	53	
		6.0		—	19	30	—	37	—	45	
$t_{W(H)}$	Minimum Pulse Width STROBE	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t_s	Minimum Set-Up Time DATA	2.0		—	10	50	—	65	—	75	ns
		4.5		—	4	10	—	13	—	15	
		6.0		—	3	9	—	11	—	13	
t_h	Minimum Hold Time DATA	2.0		—	—	5	—	5	—	5	ns
		4.5		—	—	5	—	5	—	5	
		6.0		—	—	5	—	5	—	5	
C_{IN}	Input Capacitance			—	5	10	—	10	—	10	pF
C_{PD} (*)	Power Dissipation Capacitance		HC4514	—	69	—	—	—	—	—	pF
			HC4515	—	72	—	—	—	—	—	

Note (*): C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).
Average operating curren can be obtained by the following equation. $I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$.

SWITCHING CHARACTERISTICS TEST WAVEFORM



TEST CIRCUIT I_{CC} (Opr.)



INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.