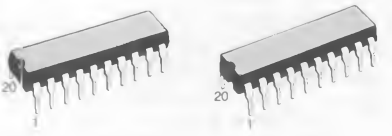
SGS-THOMSON MICROELECTRONICS

M54HC354
M74HC354

8-CHANNEL MULTIPLEXER/REGISTER (3-STATE)

- HIGH SPEED
  t_{PD} = 33 ns (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28% V_{CC} (MIN).
- OUTPUT DRIVE CAPABILITY
  15 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 6 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS354



B1N
Plastic Package

F1
Ceramic Frit Seal Package

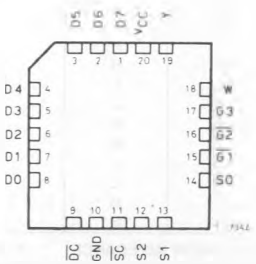
M1
Micro Package

C1
Plastic Chip Carrier

ORDERING NUMBERS:

M54HC354 F1
M74HC354 B1N
M74HC354 F1
M74HC354 C1
M74HC354 M1

PIN CONNECTIONS (top view)

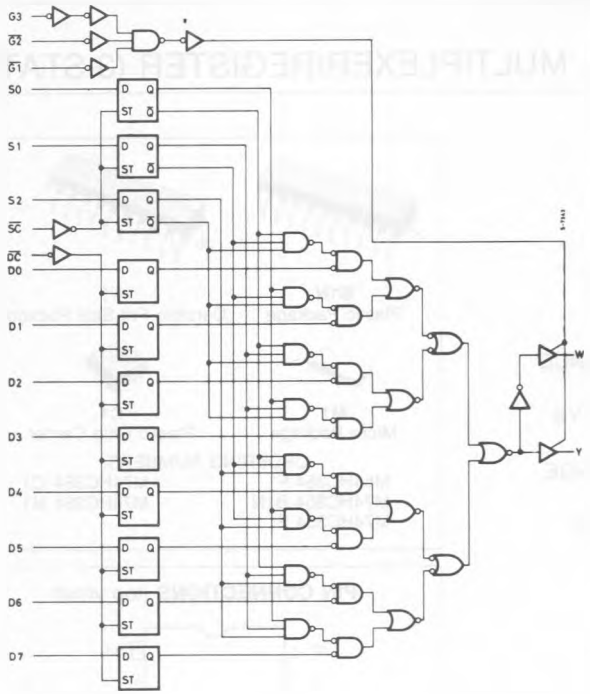


NC =
No Internal
Connection

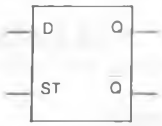
DESCRIPTION

The M54/74HC354 is a high speed CMOS 8-CHANNEL MULTIPLEXER/REGISTER (3-state) fabricated in silicon gate C²MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low consumption.
This device contains an 8 channel digital multiplexer with an 8-bit input data register and a 3-bit address input register with 3-state outputs. The one of eight input data will be provided on the Y output pin (non-inverted output) and W output pin (inverted output) determined by the address data.
The information at the data inputs (D0 to D7) is stored in the 8-bit latch at the negative pulse on $\overline{DC}$ input. The information at the address inputs (S0 to S2) is stored in the 3-bit latch at the negative pulse on $\overline{SC}$ input. These outputs are disabled to be high-impedance when input $\overline{G1}$ is held high, input $\overline{G2}$ is held high or input G3 is held low. This device is suitable for interfacing with bus lines in a bus organized system.
The M54/74HC354 is similar in function to the M54/74HC356, which has an 8-bit flip-flop as the data register instead of an 8-bit latch. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

LOGIC DIAGRAM



TRUTH TABLE OF INTERNAL LATCH



INPUTS		OUTPUTS	
D	ST	Q	$\overline{Q}$
L	H	L	H
H	H	H	L
X	L	Qn	$\overline{Qn}$

X: DON'T CARE
Qn: DATA STORED AT THE TRAILING EDGE OF THE MOST RECENT ST PULSE.

TRUTH TABLE

INPUTS							OUTPUTS	
SELECT*			$\overline{DC}$	OUTPUT ENABLES				
S2	S1	S0		$\overline{G1}$	$\overline{G2}$	G3	W	Y
X	X	X	X	H	X	X	Z	Z
X	X	X	X	X	H	X	Z	Z
X	X	X	X	X	X	L	Z	Z
L	L	L	L	L	L	H	$\overline{D0}$	D0
L	L	L	H	L	L	H	$\overline{D0n}$	D0n
L	L	H	L	L	L	H	$\overline{D1}$	D1
L	L	H	H	L	L	H	$\overline{D1n}$	D1n
L	H	L	L	L	L	H	$\overline{D2}$	D2
L	H	L	H	L	L	H	$\overline{D2n}$	D2n
L	H	H	L	L	L	H	$\overline{D3}$	D3
L	H	H	H	L	L	H	$\overline{D3n}$	D3n
H	L	L	L	L	L	H	$\overline{D4}$	D4
H	L	L	H	L	L	H	$\overline{D4n}$	D4n
H	L	H	L	L	L	H	$\overline{D5}$	D5
H	L	H	H	L	L	H	$\overline{D5n}$	D5n
H	H	L	L	L	L	H	$\overline{D6}$	D6
H	H	L	H	L	L	H	$\overline{D6n}$	D6n
H	H	H	L	L	L	H	$\overline{D7}$	D7
H	H	H	H	L	L	H	$\overline{D7n}$	D7n

X: DON'T CARE - Z: HIGH IMPEDANCE *: THIS COLUMN SHOWS THE INPUT ADDRESS SETUP WITH $\overline{SC}$ LOW.
D0n.....D7n: THE LEVEL OF STEADY-STATE INPUTS AT INPUT D0 THROUGH D7, RESPECTIVELY, BEFORE THE MOST RECENT OF THE LOW-TO-HIGH TRANSITION OF DATA CONTROL.

ABSOLUTE MAXIMUM RATINGS

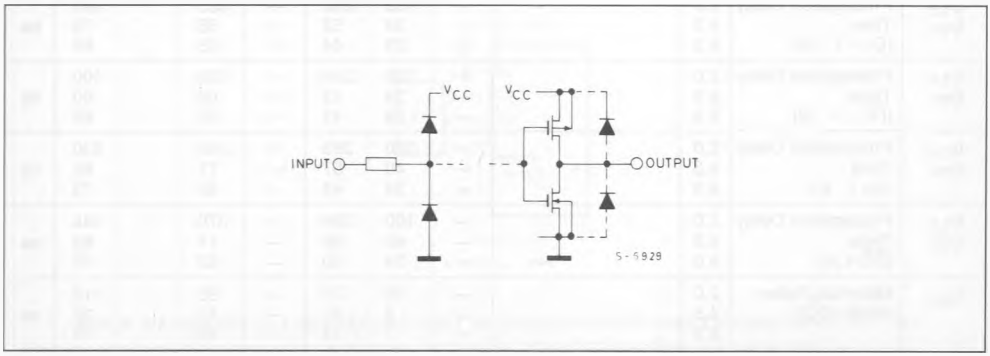
Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 35	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 70	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_A	Operating Temperature	74HC Series 54HC Series	−40 to 85 −55 to 125	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V V_{CC} = 4.5V V_{CC} = 6 V	0 to 1000 0 to 500 0 to 400	ns

INPUT AND OUTPUT EQUIVALENT CIRCUIT



DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			− 40 to 85°C 74HC		− 55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0 4.5 6.0			1.5 3.15 4.2	— — —	— — —	1.5 3.15 4.2	— — —	1.5 3.15 4.2	— — —	V
V_{IL}	Low Level Input Voltage	2.0 4.5 6.0			— — —	— — —	0.5 1.35 1.8	— — —	0.5 1.35 1.8	— — —	0.5 1.35 1.8	V
V_{OH}	High Level Output Voltage	2.0 4.5 6.0	V_I V_{IH} or V_{IL}	I_O − 20 μA	1.9 4.4 5.9	2.0 4.5 6.0	— — —	1.9 4.4 5.9	— — —	1.9 4.4 5.9	— — —	V
		4.5 6.0		− 6.0 mA − 7.8 mA	4.18 5.68	4.31 5.8	—	4.13 5.63	—	4.10 5.60	—	
V_{OL}	Low Level Output Voltage	2.0 4.5 6.0	V_{IH} or V_{IL}	20 μA	— — —	0.0 0.0 0.0	0.1 0.1 0.1	— — —	0.1 0.1 0.1	— — —	0.1 0.1 0.1	V
		4.5 6.0		6.0 mA 7.8 mA	— —	0.17 0.18	0.26 0.26	— —	0.33 0.33	— —	0.40 0.40	
I_I	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND		—	—	±0.1	—	±1.0	—	±1.0	μA
I_{OZ}	3 State Output Off-State Current	6.0	$V_I = V_{IH}$ or V_{IL} $V_O = V_{CC}$ or GND		—	—	±0.5	—	±5		±10	μA
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND		—	—	4	—	40	—	80	μA

AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

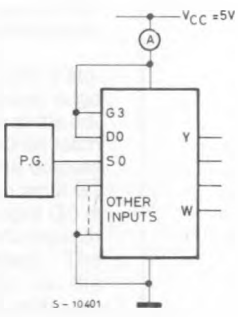
Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			− 40 to 85°C 74HC		− 55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0 4.5 6.0		— — —	25 7 6	60 12 10	— — —	75 15 13		90 18 15	ns
t_{PLH} t_{PHL}	Propagation Delay Time (Dn - Y, W)	2.0 4.5 6.0		— — —	135 34 29	260 52 44	— — —	325 65 55		390 78 66	ns
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{DC}$ - Y, W)	2.0 4.5 6.0		— — —	135 34 29	265 53 45	— — —	335 66 56		400 80 68	ns
t_{PLH} t_{PHL}	Propagation Delay Time (Sn-Y, W)	2.0 4.5 6.0		— — —	160 40 34	285 57 48	— — —	355 71 60		430 86 73	ns
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{SC}$-Y,N)	2.0 4.5 6.0		— — —	160 40 34	295 59 50	— — —	370 74 63		445 89 76	ns
$t_{W(L)}$	Minimum Pulse Width (DC)	2.0 4.5 6.0		— — —	30 8 7	75 15 13	— — —	95 19 16		110 22 19	ns

AC ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
$t_{W(L)}$	Minimum Pulse Width (SC)	2.0 4.5 6.0		— — —	30 8 7	75 15 13	— — —	95 19 16		110 22 19	ns
t_s	Minimum Set-up Time (Sn)	2.0 4.5 6.0		— — —	20 5 4	75 15 13	— — —	95 19 16		110 22 19	ns
t_s	Minimum Set-up Time (Dn)	2.0 4.5 6.0		— — —	25 5 4	75 15 13	— — —	95 19 16	— — —	110 22 19	ns
t_h	Minimum Hold Time (Sn)	2.0 4.5 6.0		— — —	— — —	5 5 5	— — —	5 5 5	 — 	5 5 5	ns
t_h	Minimum Hold Time (Dn)	2.0 4.5 6.0		— — —	— — —	0 0 0	— — —	0 0 0	— — —	0 0 0	ns
t_{PZL} t_{PZH}	Output Enable Time	2.0 4.5 6.0	 R_L = 1kΩ	— — —	68 17 15	125 25 21	— — —	155 31 26		190 38 32	
t_{PLZ} t_{PHZ}	Output Disable Time	2.0 4.5 6.0	 R_L = 1kΩ	— — —	60 22 20	155 31 26	— — —	195 39 33		235 47 40	ns
C_{IN}	Input Capacitance			—	5	10	—	10		10	
C_{OUT}	Output Capacitance			—	10	—	—	—			pF
C_{PD} (*)	Power Dissipation Capacitance			—	84	—	—	—			pF

Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit)
Average operating current can be obtained by the following equation.
I_{CC} (Opr) = $C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$.

TEST CIRCUIT I_{CC} (Opr.)



INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST

SWITCHING CHARACTERISTICS TEST WAVEFORM