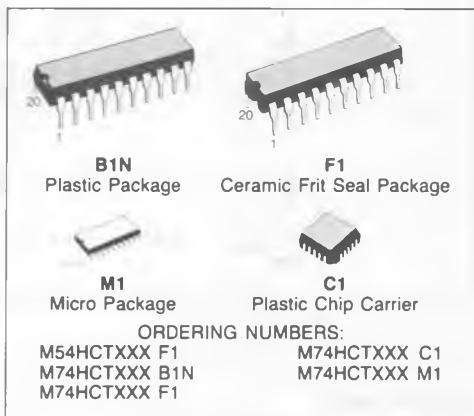


HC299 8-BIT PIPO SHIFT REGISTER WITH ASYNCHRONOUS CLEAR

HC323 8-BIT PIPO SHIFT REGISTER WITH SYNCHRONOUS CLEAR

- **LOW POWER DISSIPATION**
 $I_{CC} = 4 \mu A$ (MAX.) at $T_A = 25^\circ C$
- **HIGH NOISE IMMUNITY**
 $V_{NIH} = V_{NIL} = 28\% V_{CC}$ (Min.)
- **OUTPUT DRIVE CAPABILITY**
 10 LSTTL LOADS
- **SYMMETRICAL OUTPUT IMPEDANCE**
 $|I_{OH}| = I_{OL} = 6 \text{ mA}$ (MIN.) for Q_A , to Q_H ,
 $|I_{OH}| = I_{OL} = 4 \text{ mA}$ (MIN.) for Q_A , to Q_H
- **BALANCED PROPAGATION DELAYS**
 $t_{PLH} = t_{PHL}$
- **WIDE OPERATING VOLTAGE RANGE**
 V_{CC} (OPR) = 2V to 6V
- **PIN AND FUNCTION COMPATIBLE**
 WITH 54/74LS299



DESCRIPTION

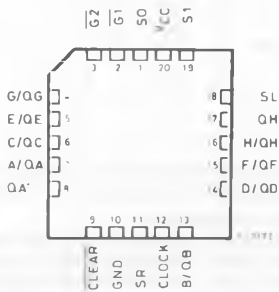
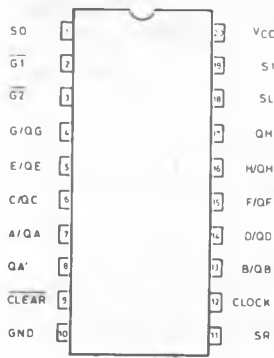
The M54/74HC299/323 are high speed CMOS 8-BIT PIPO SHIFT REGISTERS (3-STATE) fabricated with silicon gate C²MOS technology. They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power consumption.

These devices have four modes (HOLD, SHIFT LEFT, SHIFT RIGHT and LOAD DATA). Each mode is chosen by two function select inputs (S0, S1). When one or both enable inputs, (G1, G2) are high, the eight input/output terminals are in the high-impedance state; however sequential operation or clearing of the register is not affected.

Clear function on the HC299 is asynchronous to CLOCK, while the HC323 is cleared synchronous to clock.

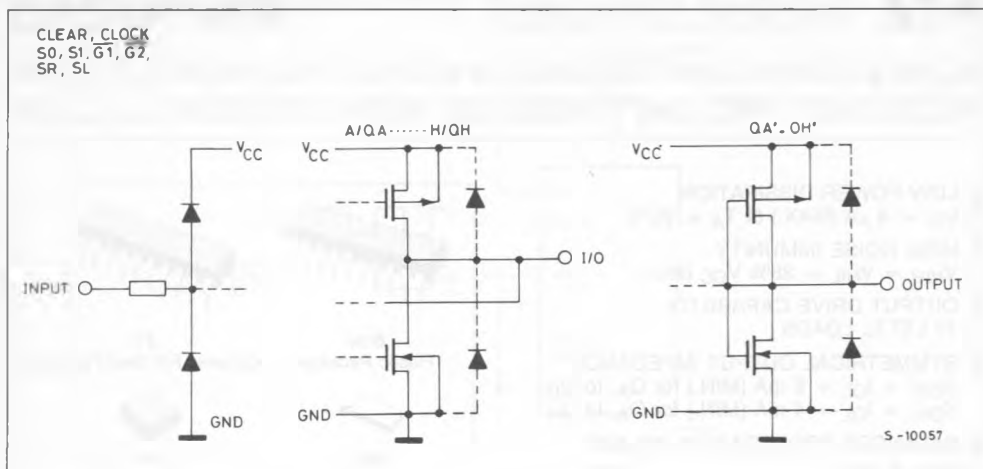
All inputs are equipped with protection circuits against static discharge and transient excess voltage.

PIN CONNECTIONS (top view)



NC =
No Internal
Connection

INPUT AND OUTPUT EQUIVALENT CIRCUIT



TRUTH TABLE

MODE	INPUTS						INPUTS/OUTPUTS				OUTPUTS		
	CLEAR	FUNCTION SELECT		OUTPUT CONTROL		CLOCK		SERIAL		A/QA	H/QH	QA'	QH'
		S1	S0	G1°	G2°	(299)	(323)	SL	SR				
Z	L	H	H	X	X	X		X	X	Z	Z	L	L
CLEAR	L	L	X	L	L	X		X	X	L	L	L	L
	L	X	L	L	L	X		X	X	L	L	L	L
HOLD	H	L	L	L	L	X		X	X	QA0	QH0	QA0	QH0
SHIFT RIGHT	H	L	H	L	L			X	H	H	QGn	H	QGn
	H	L	H	L	L			X	L	L	QGn	L	QGn
SHIFT LEFT	H	H	L	L	L			H	X	QBn	H	QBn	H
	H	H	L	L	L			L	X	QBn	L	QBn	L
LOAD	H	H	H	X	X			X	X	a	h	a	h

* When one or both output controls are high, the eight input/output terminals are in the high-impedance state; however sequential operation or clearing of the register is not affected.

Z : HIGH IMPEDANCE

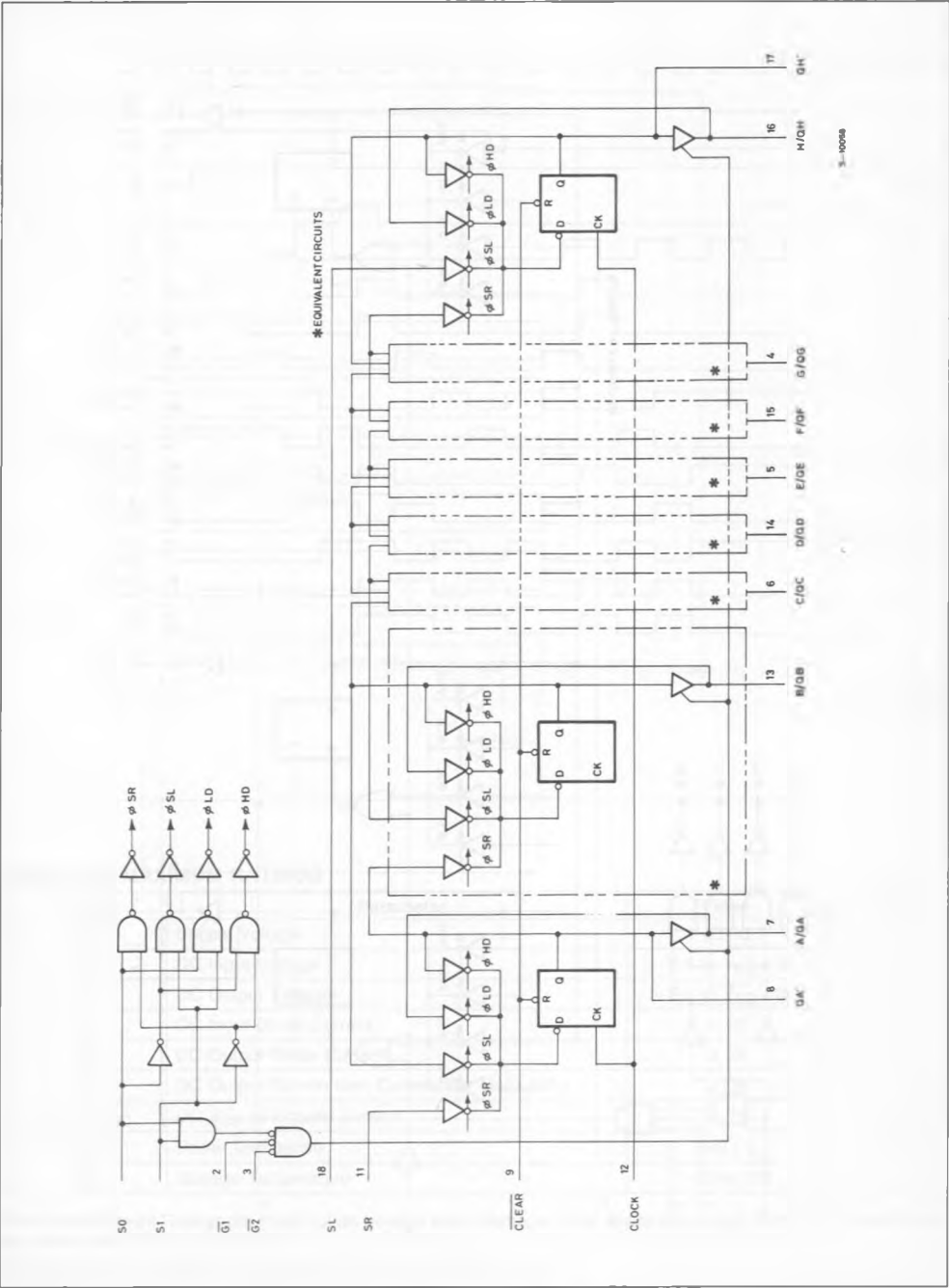
Qn0 : THE LEVEL OF An BEFORE THE INDICATED STEADY-STATE INPUT CONDITIONS WERE ESTABLISHED.

Qnn : THE LEVEL OF Qn BEFORE THE MOST RECENT ACTIVE TRANSITION INDICATED BY ↓ OR ↑

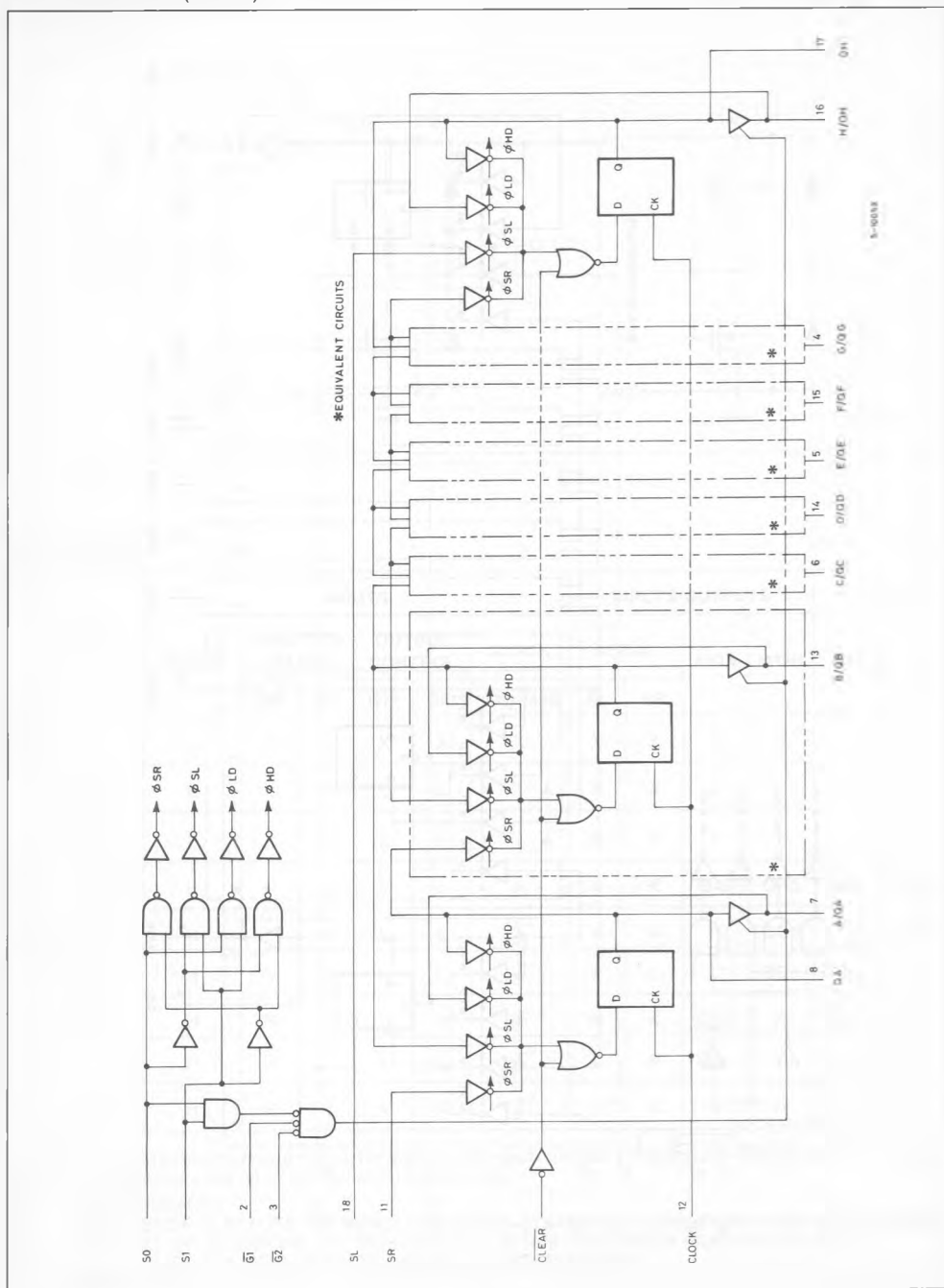
a,h : THE LEVEL OF THE STEADY-STATE INPUTS A, H, RESPECTIVELY.

X : DON'T CARE

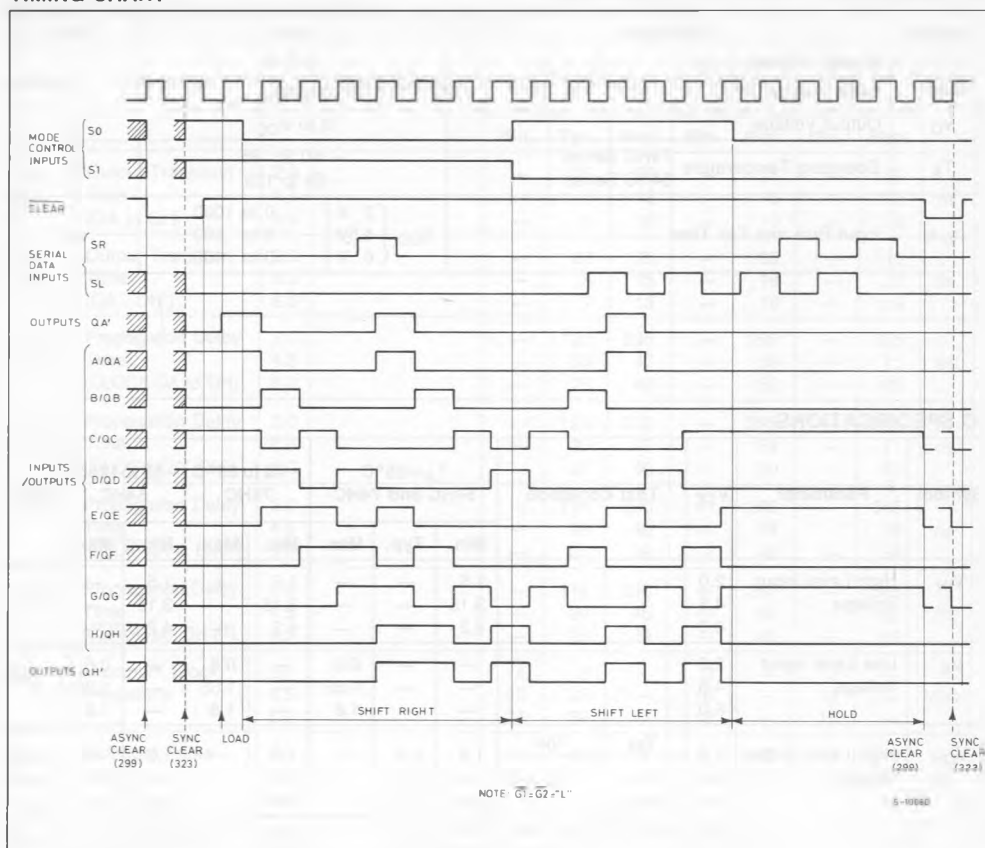
LOGIC DIAGRAM (HC299)



LOGIC DIAGRAM (HC323)



TIMING CHART



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	- 0.5 to 7	V
V_I	DC Input Voltage	- 0.5 to $V_{CC} + 0.5$	V
V_O	DC Output Voltage	- 0.5 to $V_{CC} + 0.5$	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 35	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 70	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	- 65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: $\cong 65^\circ\text{C}$ derate to 300 mW by 10 mW/°C: 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	2 to 6	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_A	Operating Temperature 74HC Series 54HC Series	- 40 to 85 - 55 to 125	°C
t_r, t_f	Input Rise and Fall Time	$V_{CC} \begin{cases} 2 \text{ V} & 0 \text{ to } 1000 \\ 4.5 \text{ V} & 0 \text{ to } 500 \\ 6 \text{ V} & 0 \text{ to } 400 \end{cases}$	ns

DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition	$T_A = 25^\circ\text{C}$ 54HC and 74HC			- 40 to 85°C 74HC		- 55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0 4.5 6.0		1.5 3.15 4.2	— — —	— — —	1.5 3.15 4.2	— — —	1.5 3.15 4.2	— — —	V
V_{IL}	Low Level Input Voltage	2.0 4.5 6.0		— — —	— — —	0.5 1.35 1.8	— — —	0.5 1.35 1.8	— — —	0.5 1.35 1.8	V
V_{OH}	High Level Output Voltage	2.0	V_{IN}	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	I_{OH}	4.4	4.5	—	4.4	—	4.4	—	
		6.0	V_{IH} or V_{IL}	5.9	6.0	—	5.9	—	5.9	—	
		4.5	Q_A to Q_H	4.18	4.31	—	4.13	—	4.10	—	
		6.0	-6.0 mA -7.8 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0	V_{IN}	—	0	0.1	—	0.1	—	0.1	V
		4.5	I_{OH}	—	0	0.1	—	0.1	—	0.1	
		6.0	V_{IH} or V_{IL}	—	0	0.1	—	0.1	—	0.1	
		4.5	Q_A to Q_H	—	0.17	0.26	—	0.33	—	0.40	
		6.0	7.8 mA	—	0.18	0.26	—	0.33	—	0.40	
I_{OZ}	3-State Output Off-State Current	6.0	Q_A', Q_H'	—	0.17	0.26	—	0.33	—	0.40	μA
		4.5	-4.0 mA -5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
		6.0	$V_{IN} = V_{IL}$ or V_{IH} $V_{OUT} = V_{CC}$ or GND	—	—	± 0.5	—	± 5.0	—	± 10	
		6.0	$V_{IN} = V_{CC}$ or GND	—	—	± 0.1	—	± 1.0	—	± 1.0	
		6.0	$V_{IN} = V_{CC}$ or GND	—	—	4	—	40	—	80	

AC ELECTRICAL CHARACTERISTICS ($C_L = 50\text{pF}$, Input $t_r = t_f = 6\text{ns}$)

Symbol	Parameter	V_{CC}	Test Condition	$T_A = 25^\circ\text{C}$ 54HC and 74HC			-40 to 85°C 74HC		-55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time (QA to QH)	2.0 4.5 6.0		— — —	25 7 6	60 12 10	— — —	75 15 13	— — —	90 18 15	ns
t_{TLH} t_{THL}	Output Transition Time (QA', QH')	2.0 4.5 6.0		— — —	30 8 7	75 15 13	— — —	95 19 16	— — —	110 22 19	ns
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK-QA to QH)	2.0 4.5 6.0		— — —	120 30 26	235 47 40	— — —	295 59 50	— — —	355 71 60	ns
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK-QA', QH')	2.0 4.5 6.0		— — —	120 30 26	235 47 40	— — —	295 59 50	— — —	345 71 60	ns
t_{PHL}	Propagation Delay Time ($\overline{\text{CLEAR}}$ -QA to QH) ⁽¹⁾	2.0 4.5 6.0		— — —	116 29 25	230 46 39	— — —	290 58 49	— — —	345 69 59	ns
t_{PHL}	Propagation Delay Time ($\overline{\text{CLEAR}}$ -QA', QH') ⁽¹⁾	2.0 4.5 6.0		— — —	116 29 25	230 46 39	— — —	290 58 49	— — —	345 69 59	ns
f_{MAX}	Maximum Clock Frequency	2.0 4.5 6.0		4 20 24	8 33 39	— — —	3 16 19	— — —	3 13 15	— — —	MHz
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width (CLOCK)	2.0 4.5 6.0		— — —	30 8 7	75 15 13	— — —	95 19 16	— — —	110 22 19	ns
$t_{W(L)}$	Minimum Pulse Width $\overline{\text{CLEAR}}$	2.0 4.5 6.0		— — —	50 12 10	100 20 17	— — —	125 25 21	— — —	150 30 26	ns
t_s	Minimum Set-up Time (SL, SR, A to H)	2.0 4.5 6.0		— — —	25 6 5	75 15 13	— — —	95 19 16	— — —	110 22 19	ns
t_s	Minimum Set-up Time (S0, S1)	2.0 4.5 6.0		— — —	50 13 11	125 25 21	— — —	155 31 26	— — —	190 38 32	ns
t_s	Minimum Set-up Time ($\overline{\text{CLEAR}}$) ⁽²⁾	2.0 4.5 6.0		— — —	32 8 7	75 15 13	— — —	95 19 16	— — —	110 22 19	ns
t_h	Minimum Hold Time (SL, SR, A to H)	2.0 4.5 6.0		— — —	— — —	0 0 0	— — —	0 0 0	— — —	0 0 0	ns
t_h	Minimum Hold Time (S0, S1)	2.0 4.5 6.0		— — —	— — —	0 0 0	— — —	0 0 0	— — —	0 0 0	ns

(1) Apply to M54/74HC299

(2) Apply to M54/74HC323

AC ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Parameter	V _{CC}	Test Condition	T _A = 25°C 54HC and 74HC			– 40 to 85°C 74HC		– 55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t _H	Minimum Hold Time (CLEAR) (2)	2.0 4.5 6.0		—	—	0	—	0	—	0	ns
t _{REM}	Minimum Removal Time (CLEAR) (1)	2.0 4.5 6.0		—	—	25	—	30	—	40	ns
t _{PZL} t _{PZH}	3-State Output Enable Time	2.0 4.5 6.0	R _L = 1kΩ	—	100	195	—	245	—	295	ns
t _{PLZ} t _{PHZ}	3-State Output Disable Time	2.0 4.5 6.0	R _L = 1kΩ	—	112	200	—	250	—	300	ns
C _{IN}	Input Capacitance			—	5	10	—	10	—	10	pF
C _{OUT}	Output Capacitance (QA to QH)			—	13	—	—	—	—	—	pF
C _{PD} (*)	Power Dissipation Capacitance			—	221	—	—	—	—	—	pF

Note (*) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test circuit).

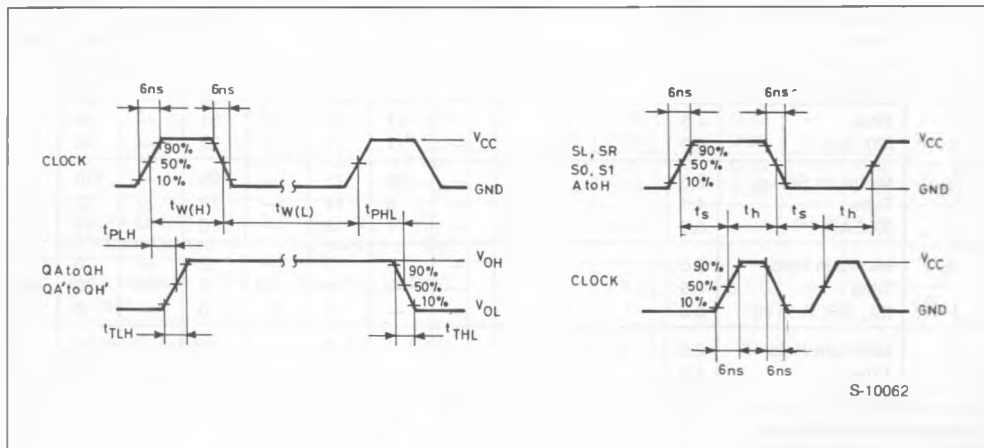
Average operating current can be obtained from the equation:

$$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

(1) Apply to M54/74HC299

(2) Apply to M54/74HC323

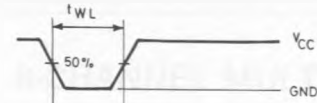
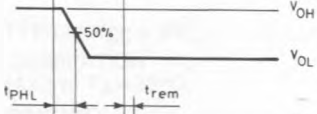
SWITCHING CHARACTERISTICS TEST WAVEFORM



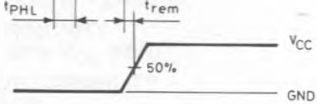
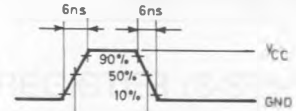
SWITCHING CHARACTERISTICS TEST WAVEFORM (Continued)

HC299

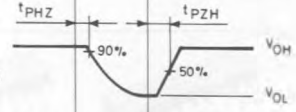
CLEAR

QA to QH
QA to QH'

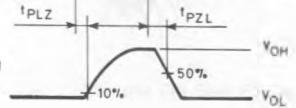
CLOCK

 $\overline{G1}, \overline{G2}$ 

QA to QH

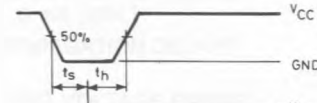


QA to QH

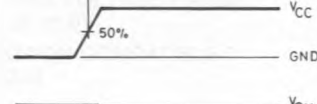


HC323

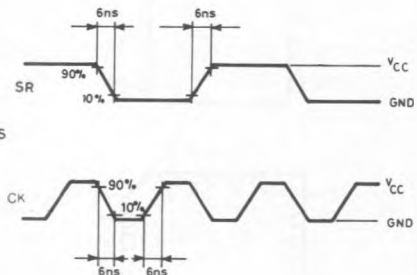
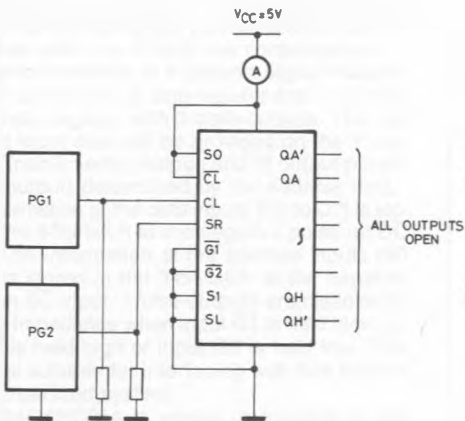
CLEAR



CLOCK

QA to QH
QA' to QH'

S-10062

TEST CIRCUIT I_{CC} (Opr.)

S-10061