SGS-THOMSON MICROELECTRONICS

M5156

A-LAW COMPANDING CODEC

- ±5-VOLT POWER SUPPLIES
- LOW POWER DISSIPATION - 30mW (Typ)
- FOLLOWS THE A-LAW COMPANDING CODE
- INCLUDES CCITT RECOMMENDED EVEN-ORDER-BIT INVERSION
- SYNCHRONOUS OR ASYNCHRONOUS OPERATION
- ON-CHIP SAMPLE AND HOLD
- ON-CHIP OFFSET NULL CIRCUIT ELIMINATES LONG-TERM DRIFT ERRORS AND NEED FOR TRIMMING
- MINIMAL EXTERNAL CIRCUITRY REQUIRED
- SERIAL DATA OUTPUT OF 64kb/s THROUGH 2.1Mb/s AT 8kHz SAMPLING RATE
- SEPARATE ANALOG AND DIGITAL GROUNDS REDUCE NOISE PROBLEMS

DESCRIPTION

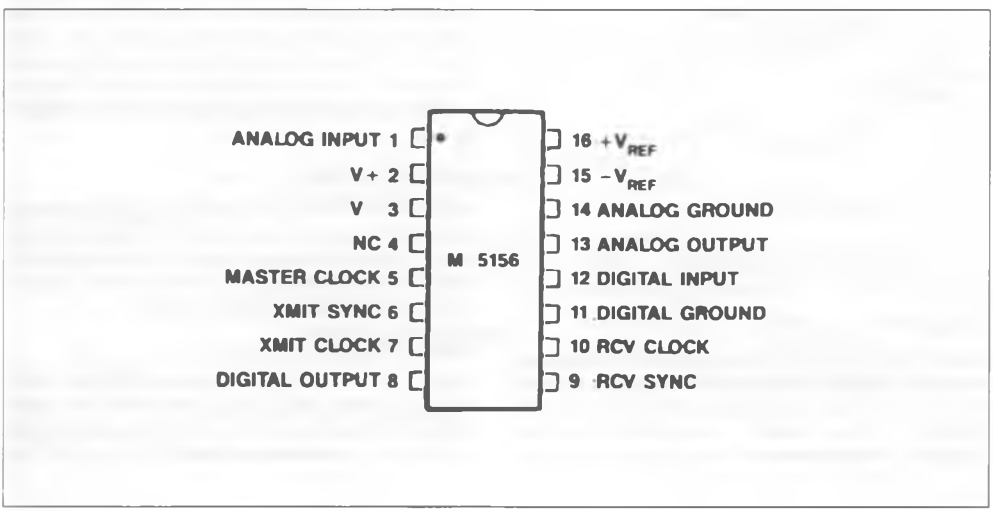
The M5156 is a monolithic CMOS companding CODEC that contains two sections : (1) An analog-to-digital converter with a transfer characteristic conforming to the A-law companding code and (2) a digital-to-analog converter that also conforms to the A-law code.

These two sections form a coder-decoder designed to meet the needs of the telecommunications industry for per-channel voice-frequency CODECs used in digital switching and transmission systems. Digital input and output are in serial format. Actual transmission and reception of 8-bit data words containing the analog information is done at a 64kb/s through 2.1Mb/s rate with analog signal sampling occuring at an 8kHz rate. A sync pulse input is provided for synchronizing transmission and reception of multi-channel information being multiplexed over a single transmission line.

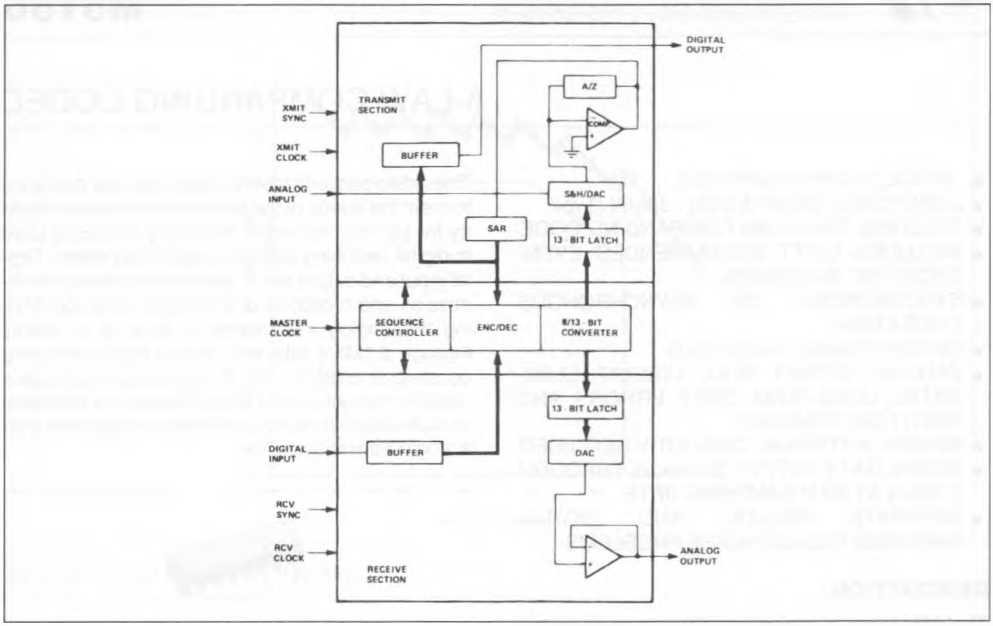
DIP-16

ORDER CODES : M5156FI (Ceramic)

PIN CONNECTION (top view)

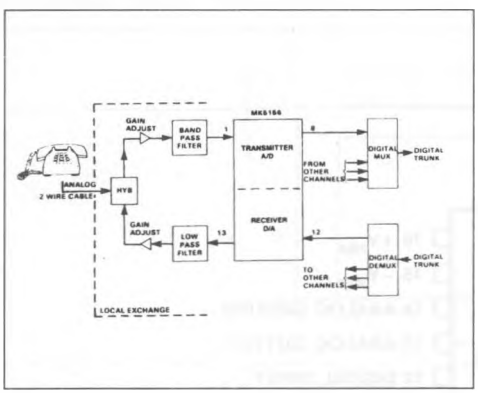


BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

PCM SYSTEM BLOCK DIAGRAM



+ V_{REF} AND - V_{REF}

Input. Pins 16 and 15. These positive and negative reference voltages provide the conversion references for the digital-to-analog converters in the M5156. + V_{REF} and - V_{REF} must maintain 100ppM/°C regulation over the operating temperature range. Variation of the reference directly affects system gain.

ANALOG INPUT

Input. Pin 1. Voice-frequency analog signals that are bandwidth-limited to 4kHz are input at this pin. Typically, they are then sampled at an 8kHz rate. (See figure 1). The analog input must remain between + V_{REF} and - V_{REF} for accurate conversion. The recommended input interface circuit is shown in figure 6.

MASTER CLOCK

Input. Pin 5. This signal provides the basic timing and control signals required for all internal conversions. It does not have to be synchronized with RCV SYNC, RCV CLOCK, XMIT SYNC or XMIT CLOCK and is not internally related to them.

XMIT SYNC

Input. Pin 6. This input is synchronized with XMIT CLOCK. When XMIT SYNC goes high, the digital output is activated and the A/D conversion begins on the next positive edge of MASTER CLOCK. The

conversion by MASTER CLOCK can be asynchronous with XMIT CLOCK. The serial output data is clocked out by the positive edges of XMIT CLOCK. The negative edge of XMIT SYNC causes the digital output to become three-state. XMIT SYNC must go low for at least one master clock period prior to the transmission of the next digital word. (see figure 9).

XMIT CLOCK

Input. Pin 7. The on-chip 8-bit output shift register of the M5156 is unloaded at the clock rate present on this pin. Clock rates of 64kHz-2.1MHz can be used for XMIT CLOCK. The positive edge of the INTERNAL CLOCK transfers the data from the master to the slave of a master-slave flip-flop. (See figure 2). If the positive edge of XMIT SYNC occurs after the positive edge of XMIT CLOCK, XMIT SYNC will determine when the first positive edge of internal clock will occur. In this event, the hold time for the first clock pulse is measured from the positive edge of XMIT SYNC.

RCV SYNC

Input. Pin 9. This input is synchronized with RCV CLOCK and serial data is clocked in by RCV CLOCK. Duration of the RCV SYNC pulse is approximately 8 RCV CLOCK periods. The conversion from digital-to-analog starts after the negative edge of the RCV SYNC pulse. (see figure 1). The negative edge of RCV SYNC should occur before the 9th positive clock edge of insure that only eight bits are clocked in. RCV SYNC must stay low for 17 MASTER CLOCKS (min.) before the next digital word is to be received (see figure 10).

RCV CLOCK

Input. Pin 10. The on-chip 8-bit shift register for the M5156 is loaded at the clock rate present on this pin. Clock rates of 64kHz-2.1MHz can be used for

Figure 1 : A/D, D/A Conversion Timing.

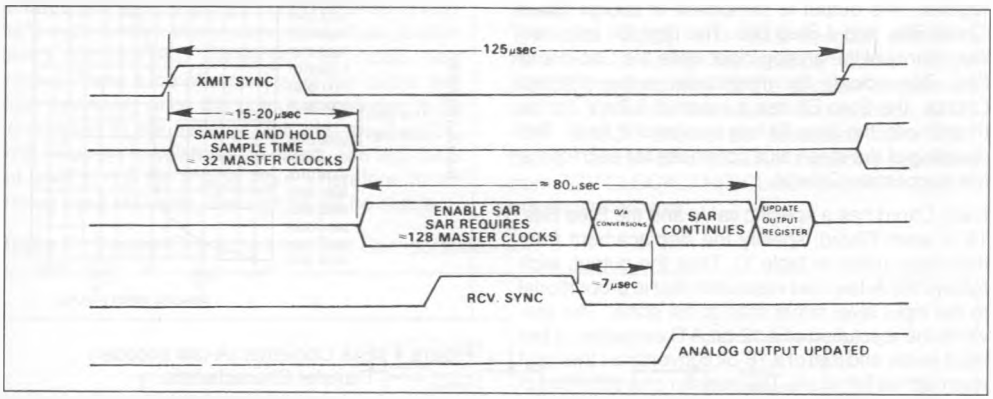
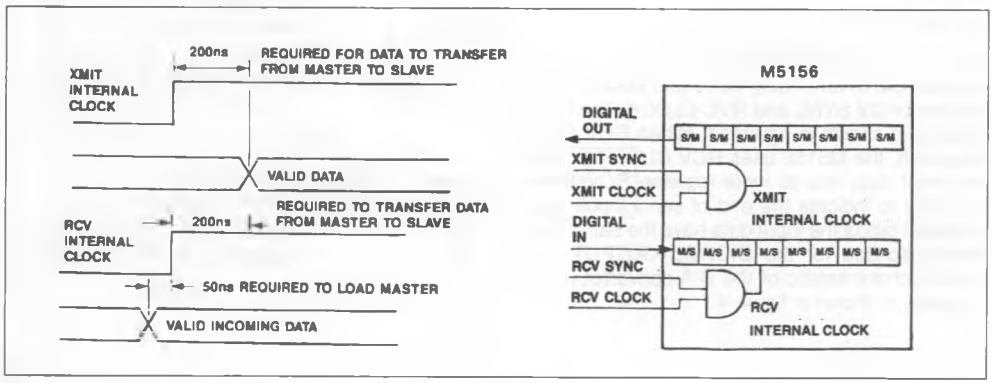


Figure 2 : Data Input/Output Timing.



RCV CLOCK. Valid data should be applied to the digital input before the positive edge of the internal clock. (See figure 2). This set up time, t_{RDS}, allows the data to be transferred into the master of a master-slave flip-flop. The positive edge of the internal clock transfers the data to the slave of the master-slave flip-flop. A hold time, t_{RDH}, is required to complete this transfer. If the rising edge of RCV SYNC occurs after the first rising edge of RCV CLOCK, RCV SYNC will determine when the first positive edge of internal clock will occur. In this event, the set-up and hold times for the first clock pulse should be measured from the positive edge of RCV SYNC.

DIGITAL OUTPUT

Output. Pin 8. The M5156 output register stores the 8-bit encoded sample of the analog input. This 8-bit word is shifted out under control of XMIT SYNC and XMIT CLOCK. When XMIT SYNC is low, the DIGITAL OUTPUT is an open circuit. When XMIT SYNC is high, the state of the DIGITAL OUTPUT is determined by the value of the output bit in the serial shift register. The output is composed of a Sign Bit, 3 Chord Bits, and 4 Step Bits. The Sign Bit indicates the polarity of the analog input while the Chord and Step Bits indicate the magnitude. In the first two Chords, the Step Bit has a value of 1.2mV. In the third Chord, the Step Bit has a value of 2.4mV. This doubling of the step value continues for each of the five successive Chords.

Each Chord has a specific value and the Step Bits, 16 in each Chord, specify the displacement from that value (refer to table 1). Thus the output, wich follows the A-law, has resolution that is proportional to the input level rather than to full scale. This provides the resolution of a 12-bit A/D converter at low input levels and that of a 16-bit converter as the input approaches full scale. The transfer characteristic of the A/D converter (A-law Encoder) is shown in figure 3.

DIGITAL INPUT

Input. Pin 12. The M5156 input register accepts the 8-bit sample of an analog value and loads it under control of RCV SYNC and RVC CLOCK. The timing diagram is shown in figure 11. When RCV SYNC goes high, the M5156 uses RCV CLOCK to clock the serial data into its input register. RCV SYNC goes low to indicate the end of serial inputr data. The eight bits of the input data have the same functions described for the DIGITAL OUTPUT. The transfer characteristic of the D/A converter (A-law Decoder) is shown in figure 4.

Table 1 : Digital Output Code : A Law.

	Chord Code	Chord Value	Step Value
1.	101	0.0mV	1.221mV
2.	100	20.1mV	1.221mV
3.	111	40.3mV	2.44mV
4.	110	80.6mV	4.88mV
5.	001	161.1mV	9.77mV
6.	000	332mV	19.53mV
7.	011	645mV	39.1mV
8.	010	1.289V	78.1mV

EXAMPLE :

1 110 0111 = + 80.6mV + (2 x 4.88mV)

Sign Bit Chord Step Bits

If the sign bit were a zero, then both plus signs would be changed to minus signs.

Figure 3 : A/D Converter (A-law encoder) Transfer Characteristic.

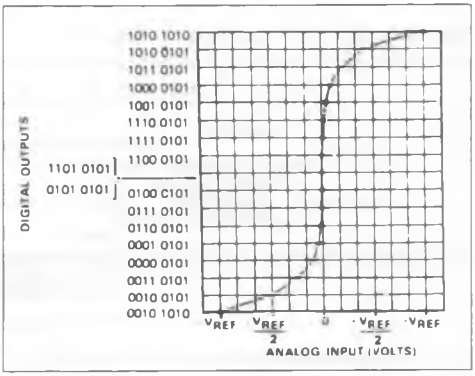
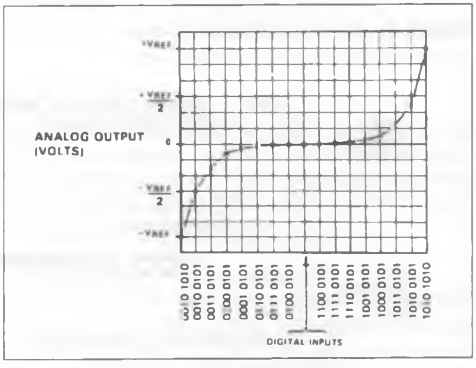


Figure 4 : D/A Converter (A-law encoder) Transfer Characteristic.



ANALOG OUTPUT

Output. Pin 13. The analog output is in the form of voltage steps (100 % duty cycle) having amplitude equal to the analog sample which was encoded. This waveform is then filtered with an external low-pass filter with sinx/x correction to recreate the sampled voice signal.

OPERATION OF CODEC WITH 64kHz XMIT/RCV. CLOCK FREQUENCIES

XMIT/RCV SYNC must not be allowed to remain at a logic "1" state. XMIT SYNC is required to be at a logic "0" state for one master clock period (min.) before the next digital word is transmitted. RCV SYNC is required to be at a logic "0" state for 17 master clock periods (min.) before the next digital word is received (see figures 9 and 10).

OFFSET NULL

The offset null feature of the M5156 eliminates long-term drift errors and conversion errors due to temperature changes by going through an offset adjustment cycle before every conversion, thus guaranteeing accurate A/D conversion for inputs near ground. There is no offset adjust of the output amplifier because, since the output is intended to be AC-coupled to the external filter. the resultant DC error ($V_{OFFSET\ O}$) will have no effect. The sign bit is not used to null the analog input. Therefore, for an analog input of 0 volts, the sign bit will be stable.

PERFORMANCE EVALUATION

The equipment connections shown in figure 5 can be used to evaluate the performance of the M5156. An analog signal provided by the HP3552A Transmission Test Set is connected to the Analog Input (pin 1) of the M5156. The Digital Output of the CODEC is tied back to the Digital Input and the Analog Output is fed through a low-pass filter to the HP2552A. Remaining pins of the M5156 are connected as follows :

(1) RCV SYNC is tied to XMIT SYNC
(2) XMIT CLOCK is tied to MASTER CLOCK. The signal is inverted and tied to RCV CLOCK.

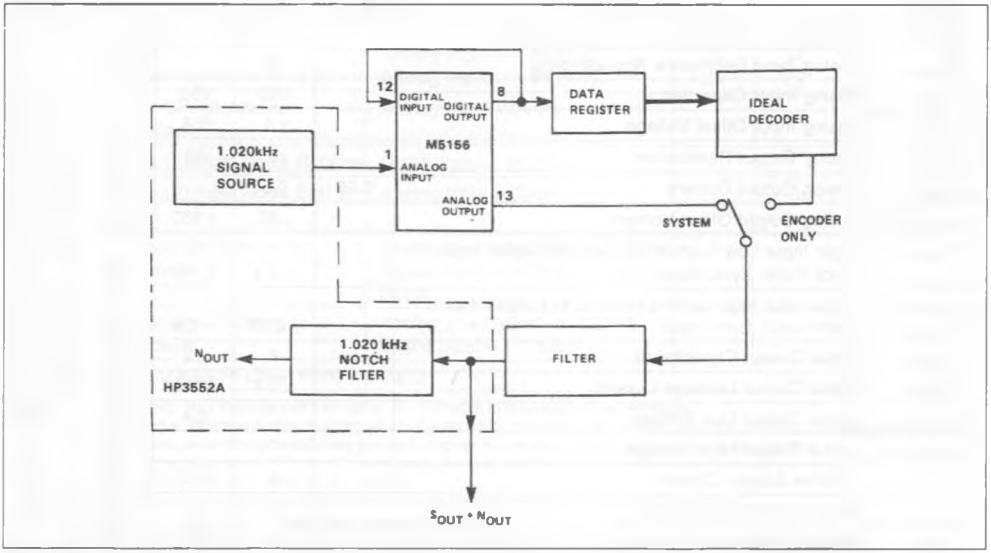
The following timing signals are required :

(1) MASTER CLOCK = 2.048MHz
(2) XMIT SYNC repetition rate = 8kHz
(3) XMIT SYNC width = 8 XMIT CLOCK periods

When all the above requirements are met, the setup of figure 5 permits the measurement of synchronous system performance over a wide range of analog inputs.

The data register and ideal decoder provide a means of checking the encoder portion of the M5156 independently of the decoder section. To test the system in the asynchronous mode, MASTER CLOCK should be separated from XMIT CLOCK and MASTER CLOCK should be separated from RCV CLOCK. XMIT CLOCK and RCV CLOCK are separated also.

Figure 5 : System Characteristics Test Configuration.



Note : The ideal decoder consists of a digital decompander and a 13-bit precision DAC.

ABSOLUTE MAXIMUM RATINGS

Parameter	Value	Unit
DC Supply Voltage, V+	+ 6	V
DC Supply Voltage, V–	– 6	V
Ambient Operating Temperature, T_A	0 to 70	°C
Storage Temperature	– 55 to + 125	°C
Package Dissipation at 25°C (derated 9mW/°C when soldered into PCB)	500	mW
Digital Input	$-0.5V \leq V_{IN} \leq V+$	
Analog Input	$V- \leq V_{IN} \leq V+$	
$+ V_{REF}$	$-0.5V \leq + V_{REF} \leq V+$	
$- V_{REF}$	$V- \leq - V_{REF} \leq + 0.5$	V

* Stressed above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating condition for extended periods may affect device reliability.

ELECTRICAL OPERATING CHARACTERISTICS

POWER SUPPLY

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
V+	Positive Supply Voltage	4.75	5.0	5.25	V	
V–	Negative Supply Voltage	– 5.25	– 5.0	– 4.75	V	
$+ V_{REF}$	Positive Reference Voltage	2.375	2.5	2.625	V	1
$- V_{REF}$	Negative Reference Voltage	– 2.625	– 2.5	– 2.375	V	1

TEST CONDITIONS : V+ = 5.0V, V– = – 5.0V, $+ V_{REF}$ = 2.5V, $- V_{REF}$ = – 2.5V, T_A = 0°C to 70°C

DC CHARACTERISTICS

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
R_{INAS}	Analog Input Resistance During Sampling		2		kΩ	2
R_{INANS}	Analog Input Resistance Non-sampling		100		MΩ	
C_{INA}	Analog Input Capacitance		150	250	pF	2
$V_{OFFSET/1}$	Analog Input Offset Voltage		± 1	± 8	mV	2
R_{OUTA}	Analog Output Resistance		1	50	Ω	
I_{OUTA}	Analog Output Current	0.25	0.5		mA	
$V_{OFFSET/0}$	Analog Output Offset Voltage		+ 50	± 850	mV	
I_{INLOW}	Logic Input Low Current (V_{IN} = 0.8V) Digital Input, Clock Input, Sync Input		± 0.1	± 10	µA	3
I_{INHIGH}	Logic Input High Current (V_{IN} = 2.4V) Digital Input, Clock Input, Sync Input		– 0.25	– 0.8	mA	3
C_{DO}	Digital Output Capacitance		8	12	pF	
I_{DOL}	Digital Output Leakage Current		± 0.1	± 10	µA	
V_{OUTLOW}	Digital Output Low Voltage			0.4	V	4
$V_{OUTHIGH}$	Digital Output High Voltage	3.9			V	4
I+	Positive Supply Current		4	10	mA	5
I–	Negative Supply Current		2	6	mA	5
I_{REF+}	Positive Reference Current		4	20	µA	
I_{REF-}	Negative Reference Current		4	20	µA	

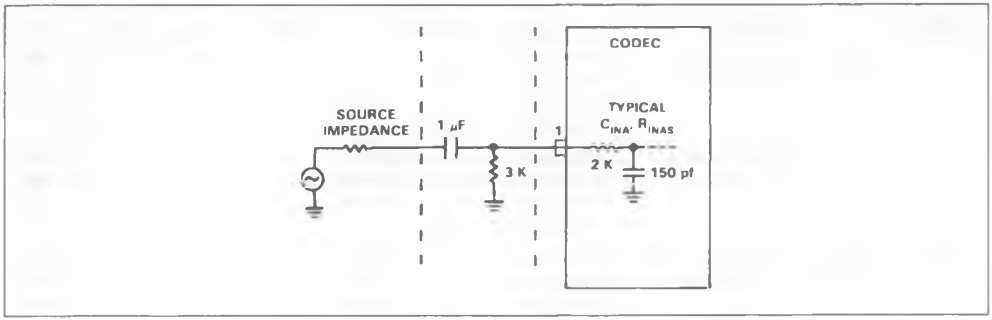
AC CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
GT_X	Gain Tracking Transmit CCITT G712 Method 2	Analog Input = + 3 to – 40dBm0 Analog Input = – 40 to – 50dBm0 Analog Input = – 50 to – 55dBm0 Relative to – 10 dBm0	– .2 – .4 – 1.25	0.0 ± 0.1 ± 0.2	+ .2 + .4 + 1.25	dB dB dB
GT_R	Gain Tracking Receive CCITT G712 Method 2	Input Level = + 3 to – 40dBm0 Input Level = – 40 to – 50dBm0 Input Level = – 50 to – 55dBm0 Relative to – 10 dBm0	– .2 – .4 – 1.25	0.0 ± 0.1 ± 0.2	+ .2 + .4 + 1.25	dB dB dB
GT_{EE}	Gain Tracking End to End CCITT G712 Method 2	Analog Input = + 3 to – 40dBm0 Analog Input = – 40 to – 50dBm0 Analog Input = – 50 to – 55dBm0 Relative to – 10 dBm0	– 0.4 – 0.8 – 2.5	± 0.1 ± 0.1 ± 0.2	+ 0.4 + 0.8 + 2.5	dB dB dB
$SD1_X$	Signal to Distortion Transmit CCITT G712 Method 1	Analog Input = – 3dBm0 Analog Input = – 6 to – 27dBm0 Analog Input = – 34dBm0 Analog Input = – 40dBm0 Analog Input = – 55dBm0 Narrow Band Noise Input	30 36 34 30 15			dB dB dB dB dB
$SD1_R$	Signal to Distortion Receive CCITT G712 Method 1	Input Level = – 3dBm0 Input Level = – 6 to – 27dBm0 Input Level = – 34dBm0 Input Level = – 40dBm0 Input Level = – 55dBm0 Narrow Band Noise Input	30 37 35 31 16			dB dB dB dB dB
$SD2_X$	Signal to Distortion Transmit CCITT G712 Method 2	Analog Input = 0 to – 30dBm0 Analog Input = – 40dBm0 Analog Input = – 45dBm0	37 31 25			dB dB dB
$SD2_R$	Signal to Distortion Receive CCITT G712 Method 2	Input Level = 0 to – 30dBm0 Input Level = – 40dBm0 Input Level = – 45dBm0	37 31 25			dB dB dB
SD_{EE}	Signal to Distortion End to End CCITT G712 Method 2	Analog Input = 0 to – 30dBm0 Analog Input = – 40dBm0 Analog Input = – 45dBm0	35 29 24	39 34 29		db db dB
N_X	Idle Channel Noise Transmit	Analog Input = 0Volts			– 68	dBm0p
N_R	Idle Channel Noise Receive	Digital Input = + 0 Code			– 90	dBm0p
N_{EE}	Idle Channel Noise End to End	Analog Input = 0Volts		– 80	– 68	dBm0p
CT_{RX}	Crosstalk Receive to Transmit	Analog In = – 50dBm0 at 2600Hz Digital Input = 0dBm0 at 1008Hz Digital			– 80	dB
CT_{XR}	Crosstalk Transmit to Receive	Analog In = 0dBm0 at 1008Hz Digital Input = + 0 Code			– 80	dB
TLP	Transmission Level Point	600Ω		+ 4		dB

Notes :

1. - V_{REF} and - V_{REF} must be matched within ±1 % in order to meet system requirements.
2. Sampling is accomplished by charging an internal capacitor ; therefore, the designer should avoid excessive source impedance. Input related device characteristics are derived using the Recommended Analog Input Circuit. See figure 6.
3. When a transition from a "1" to a "0" takes place, the user must sink the "1" current until reading the "0" level.
4. Driving 30pF with I_{OH} = - 100 µA, I_{OL} - 500 µA.
5. Results in 30mW typical power dissipation (clocks applied) under normal operating conditions.
6. This delay is necessary to avoid overlapping Clock and Sync.
7. This first bit of data is loaded when Sync and Clock are both "1" during bit time 1 as shown on RCV timing diagram.

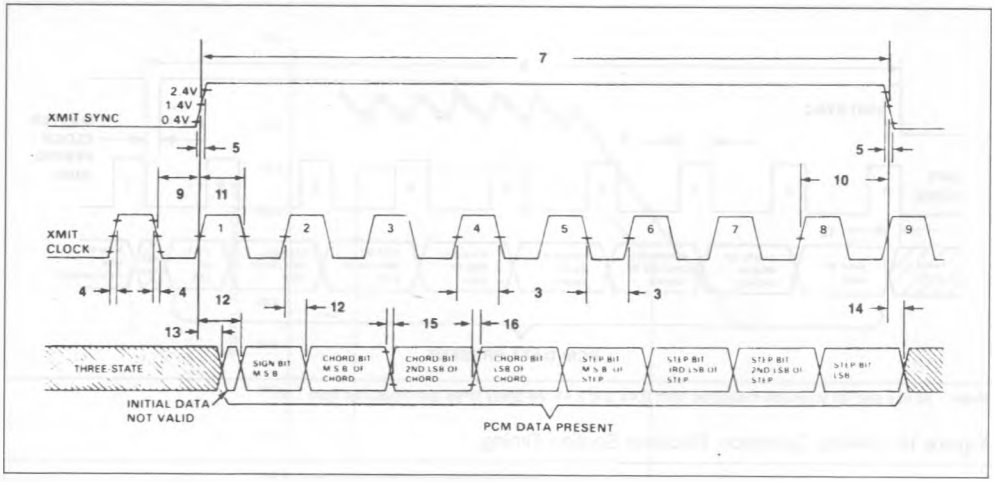
Figure 6 : Recommended Analog Input Circuit.



TIMING SPECIFICATIONS (refer to figures 7 and 8)

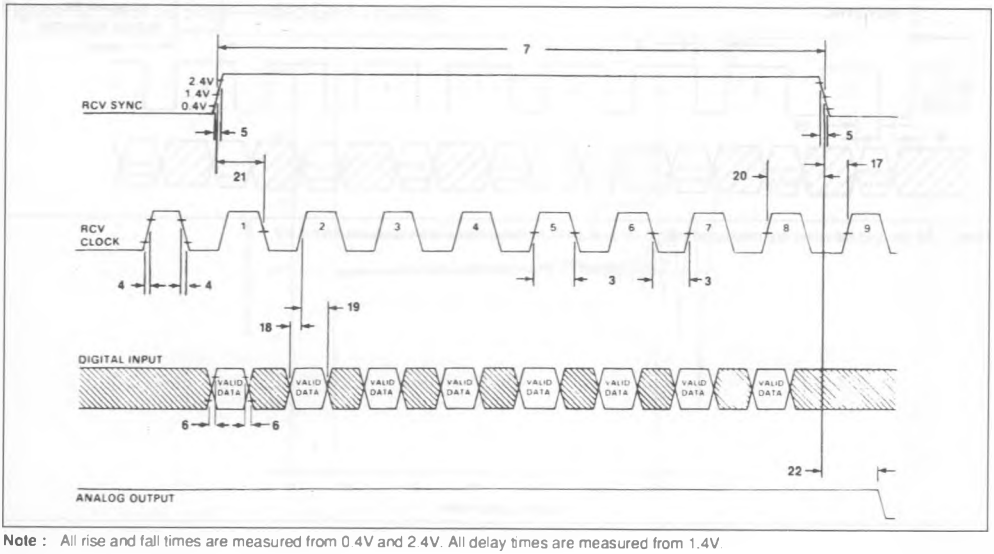
#	Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
1	F_M	Master Clock Frequency	1.5	2.048	2.1	MHz	
2	F_R, F_X	XMIT, RCV Clock Frequency	0.064	2.048	2.1	MHz	
3	PW_{CLK}	Clock Pulse Width (MASTER, XMIT, RCV)	200			ns	
4	t_{RC}, t_{FC}	Clock Rise, Fall Time (MASTER, XMIT, RCV)			25% of PW_{CLK}	ns	
5	t_{RS}, t_{FS}	Sync Rise, Fall Time (XMIT, RCV)			25% of PW_{CLK}	ns	
6	t_{DIR}, t_{DIF}	Data Input Rise, Fall Time			25% of PW_{CLK}	ns	
7	t_{WSX}, t_{WSR}	Sync Pulse Width (XMIT RCV)		$\frac{8}{F_X(F_R)}$		µs	
8	t_{PS}	Sync Pulse Period (XMIT, RCV)		125		µs	
9	t_{XCS}	XMIT Clock-to-XMIT Sync Delay	50% of t_{FC} (t_{RS})			ns	6
10	t_{XCSN}	XMIT Clock-toXMIT Sync (negative edge) Delay	200			ns	
11	t_{XSS}	XMIT Sync Set-up Time	200			ns	
12	t_{XDD}	XMIT Data Delay	0		200	ns	4
13	t_{XDP}	XMIT Data Present	0		200	ns	4
14	t_{XDT}	XMIT Data Three State			150	ns	4
15	t_{DOF}	Digital Output Fall Time		50	100	ns	4
16	t_{DOR}	Digital Output Rise Time		50	100	ns	4
17	t_{SRC}	RVC Sync-to-RCV Clock Delay	50% of t_{RC} (t_{FS})			ns	6
18	t_{RDS}	RCV Data Set-up Time	50			ns	7
19	t_{RDH}	RCV Data Hold Time	200			ns	7
20	t_{RCS}	RCV Clock-to-RCV Sync Delay	200			ns	
21	t_{RSS}	RCV Sync Set-up Time	200			ns	7
22	t_{SAO}	RCV Sync-to-analog Output Delay		7		µs	
23	SLEW+	Analog Output Positive Slew Rate		1		V/µs	
24	SLEW–	Analog Output Negative Slew Rate		1		V/µs	
25	DROOP	Analog Output Droop Rate		25		µV/µs	

Figure 7 : Transmitter Section Timing.



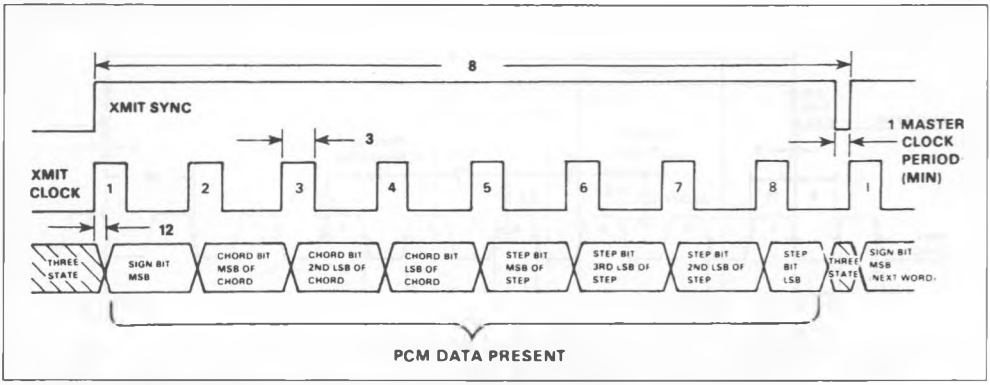
Note : All rise and fall times are measured from 0.4V and 2.4V. All delay times are measured from 1.4V.

Figure 8 : Receiver Section Timing.



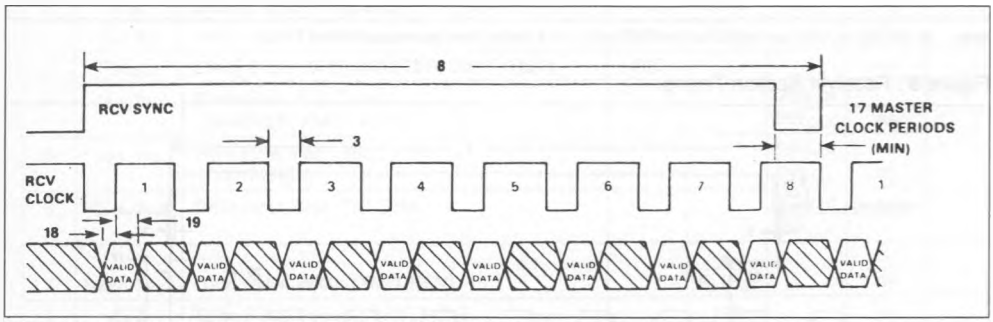
Note : All rise and fall times are measured from 0.4V and 2.4V. All delay times are measured from 1.4V.

Figure 9 : 64kHz Operation, Transmitter Section Timing.



Note : All rise and fall times are measured from 0.4V and 2.4V. All delay times are measured from 1.4V.

Figure 10 : 64kHz Operation, Receiver Section Timing.



Note : All rise and fall times are measured from 0.4V and 2.4V. All delay times are measured from 1.4V.

Figure 11 : M5156 Single-ended Signal to Distortion.

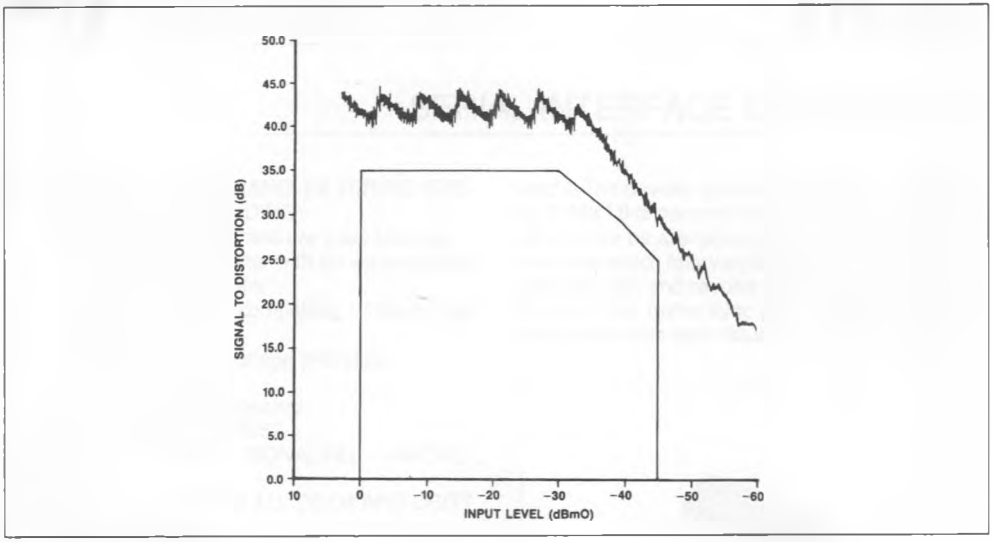


Figure 12 : M5156 Single-ended Gain Tracking.