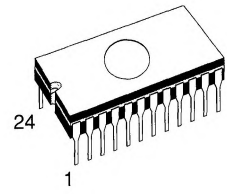
SGS-THOMSON MICROELECTRONICS

M2732A

32K (4K x 8) NMOS UV EPROM

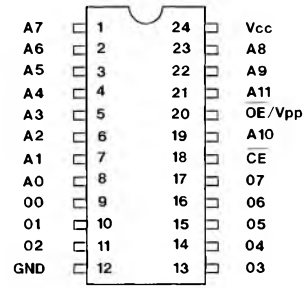
- FAST ACCESS TIME : 200 ns.
- 0 TO + 70 °C STANDARD TEMPERATURE RANGE.
- – 40 TO + 85 °C EXTENDED TEMPERATURE RANGE.
- SINGLE + 5V POWER SUPPLY.
- LOW STANDBY CURRENT (35mA MAX).
- INPUTS AND OUTPUTS TTL COMPATIBLE DURING READ AND PROGRAM.
- COMPLETELY STATIC.
- 21V PROGRAMMING VOLTAGE.



FDIP-24

(Ordering information at the end of the datasheet)

Figure 1 : Pin Connection



VR000654

DESCRIPTION

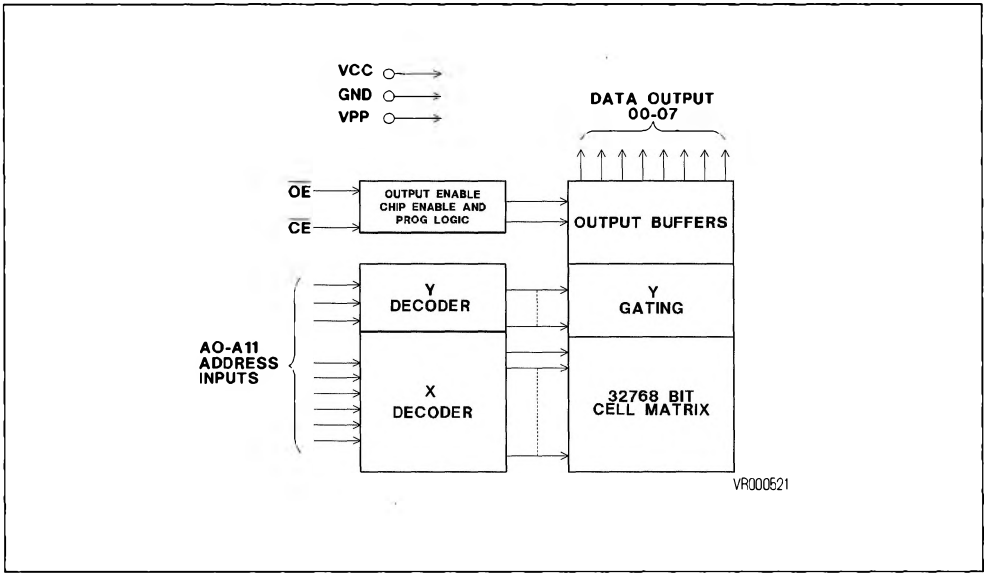
The M2732A is a 32,768-bits ultraviolet erasable and electrically programmable read-only memory (EPROM). It is organized as 4,096 words by 8 bits. The M2732A with its single + 5V power supply and with an access time of 200 ns, is ideal for use with the high performance + 5V microprocessors such as the Z8*, Z80* and Z8000*.

The M2732A is available in a 24-lead dual in-line ceramic package glass lens (Frit-Seal).

PIN FUNCTIONS

A0-A11	ADDRESS INPUT
$\overline{CE}$	CHIP ENABLE INPUT
$\overline{OE}$	OUTPUT ENABLE INPUT
O0-O7	DATA INPUT/OUTPUT

Figure 2 : Block Diagram



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameters	Values	Units
V_I	All input or Output voltages with respect to ground	+6 to -0.6	V
V_{PP}	Supply voltage with respect to ground	+22 to -0.6	V
T_{AMB}	Ambient temperature under bias F1/-2F1/-3F1/-4F1 F6/4F6	-10 to +80 -50 to +95	°C °C
T_{STG}	Storage temperature range	-65 to +125	°C

NOTE : Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

OPERATING MODES

MODE	PINS			
	$\overline{CE}$ (18)	$\overline{OE}/V_{PP}$ (20)	V_{CC} (24)	OUPUTS (9-11, 13-17)
READ	V_{IL}	V_{IL}	+ 5	D_{OUT}
STANDBY	V_{IH}	Dont't Care	+ 5	HIGH Z
PROGRAM	V_{IL}	V_{PP}	+ 5	D_{IN}
PROGRAM VERIFY	V_{IL}	V_{IL}	+ 5	D_{OUT}
PROGRAM INHIBIT	V_{IH}	V_{PP}	+ 5	HIGH Z

READ OPERATION

DC AND AC CONDITIONS

SELECTION CODE	F1	F6
Operating Temperature Range	0 to 70°C	-40 to 85°C
SELECTION CODE (Example for 0°C to 70°C Oper. Temp. Range)	**2F1, F1, 3F1, 4F1**	**20F1, 25F1, 30F1, 45F1**
V_{CC} Power Supply (1)	5V ± 5%	5V ± 10%

DC AND OPERATING CHARACTERISTICS

Symbol	Parameter	Test Condition	Values			Unit
			Min	Typ (3)	Max	
I_{LI}	Input Leakage Current	V_{IN} = 5.5V			10	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V			10	µA
I_{CC1} (2)	V_{CC} Current Standby	$\overline{CE}$ = V_{IH} $\overline{OE}$ = V_{IL}			35	mA
I_{CC2} (3)	V_{CC} Current Active	$\overline{CE}$ = $\overline{OE}$ = V_{IL}		70	125	mA
V_{IL}	Input low voltage		-0.1		+0.8	V
V_{IH}	Input high voltage		2.0		V_{CC}+ 1	V
V_{OL}	Output Low voltage	I_{OL} = 2.1 mA			0.45	V
V_{OH}	Output high voltage	I_{OH} = -400 µA	2.4			V

AC CHARACTERISTICS

Symbol	Parameter	Test Condition	2732A-2 2732A-20		2732A 2732A-25		2732A-3 2732A-30		2732A-4 2732A-45		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE}$=$\overline{OE}$=V_{IL}		200		250		300		450	ns
t_{CE}	$\overline{CE}$ to Output delay	$\overline{OE}$=V_{IL}		200		250		300		450	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE}$=V_{IL}		100		100		150		150	ns
t_{DF} (4)	$\overline{OE}$ High to Output float	$\overline{CE}$=V_{IL}	0	60	0	60	0	130	0	130	ns
t_{OH}	Output hold from address, $\overline{CE}$ or $\overline{OE}$ whichever occured first	$\overline{CE}$=$\overline{OE}$=V_{IL}	0		0		0		0		ns

CAPACITANCE(4)

(T_{AMB} = 25°C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
C_{IN1}	Input Capacitance except $\overline{OE}$/V_{PP}	V_{IN} = 0V		4	6	pF
C_{IN2}	$\overline{OE}$/V_{PP} Input Capacitance	V_{IN} = 0V			20	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		8	12	pF

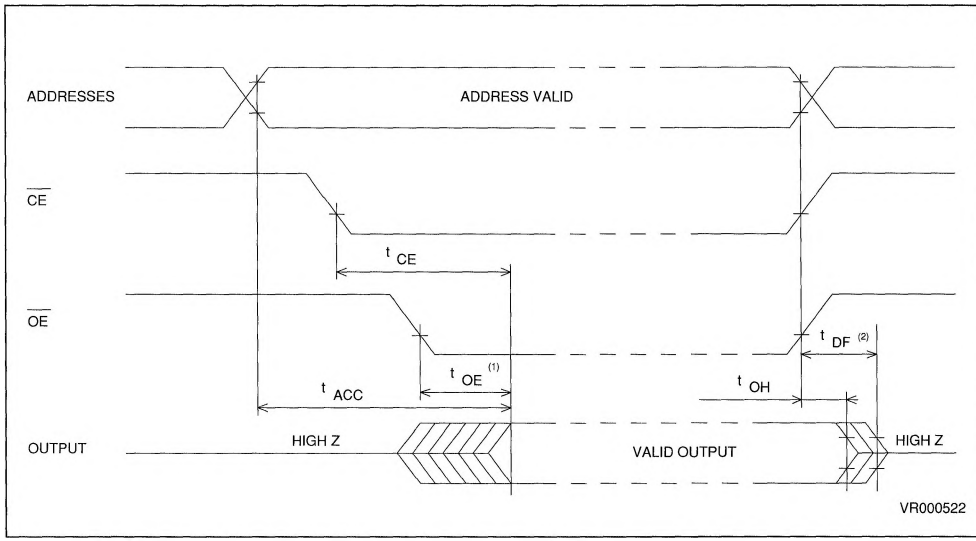
NOTES :
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. V_{PP} may be connected directly to V_{CC} except during programming. The supply current would then be the sum of I_{CC} and I_{PP1}.
3. Typical values are for T_{AMB} = 25°C and nominal supply voltages.
4. This parameter is only sampled and not 100 % tested.

READ OPERATION (Continued)

AC TEST CONDITIONS

Input Rise and Fall Times	:	≤ 20 ns	Timing Measurement Reference Levels :
Input Pulse Levels	:	0.45 to 2.4V	Inputs : 0.8 and 2V - Outputs : 0.8 and 2V

Figure 3 : AC Waveforms



NOTES : 1. $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge $\overline{CE}$ without impact on t_{ACC}.
2. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first.

READ MODE

The M2732A has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection.

Assuming that the addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output ($t_{\overline{CE}}$). Data is available at the outputs after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and the addresses have been stable for at least t_{ACC}-t_{OE}.

STANDBY MODE

The M2732A has a standby mode which reduces the active power current by 70 %, from 125 mA to 35 mA. The M2732A is placed in the standby mode by applying a TTL high signal to $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

TWO LINE OUTPUT CONTROL

Because M2732A's are usually used in larger memory arrays, this product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows :

a) the lowest possible memory power dissipation,

b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{CE}$ be decoded and used as the primary device selecting function, while $\overline{OE}$ should be made a common connection to all devices in the array and connected to the READ line from the system control bus.

This ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is required from a particular memory device.

PROGRAMMING OPERATION

(T_{AMB} = 25°C ± 5°C, V_{CC}[2] = 5 V ± 5 %, V_{PP}[2, 3] = 21 V± 0.5 V)

DC AND OPERATING CHARACTERISTICS

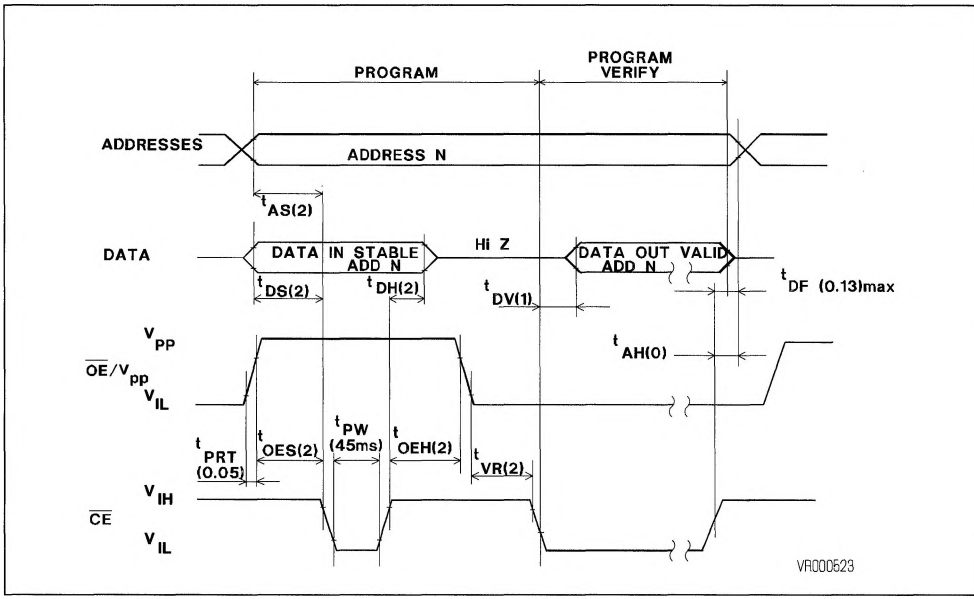
Symbol	Parameter	Test Condition (see note 1)	Values			Unit
			Min	Typ	Max	
I_{LI}	Input Current (All Inputs)	V_{IN} = V_{IL} or V_{IH}			10	µA
V_{IL}	Input Low Level		-0.1		0.8	V
V_{IH}	Input High Level		2.0		V_{CC}+1	V
V_{OL}	Output Low Voltage During Verify	I_{OL} = 2.1 mA			0.45	V
V_{OH}	Output High Voltage During Verify	I_{OH} = -400µA	2.4			V
I_{CC2}	V_{CC} Supply Current (Verify)			70	125	mA
I_{PP}	V_{PP} Supply Current	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{PP}			30	mA

AC CHARACTERISTICS

Symbol	Parameter	Test Condition (see note 1)	Values			Unit
			Min	Typ	Max	
t_{AS}	Address Setup Time		2			µs
t_{OES}	$\overline{OE}$ Setup Time		2			µs
t_{DS}	Data Setup Time		2			µs
t_{AH}	Address Hold Time		0			µs
t_{DH}	Data Hold Time		2			µs
t_{DF}	Chip Enable to Output Float Delay		0		130	ns
t_{DV}	Data valid from $\overline{CE}$	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IL}			1	µs
t_{PW}	$\overline{CE}$ Pulse Width During Programming		45	50	55	ms
t_{PRT}	$\overline{CE}$ Pulse rise time During Programming		50			ns
t_{VR}	V_{PP} recovery time		2			µs

NOTES :
1. Product is guaranteed only if programmed within described specifications.
2. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously with or after V_{PP}. The M2732A must not be inserted into or removed from a board with V_{PP} at 21 ± 0.5V. Otherwise damage may occur to the device.
3. The maximum allowable voltage which may be applied to the V_{PP} pin during programming is +22V. Care must be taken when switching the V_{PP} supply to prevent overshoot exceeding this 22V maximum specification.

Figure 4 : Programming Waveforms



NOTES : 1. All times shown in ( ) are minimum and in µsec unless otherwise specified.
2. The input timing reference level is 0.8V for a V_{IL} and 2V for a V_{IH}.
3. t_{OE} and t_{DFF} are characteristics of the device but must be accommodated by the programmer.

PROGRAMMING

Caution : Exceeding 22V on pin (V_{PP}) will damage the M2732A.

When delivered, and after each erasure, all bits of the M2732A are in the "1" state. Data is introduced by selectively programming "0's" into the desired bit locations. Although only "0's" will be programmed, both "1's" and "0's" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The M2732A is in the programming mode when the $\overline{OE}/V_{PP}$ input is at 21V. A 0.1µF capacitor must be placed across $\overline{OE}/V_{PP}$ and ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied, 8 bits in parallel, to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, a 50 msec, active low, TTL program pulse is applied to the $\overline{CE}$ input. A program pulse must be applied at each address location to be programmed. Any location can be programmed at any time - either individually, sequentially, or at random. The program pulse has a maximum width of 55 msec. The 2732A must not be programmed with a DC signal applied to the $\overline{CE}$ input.

Programming of multiple 2732As in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled M2732As may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{CE}$ input programs the paralleled 2732As.

PROGRAM INHIBIT

Programming of multiple 2732As in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs (including $\overline{OE}/V_{PP}$) of the parallel 2732As may be common. A TTL level program pulse applied to a 2732A's $\overline{CE}$ input with $\overline{OE}/V_{PP}$ at 21V will program that 2732A. A high level $\overline{CE}$ input inhibits the other 2732As from being programmed.

PROGRAM VERIFY

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify is curried out with $\overline{OE}/V_{PP}$ and $\overline{CE}$ at V_{IL}.

ERASURE OPERATION

The erasure characteristics of the M2732A are such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000 Å. It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000-4000 Å range. Research shows that constant exposure to room level fluorescent lighting could erase a typical M2732A in approximately 3 years, while it would take approximately 1 week to cause erasure when exposed to the direct sunlight. If the M2732A is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque labels be put over the M2732A window to prevent unintentional erasure.

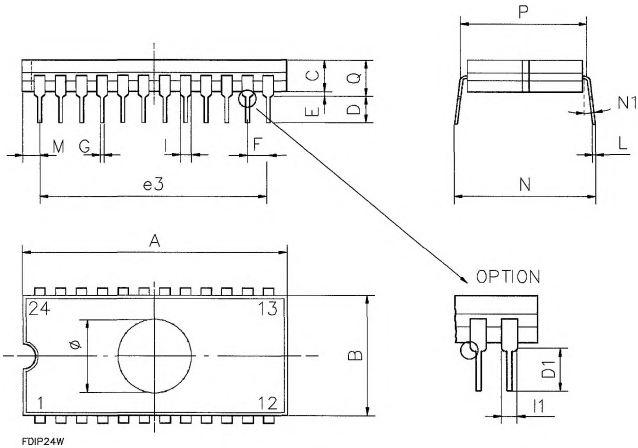
The recommended erasure procedure for the M2732A is exposure to shortwave ultraviolet light which has a wavelength of 2537 Å. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 μW/cm^2 power rating. The M2732A should be placed within 2.5 cm of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure.

ORDERING INFORMATION

Part Number	Access Time	Supply Voltage	Temp. Range	Package
M2732A-2F1	200 ns	5 V ± 5%	0 to + 70°C	FDIP24-W
M2732AF1	250 ns	5 V ± 5%	0 to + 70°C	FDIP24-W
M2732A-3F1	300 ns	5 V ± 5%	0 to + 70°C	FDIP24-W
M2732A-4F1	450 ns	5 V ± 5%	0 to + 70°C	FDIP24-W
M2732A-20F1	200 ns	5 V ± 10%	0 to + 70°C	FDIP24-W
M2732A-25F1	250 ns	5 V ± 10%	0 to + 70°C	FDIP24-W
M2732A-30F1	300 ns	5 V ± 10%	0 to + 70°C	FDIP24-W
M2732A-45F1	450 ns	5 V ± 10%	0 to + 70°C	FDIP24-W
M2732AF6	250 ns	5 V ± 5%	-40 to + 8 5°C	FDIP24-W
M2732A-4F1	450 ns	5 V ± 5 %	-40 to + 85°C	FDIP24-W

PACKAGE MECHANICAL DATA

Figure 5 : 24-PIN CERAMIC DIP BULL'S EYE



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			32.00			1.259
B	13.05		13.36	0.514		0.526
C	3.90		5.08	0.154		0.200
D	3.00			0.118		
D1	3.40			0.134		
E	0.50		1.78	0.020		0.070
e3		27.94			1.10	
F	2.29		2.79	0.090		0.110
G	0.40		0.55	0.016		0.022
I	1.17		1.42	0.046		0.056
I1	1.27		1.52	0.050		0.060
L	0.22		0.31	0.009		0.012
M	1.52		2.49	0.060		0.098
N						
N1	0°		10°	0°		10°
P	15.40		15.80	0.606		0.622
Q			5.71			0.225
Ø	6.86		7.36	0.270		0.290