LTC4211

# Hot Swap Controller with Multifunction Current Control

April 2001

## FEATURES

- **Allows Safe Board Insertion and Removal from a Live Backplane**
- **Controls Supply Voltages from 2.5V to 16.5V**
- **Programmable Soft-Start with Inrush Current Limiting, No External Gate Capacitor Required**
- **Faster Turn-Off Time Because No External Gate Capacitor is Required**
- **Dual Level Overcurrent Fault Protection**
- **Programmable Response Time for Overcurrent Protection (MS10)**
- **Programmable Overvoltage Protection (MS10)**
- **Automatic Retry or Latched Mode Operation (MS10)**
- High Side Drive for an External N-Channel FET
- User-Programmable Supply Voltage Power-Up Rate
- FB Pin Monitors $V_{OUT}$ and Signals $\overline{RESET}$
- Glitch Filter Protects Against Spurious $\overline{RESET}$ Signal

## APPLICATIONS

- Electronic Circuit Breaker
- Hot Board Insertion and Removal (Either On Backplane or On Removable Card)
- Industrial High Side Switch/Circuit Breaker

## DESCRIPTION

The LTC®4211 is a Hot Swap™ controller that allows a board to be safely inserted and removed from a live backplane. An internal high side switch driver controls the gate of an external N-channel MOSFET for supply voltages ranging from 2.5V to 16.5V. The LTC4211 provides soft-start and inrush current limiting during the programmable start-up period.

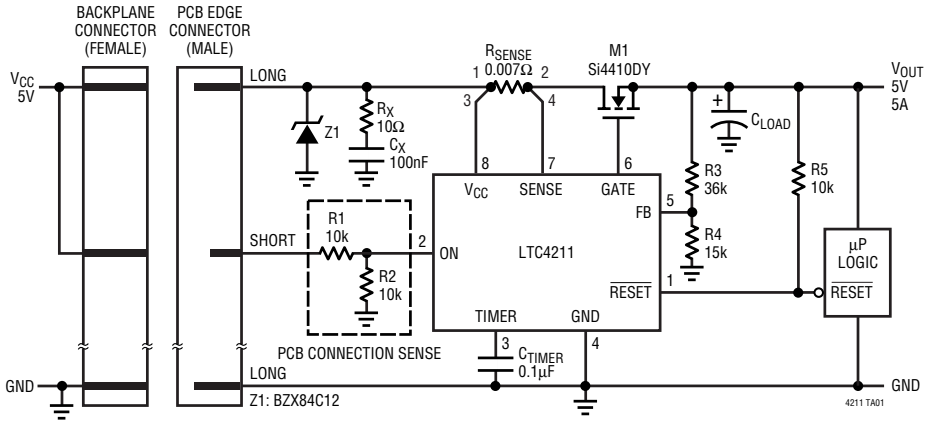
Two on-chip current limit comparators provide dual level overcurrent circuit breaker protection. The slow comparator trips at $V_{CC}$ – 50mV and activates in 20µs (or programmed by an external filter capacitor, MS10 only). The fast comparator trips at $V_{CC}$ – 150mV and typically responds in 300ns.

The FB pin monitors the output supply voltage and signals the $\overline{RESET}$ pin. The ON pin turns the chip on and off and can also be used for the reset function. The MS10 package has $\overline{FAULT}$ and FILTER pins to provide additional functions like fault indication, autoretry or latch-off modes, programmable current limit response time and programmable overvoltage protection using an external Zener diode clamp.

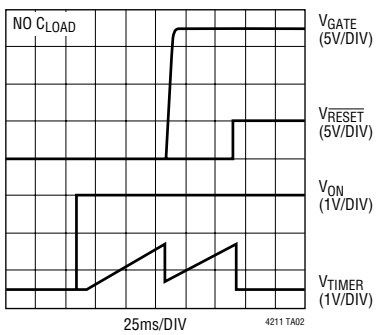


## TYPICAL APPLICATION

**Single Channel 5V Hot Swap Controller**




**Power-Up Sequence**

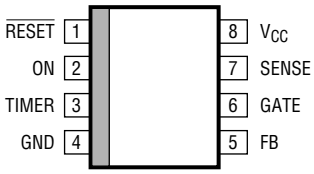


## ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage ($V_{CC}$) ..... 17V
Input Voltage
FB, ON ..... –0.3V to 17V
SENSE, FILTER ..... –0.3V to $V_{CC}$ + 0.3V
TIMER ..... –0.3V to 2V
Output Voltage
GATE ..... Internally Limited (Note 3)
$\overline{RESET}$, $\overline{FAULT}$ ..... –0.3V to 17V

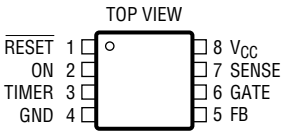
Operating Temperature Range
LTC4211C ..... 0°C to 70°C
LTC4211I ..... –45°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

## PACKAGE/ORDER INFORMATION



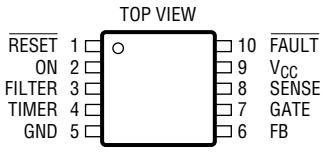

S8 PACKAGE
8-LEAD PLASTIC SO

$T_{JMAX}$ = 125°C, $\theta_{JA}$ = 150°C/W




MS8 PACKAGE
8-LEAD PLASTIC MSOP

$T_{JMAX}$ = 125°C, $\theta_{JA}$ = 200°C/W




MS10 PACKAGE
10-LEAD PLASTIC MSOP

$T_{JMAX}$ = 125°C, $\theta_{JA}$ = 200°C/W

| ORDER PART NUMBER | S8 PART MARKING | ORDER PART NUMBER | MS8 PART MARKING | ORDER PART NUMBER | MS10 PART MARKING |
|---|---|---|---|---|---|
| LTC4211CS8<br>LTC4211IS8 | 4211<br>4211I | LTC4211CMS8 | LTSC | LTC4211CMS | LTSU |

Consult factory for parts specified with wider operating temperature ranges.

## ELECTRICAL CHARACTERISTICS

**The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are $T_A$ = 25°C. $V_{CC}$ = 5V, (Note 2) unless otherwise noted.**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $V_{CC}$ | $V_{CC}$ Supply Voltage Range | | ● | 2.5 | | 16.5 | V |
| $I_{CC}$ | $V_{CC}$ Supply Current | FB = High, ON = High, TIMER = Low | ● | | 1 | 1.5 | mA |
| $V_{LKO}$ | Internal $V_{CC}$ Undervoltage Lockout | $V_{CC}$ Low-to-High Transition | ● | 2.13 | 2.3 | 2.47 | V |
| $V_{LKOHST}$ | $V_{CC}$ Undervoltage Lockout Hysteresis | | | | 120 | | mV |
| $I_{INFB}$ | FB Input Current | $V_{FB}$ = $V_{CC}$ or GND | | | ±1 | ±10 | µA |
| $I_{INON}$ | ON Input Current | $V_{ON}$ = $V_{CC}$ or GND | | | ±1 | ±10 | µA |
| $I_{INSENSE}$ | SENSE Input Current | $V_{SENSE}$ = $V_{CC}$ or GND | | | ±1 | ±10 | µA |
| $V_{CB(FAST)}$ | SENSE Trip Voltage ($V_{CC}$ – $V_{SENSE}$) | Fast Comparator Trips | ● | 130 | 150 | 170 | mV |
| $V_{CB(SLOW)}$ | SENSE Trip Voltage ($V_{CC}$ – $V_{SENSE}$) | Slow Comparator Trips | ● | 40 | 50 | 60 | mV |
| $I_{GATEUP}$ | GATE Pull-Up Current | Charge Pump On, $V_{GATE}$ ≤ 0.2V | ● | –12.5 | –10 | –7.5 | µA |
| $I_{GATEDOWN}$ | Normal GATE Pull-Down Current | ON Low | ● | 130 | 200 | 270 | µA |
| | Fast GATE Pull-Down Current | $\overline{FAULT}$ Latched and Circuit Breaker Tripped or in UVLO | | | 50 | | mA |

## ELECTRICAL CHARACTERISTICS

**The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are $T_A$ = 25°C. $V_{CC}$ = 5V, (Note 2) unless otherwise noted.**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $\Delta V_{GATE}$ | External N-Channel Gate Drive | $V_{GATE} - V_{CC}$ (For $V_{CC}$ = 2.5V) | ● | 4.0 | | 8 | V |
| | | $V_{GATE} - V_{CC}$ (For $V_{CC}$ = 2.7V) | ● | 4.5 | | 8 | V |
| | | $V_{GATE} - V_{CC}$ (For $V_{CC}$ = 3.3V) | ● | 5.0 | | 10 | V |
| | | $V_{GATE} - V_{CC}$ (For $V_{CC}$ = 5V) | ● | 10 | | 16 | V |
| | | $V_{GATE} - V_{CC}$ (For $V_{CC}$ = 12V) | ● | 10 | | 18 | V |
| | | $V_{GATE} - V_{CC}$ (For $V_{CC}$ = 15V) | ● | 8 | | 18 | V |
| $V_{GATEOV}$ | GATE Overvoltage Lockout Threshold | | ● | 0.08 | 0.2 | 0.3 | V |
| $V_{FB}$ | FB Voltage Threshold | | ● | 1.223 | 1.236 | 1.248 | V |
| $\Delta V_{FB}$ | FB Threshold Line Regulation | 2.5V ≤ $V_{CC}$ ≤ 16.5V | ● | | 0.5 | 5 | mV |
| $V_{FBHST}$ | FB Voltage Threshold Hysteresis | | | | 3 | | mV |
| $V_{ONHI}$ | ON Threshold High | | ● | 1.23 | 1.316 | 1.39 | V |
| $V_{ONLO}$ | ON Threshold Low | | ● | 1.20 | 1.236 | 1.26 | V |
| $V_{ONHST}$ | ON Hysteresis | | | | 80 | | mV |
| $I_{FILTER}$ | FILTER Current | During Slow Fault Condition | ● | –2.5 | –2 | –1.5 | µA |
| | | During Normal and Reset Conditions | ● | 7 | 10 | 13 | µA |
| $V_{FILTER}$ | FILTER Threshold | Latched Off Threshold, FILTER Low to High | ● | 1.20 | 1.236 | 1.26 | V |
| $V_{FILTERHST}$ | FILTER Threshold Hysteresis | FILTER High to Low | | | –80 | | mV |
| $I_{TMR}$ | TIMER Current | Timer On, GND ≤ $V_{TIMER}$ ≤ 1.5V | ● | –2.5 | –2 | –1.5 | µA |
| | | Timer Off, TIMER = 1.5V | | | 3 | | mA |
| $V_{TMR}$ | TIMER Threshold | TIMER Low to High | ● | 1.20 | 1.236 | 1.26 | V |
| | | TIMER High to Low | ● | 0.15 | 0.200 | 0.40 | V |
| $V_{TMRHST}$ | TIMER Threshold Hysteresis | (Note 4) | | | 40 | | mV |
| $V_{\overline{FAULT}}$ | $\overline{FAULT}$ Threshold | Latched Off Threshold, $\overline{FAULT}$ High to Low | ● | 1.20 | 1.236 | 1.26 | V |
| $V_{\overline{FAULT}HST}$ | $\overline{FAULT}$ Threshold Hysteresis | 2.5V ≤ $V_{CC}$ ≤ 16.5V, $\overline{FAULT}$ Low to High | | | 50 | | mV |
| $V_{OL\overline{FAULT}}$ | Output Low Voltage | $I_{\overline{FAULT}}$ = 1.6mA | ● | | 0.14 | 0.4 | V |
| $V_{OL\overline{RESET}}$ | Output Low Voltage | $I_{\overline{RESET}}$ = 1.6mA | ● | | 0.14 | 0.4 | V |
| $t_{\overline{FAULT}FC}$ | FAST COMP Trip to GATE Discharging | $V_{CB}$ = 0mV to 200mV Step | ● | | 300 | 700 | ns |
| $t_{\overline{FAULT}SC}$ | SLOW COMP Trip to GATE Discharging | $V_{CB}$ = 0mV to 100mV Step, 8-Pin Version or FILTER Floating | ● | 10 | 20 | 30 | µs |
| | | $V_{CB}$ = 0mV to 100mV Step, 10nF at FILTER Pin to GND | ● | 4 | 6 | 8 | ms |
| $t_{EXT\overline{FAULT}}$ | $\overline{FAULT}$ Low to GATE Discharging | $V_{\overline{FAULT}}$ = 5V to 0V | ● | 1 | 3 | 5 | µs |
| $t_{FILTER}$ | FILTER High to $\overline{FAULT}$ Latched | $V_{FILTER}$ = 0V to 5V | ● | 2 | 4.5 | 7 | µs |
| $t_{RESET}$ | Circuit Breaker Reset Delay Time | ON Goes Low to $\overline{FAULT}$ High | ● | | 150 | 250 | µs |
| $t_{OFF}$ | Turn-Off Time | ON Goes Low to Gate Off | | | 8 | | µs |

**Note 1:** Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

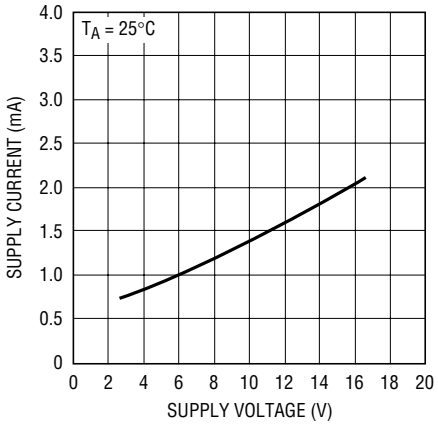
**Note 2:** All current into device pins are positive; all current out of device pins are negative; all voltages are referenced to ground unless otherwise specified.

**Note 3:** An internal Zener at the GATE pin clamps the charge pump voltage to a typical maximum operating voltage of 26V. External voltage applied to the GATE pin beyond the internal Zener voltage may damage the part. If a lower GATE pin voltage is desired, use an external Zener diode. The GATE capacitance must be <0.15µF at maximum $V_{CC}$.

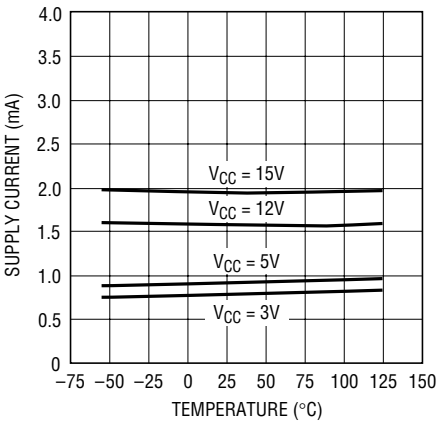
**Note 4:** Guaranteed by design.

# TYPICAL PERFORMANCE CHARACTERISTICS

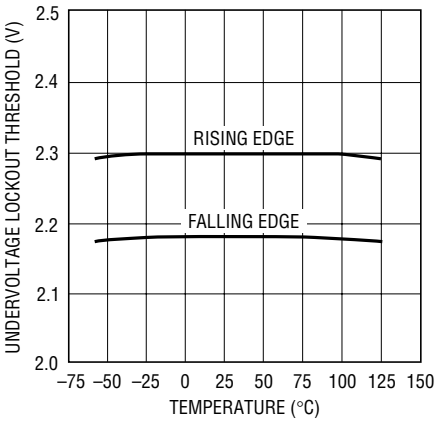
### Supply Current vs Supply Voltage



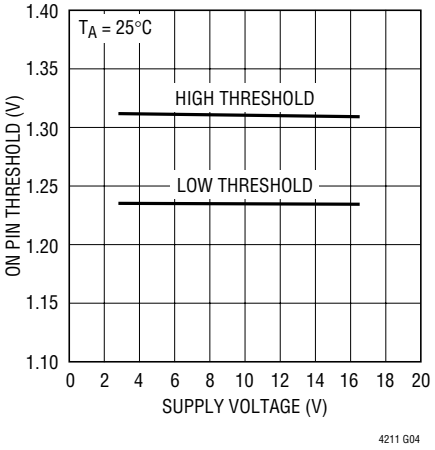

### Supply Current vs Temperature



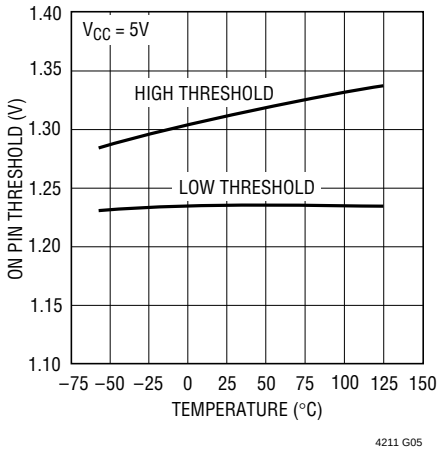

### Undervoltage Lockout Threshold vs Temperature



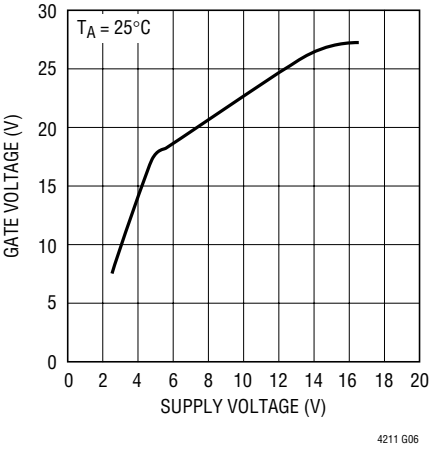

### ON Pin Threshold vs Supply Voltage



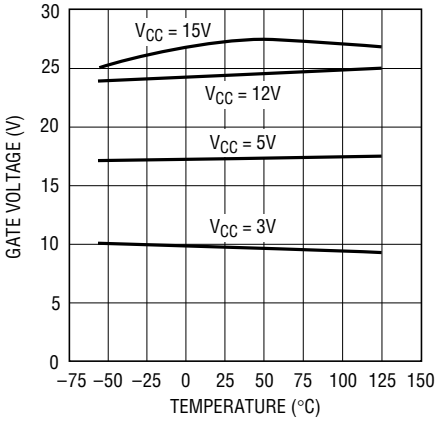

### ON Pin Threshold vs Temperature



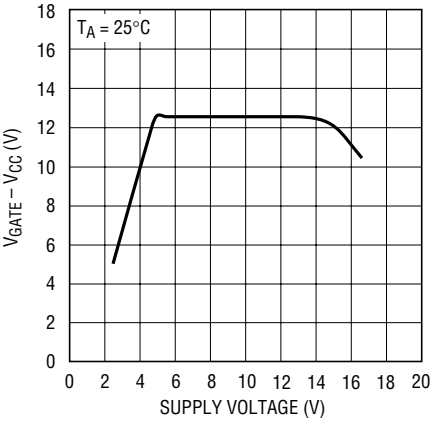

### GATE Voltage vs Supply Voltage



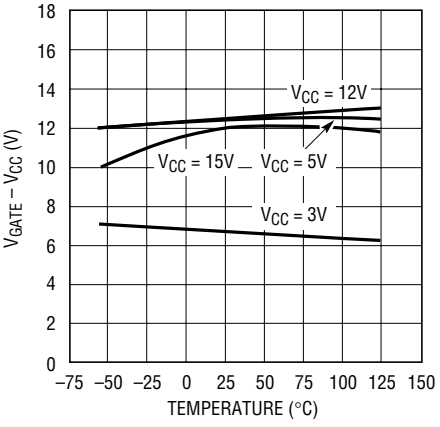

### GATE Voltage vs Temperature




### $V_{GATE} - V_{CC}$ vs Supply Voltage

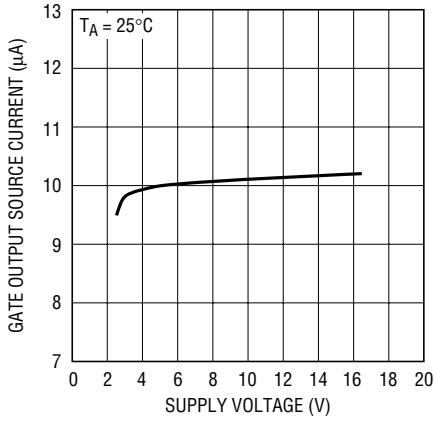



### $V_{GATE} - V_{CC}$ vs Temperature

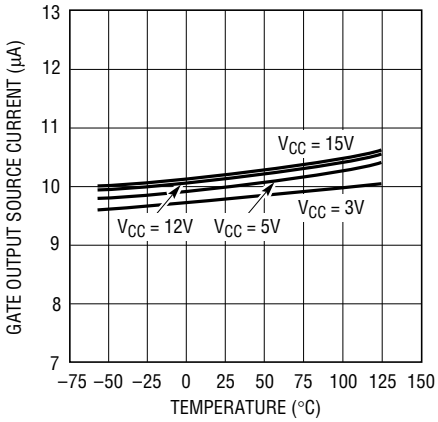


# TYPICAL PERFORMANCE CHARACTERISTICS

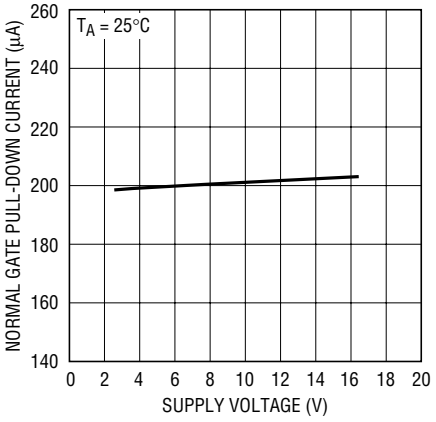
### GATE Output Source Current vs Supply Voltage



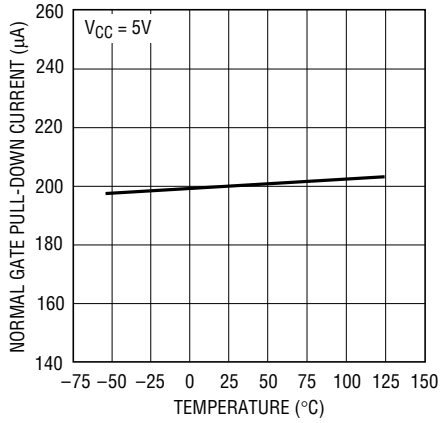

### GATE Output Source Current vs Temperature



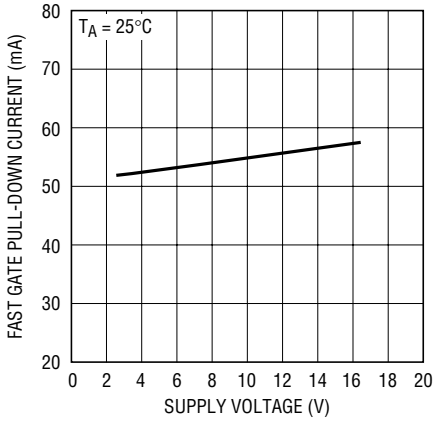

### Normal GATE Pull-Down Current vs Supply Voltage



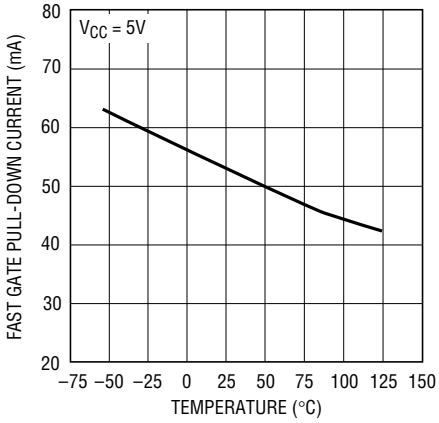

### Normal GATE Pull-Down Current vs Temperature



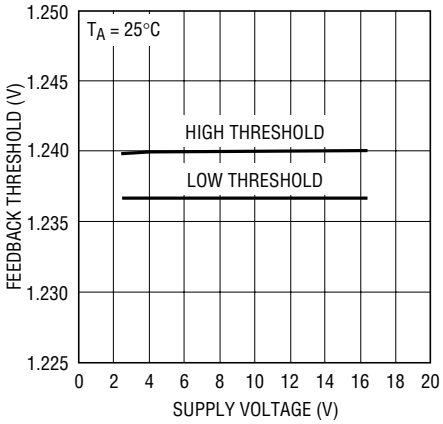

### Fast GATE Pull-Down Current vs Supply Voltage



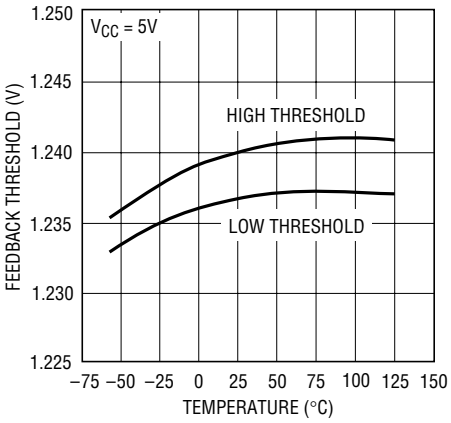

### Fast GATE Pull-Down Current vs Temperature



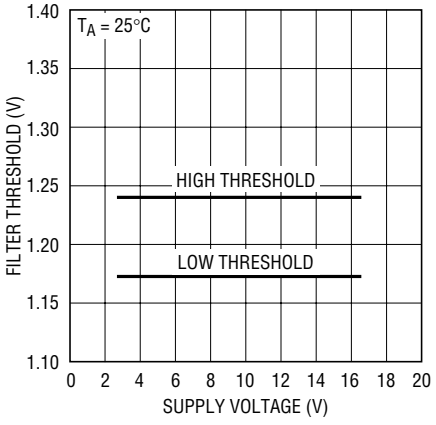

### Feedback Threshold vs Supply Voltage




### Feedback Threshold vs Temperature

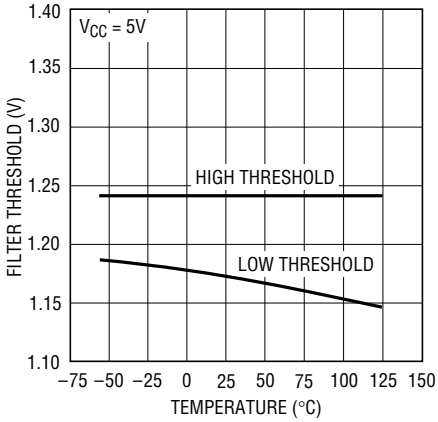



### FILTER Threshold vs Supply Voltage



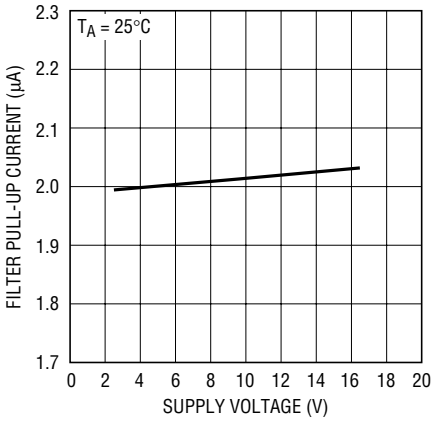
## TYPICAL PERFORMANCE CHARACTERISTICS

**FILTER Threshold vs Temperature**



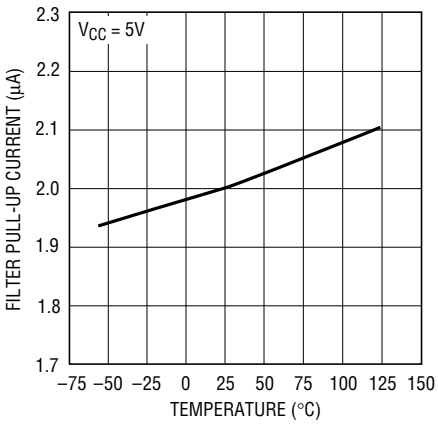

4211 G19

**FILTER Pull-Up Current vs Supply Voltage**



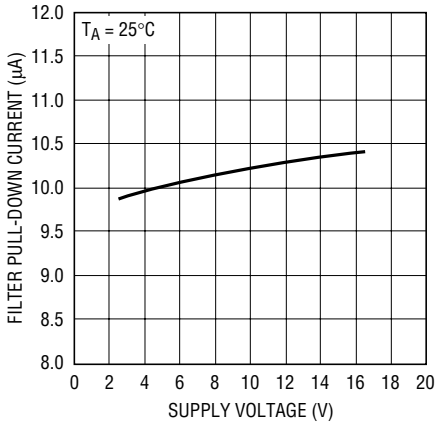

4211 G20

**FILTER Pull-Up Current vs Temperature**



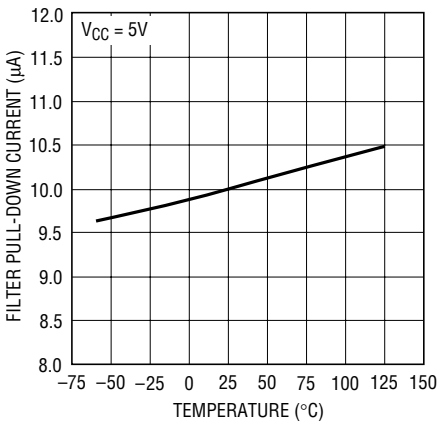

4211 G21

**FILTER Pull-Down Current vs Supply Voltage**



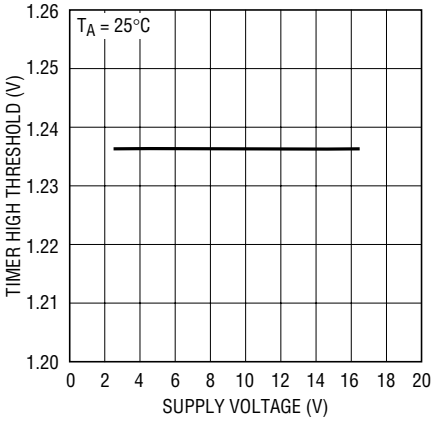

4211 G22

**FILTER Pull-Down Current vs Temperature**



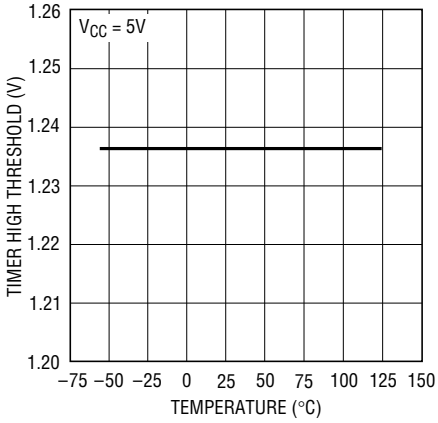

4211 G23

**TIMER High Threshold vs Supply Voltage**



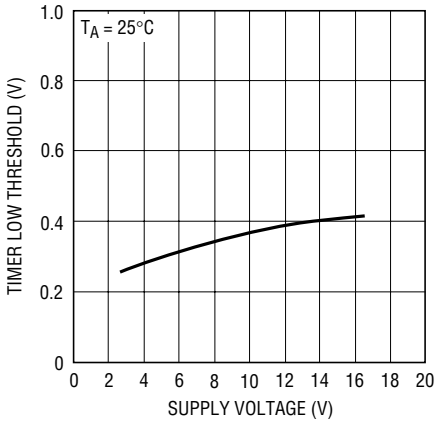

4211 G24

**TIMER High Threshold vs Temperature**



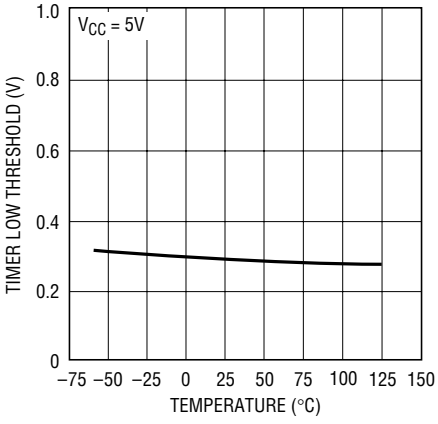

4211 G25

**TIMER Low Threshold vs Supply Voltage**




4211 G26

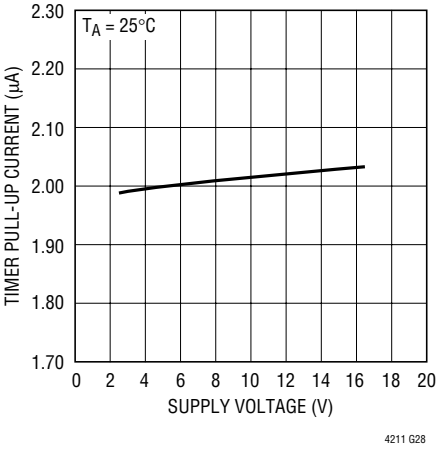
**TIMER Low Threshold vs Temperature**



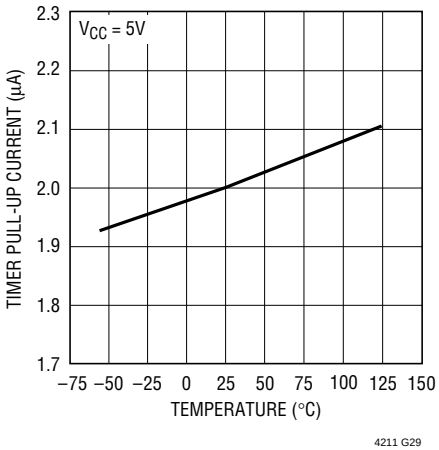

4211 G27

# TYPICAL PERFORMANCE CHARACTERISTICS

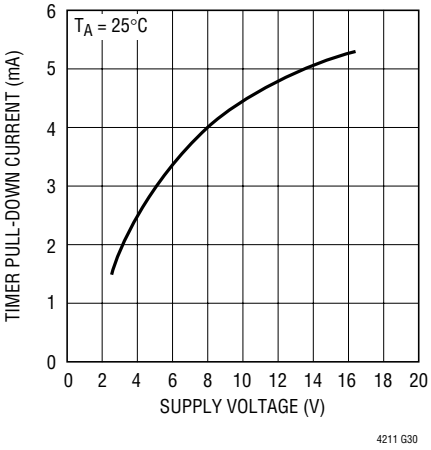
**TIMER Pull-Up Current vs Supply Voltage**



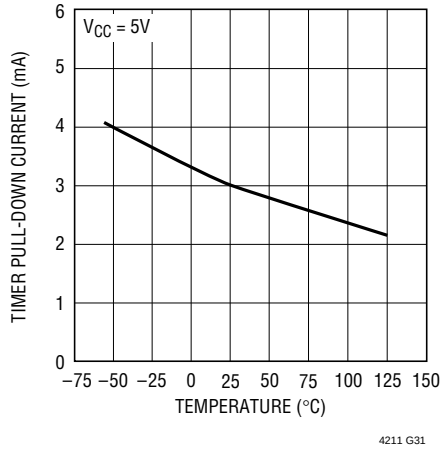

**TIMER Pull-Up Current vs Temperature**



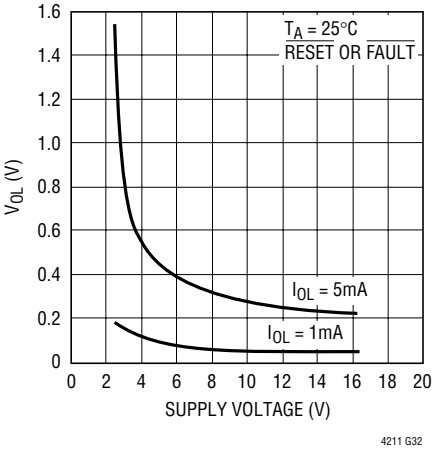

**TIMER Pull-Down Current vs Supply Voltage**



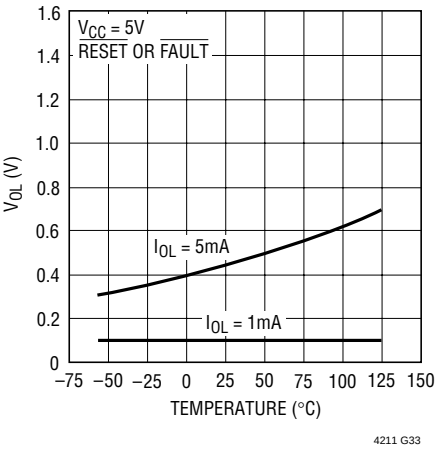

**TIMER Pull-Down Current vs Temperature**



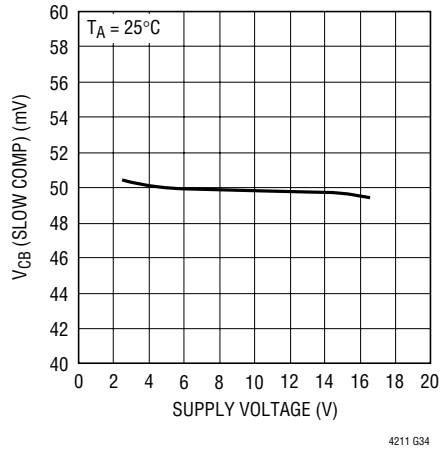

**$V_{OL}$ vs Supply Voltage**



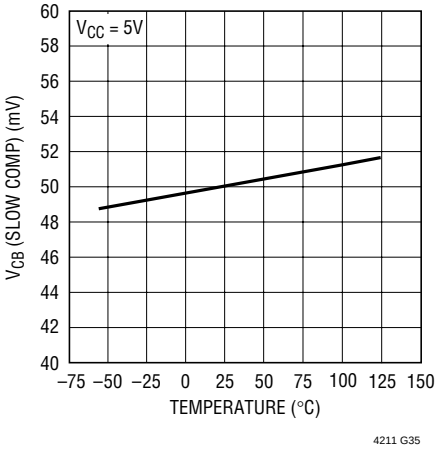

**$V_{OL}$ vs Temperature**



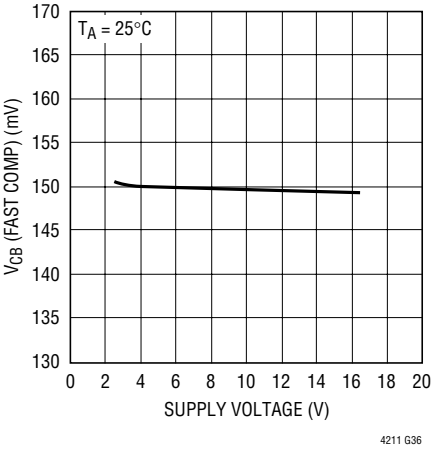

**$V_{CB}$ (SLOW COMP) vs Supply Voltage**




**$V_{CB}$ (SLOW COMP) vs Temperature**

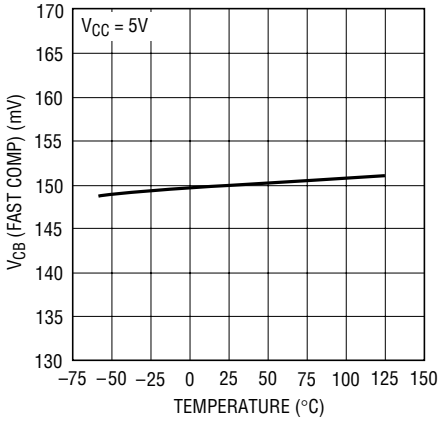



**$V_{CB}$ (FAST COMP) vs Supply Voltage**



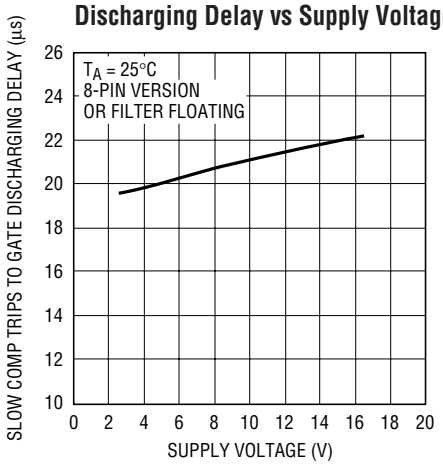
# TYPICAL PERFORMANCE CHARACTERISTICS

**$V_{CB}$ (FAST COMP) vs Temperature**



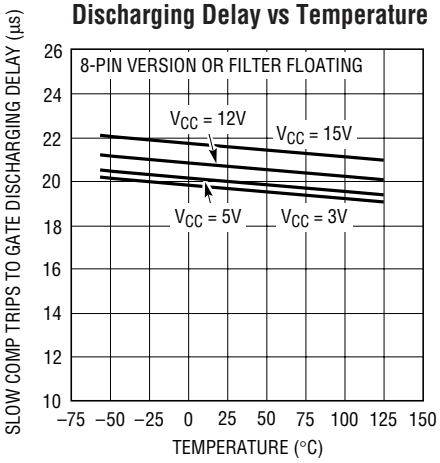

4211 G37

**SLOW COMP Trips to GATE Discharging Delay vs Supply Voltage**



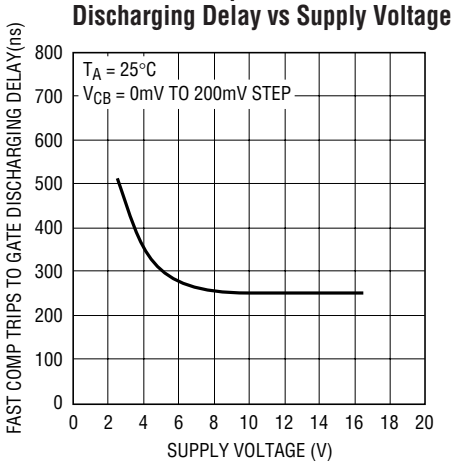

4211 G38

**SLOW COMP Trips to GATE Discharging Delay vs Temperature**



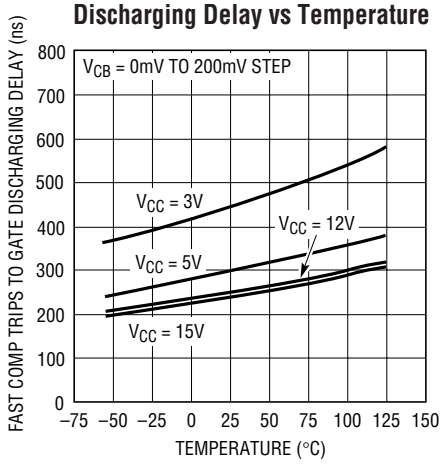

4211 G39

**FAST COMP Trips to GATE Discharging Delay vs Supply Voltage**



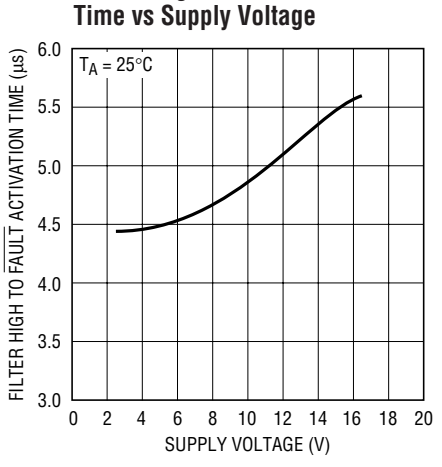

4211 G40

**FAST COMP Trips to GATE Discharging Delay vs Temperature**



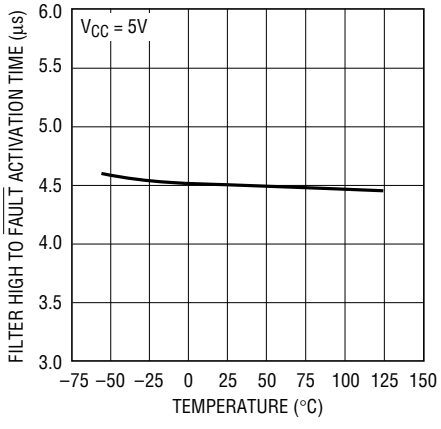

4211 G41

**FILTER High to $\overline{\text{FAULT}}$ Activation Time vs Supply Voltage**



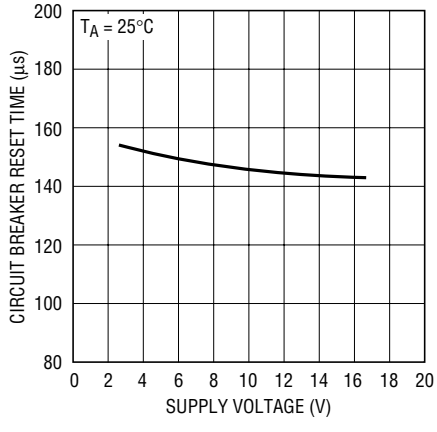

4211 G42

**FILTER High to $\overline{\text{FAULT}}$ Activation Time vs Temperature**



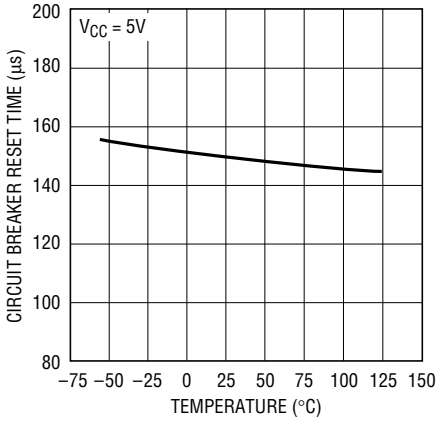

4211 G43

**Circuit Breaker RESET Time vs Supply Voltage**




4211 G44

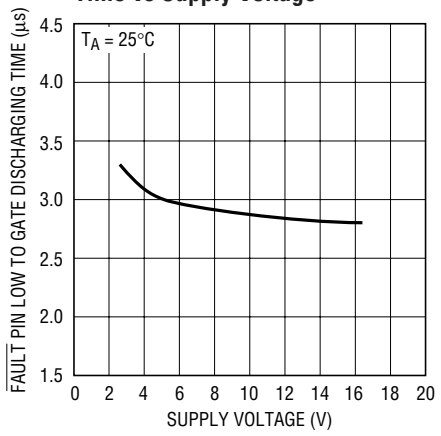
**Circuit Breaker RESET Time vs Temperature**



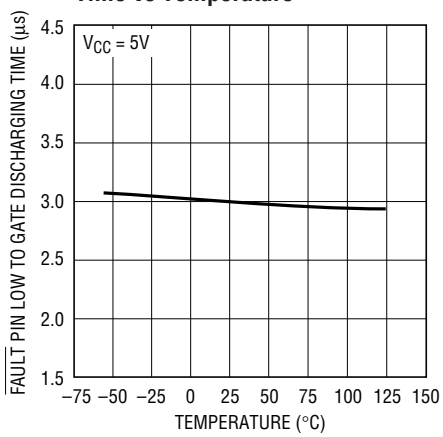

4211 G45

# TYPICAL PERFORMANCE CHARACTERISTICS

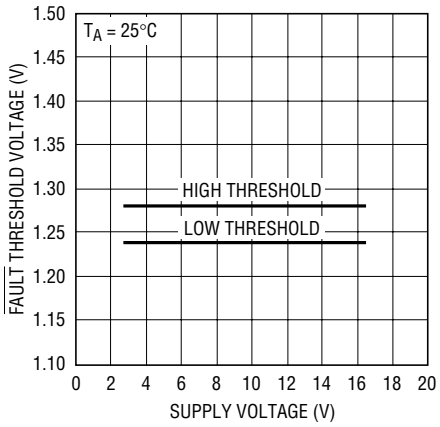
**$\overline{\text{FAULT}}$ Pin Low to GATE Discharging Time vs Supply Voltage**



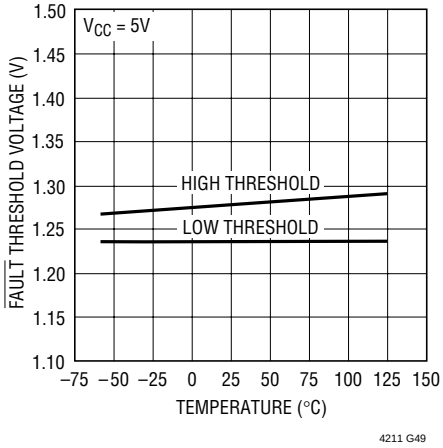

**$\overline{\text{FAULT}}$ Pin Low to GATE Discharging Time vs Temperature**



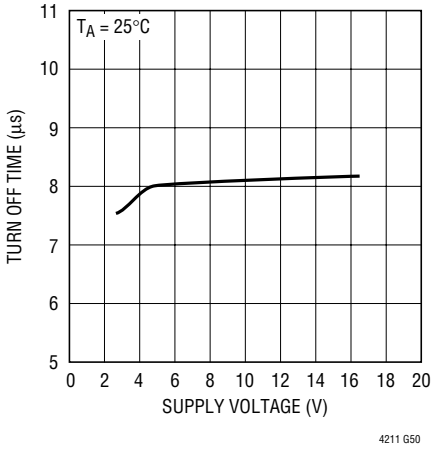

**$\overline{\text{FAULT}}$ Threshold Voltage vs Supply Voltage**



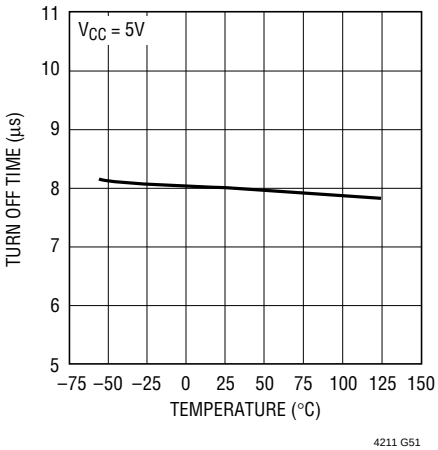

**$\overline{\text{FAULT}}$ Threshold Voltage vs Temperature**



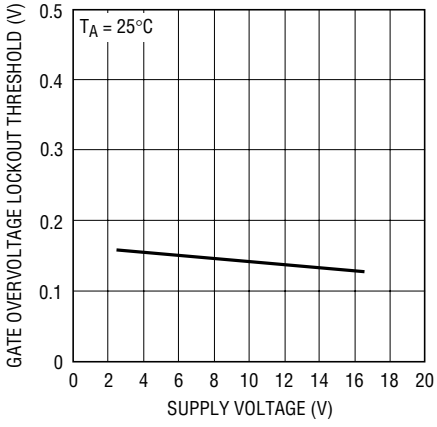

**Turn Off Time vs Supply Voltage**



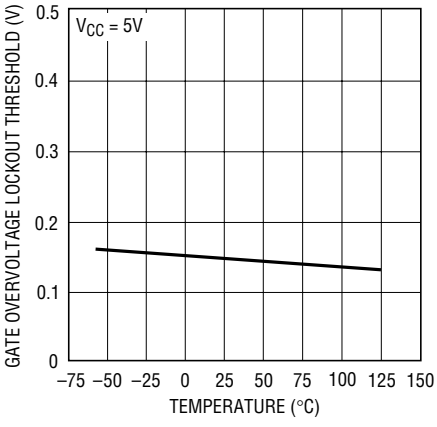

**Turn Off Time vs Temperature**




**GATE Overvoltage Lockout Threshold vs Supply Voltage**




**GATE Overvoltage Lockout Threshold vs Temperature**



## PIN FUNCTIONS (8-Lead Package/10-Lead Package)

**$\overline{\text{RESET}}$ (Pin 1/Pin 1):** An open-drain N-channel device whose source connects to GND (Pin 4/Pin 5). This pin pulls low if the voltage at the FB pin (Pin 5/Pin 6) falls below the FB pin threshold (1.236V). During the start-up cycle, the $\overline{\text{RESET}}$ pin goes high impedance at the end of the second timing cycle after the FB pin goes above the FB threshold. This pin requires an external pull-up resistor to $V_{CC}$. If an undervoltage lockout condition occurs, the $\overline{\text{RESET}}$ pin pulls low independently of the FB pin to prevent false glitches.

**ON (Pin 2/Pin 2):** An active high signal used to enable or disable LTC4211 operation. As shown in the LTC4211 Block Diagram, COMP1's threshold is set at 1.236V and its hysteresis is set at 80mV. If a logic high signal is applied to the ON pin ($V_{ON}$ > 1.316V), the first timing cycle begins if an overvoltage condition does not exist on the GATE pin (Pin 6/Pin 7). If a logic low signal is applied to the ON pin ($V_{ON}$ < 1.236V), the GATE pin is pulled low by an internal 200μA current sink. The ON pin can also be used to reset the electronic circuit breaker. If the ON pin is cycled low and then high following a circuit breaker trip, the internal circuit breaker is reset, and the LTC4211 begins a new start-up cycle.

**TIMER (Pin 3/Pin 4):** A capacitor connected from this pin to GND sets the LTC4211's system timing. The LTC4211's initial and second start-up timing cycles and its internal "power good" delay time are controlled by this capacitor.

**GND (Pin 4/Pin 5):** Device Ground Connection. Connect this pin to the system's analog ground plane.

**FB (Pin 5/Pin 6):** The FB (Feedback) pin is an input to the COMP2 comparator and monitors the output supply voltage through an external resistor divider. If $V_{FB}$ < 1.236V, the $\overline{\text{RESET}}$ pin pulls low. An internal glitch filter at COMP2's output helps prevent negative voltage transients from triggering a reset condition. If $V_{FB}$ > 1.239V, the $\overline{\text{RESET}}$ pin goes high after one timing cycle.

**GATE (Pin 6/Pin 7):** The output signal at this pin is the high side gate drive for the external N-channel FET pass transistor. An internal charge pump produces a 4V (minimum) to 18V (maximum) gate drive voltage for supply voltages from 2.5V to 16.5V, respectively.

As shown in the Block Diagram, an internal charge pump supplies a 10μA gate current and sufficient gate voltage drive to the external FET. The internal charge pump produces a minimum 4V gate drive for supplies in the range of 2.5V < $V_{CC}$ < 4.75V. For $V_{CC}$ > 4.75V, the minimum gate voltage drive is at least 10V. For $V_{CC}$ > 15V, the minimum gate voltage drive is 8V which is set by an internal Zener diode clamp connected between the GATE pin and GND.

**SENSE (Pin 7/Pin 8):** Circuit Breaker Set Pin. With a sense resistor placed in the power path between $V_{CC}$ and SENSE, the LTC4211's electronic circuit breaker trips if the voltage across the sense resistor exceeds the thresholds set internally for the SLOW COMP and the FAST COMP, as shown in the Block Diagram. The threshold for the SLOW COMP is $V_{CB(SLOW)}$ = 50mV, and the electronic circuit breaker trips if the voltage across the sense resistor exceeds 50mV for 20μs. The SLOW COMP delay is fixed in the S8/MS8 version and adjustable in the MS10 version of the LTC4211. To adjust the SLOW COMP's delay, please refer to the section on Adjusting SLOW COMP's Response Time.

Under transient conditions where large step current changes can and do occur over shorter periods of time, a second (fast) comparator instead trips the electronic circuit breaker. The threshold for the FAST COMP is set at $V_{CB(FAST)}$ = 150mV, and the circuit breaker trips if the voltage across the sense resistor exceeds 150mV for more than 300ns. The FAST COMP's delay is fixed in the LTC4211 and cannot be adjusted. To disable the electronic circuit breaker, connect the $V_{CC}$ and SENSE pins together.

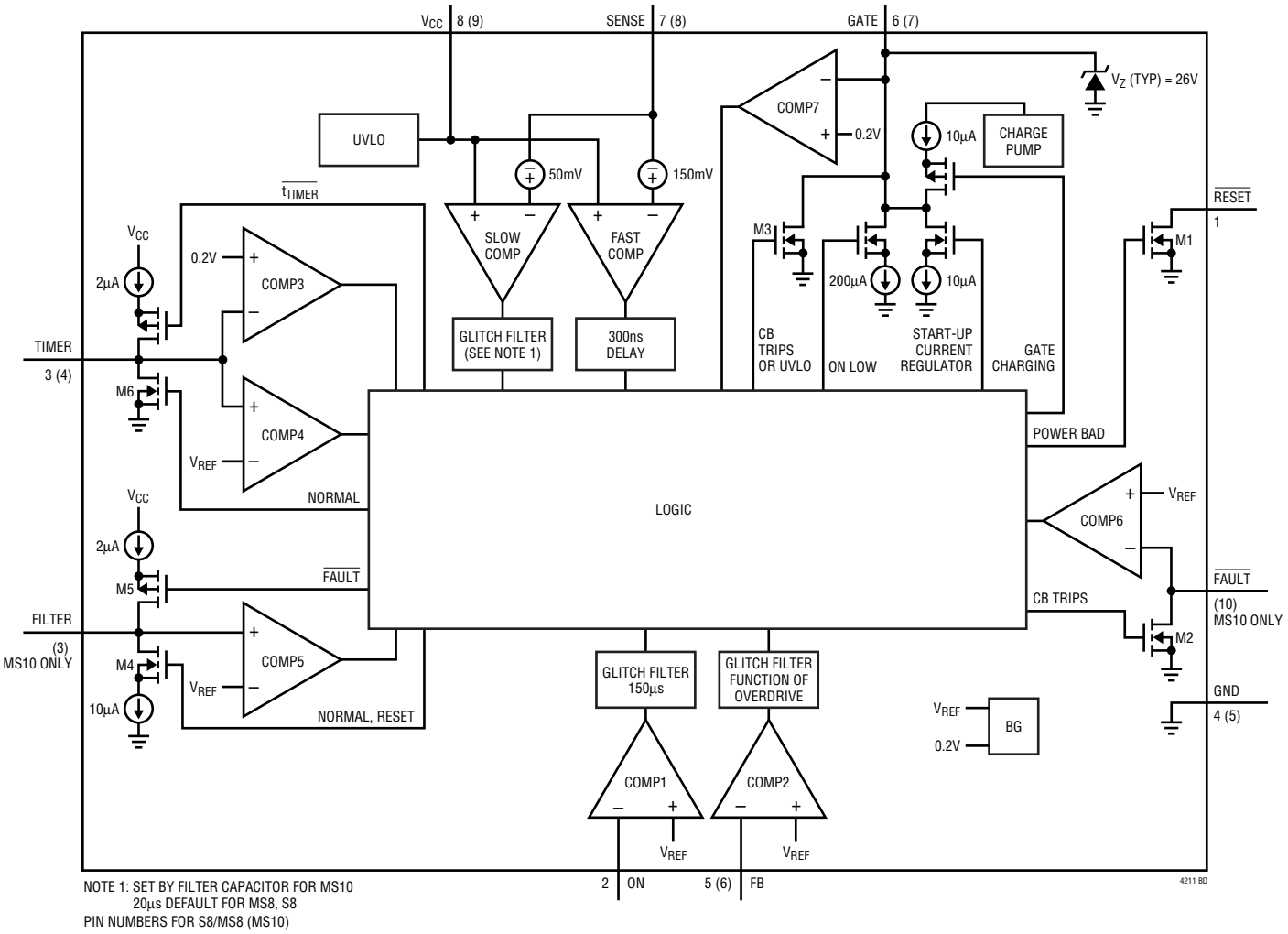
**$V_{CC}$ (Pin 8/Pin 9):** This is the positive supply input to the LTC4211. The LTC4211 operates from 2.5V < $V_{CC}$ < 16.5V, and the supply current is typically 1mA. An internal undervoltage lockout circuit disables the device until the voltage at $V_{CC}$ exceeds 2.3V.

## PIN FUNCTIONS (8-Lead Package/10-Lead Package)

**$\overline{\text{FAULT}}$ (Not available on S8/MS8, Pin 10 MS10):** $\overline{\text{FAULT}}$ is a dual function (an input and an output) internal to the LTC4211. Connected to this pin are an analog comparator (COMP6) and an open-drain N-channel FET. During normal operation, if COMP6 is driven below 1.236V, the electronic circuit breaker trips and the GATE pin pulls low. Typically, a 10k pull-up resistor connects to the $\overline{\text{FAULT}}$ pin. This allows the LTC4211 to begin a second timing cycle ($V_{\overline{\text{FAULT}}}$ > 1.286) and start-up properly. This also allows the use of the $\overline{\text{FAULT}}$ pin as a status output. Under normal operating conditions, the $\overline{\text{FAULT}}$ output is a logic high. Two conditions cause an active low on $\overline{\text{FAULT}}$: (1) the LTC4211's electronic circuit breaker trips because of an output short circuit ($V_{OUT}$ = 0V) or because of a fast output overcurrent transient (FAST COMP trips circuit breaker); or (2) $V_{FILTER}$ > 1.236V. The $\overline{\text{FAULT}}$ output is driven to logic low and is latched logic low until the ON pin is driven to logic low for 150µs (the $t_{RESET}$ duration).

**FILTER (Not available S8/MS8, Pin 3 MS10):** Overcurrent Fault Timing Pin and Overvoltage Fault Set pin. With a capacitor connected from this pin to ground, the SLOW COMP's response time can be adjusted. In the S8/MS8 version of the LTC4211, the FILTER pin is not available and the delay time from overcurrent detect to GATE OFF is fixed at 20µs.

## BLOCK DIAGRAM




NOTE 1: SET BY FILTER CAPACITOR FOR MS10
20µs DEFAULT FOR MS8, S8
PIN NUMBERS FOR S8/MS8 (MS10)

## OPERATION

### HOT CIRCUIT INSERTION

When circuit boards are inserted into or removed from live backplanes, the supply bypass capacitors can draw huge transient currents from the backplane power bus as they charge. The transient current can cause permanent damage to the connector pins as well as cause glitches on the system supply, causing other boards in the system to reset.

The LTC4211 is designed to turn a printed circuit board's supply voltages ON and OFF in a controlled manner, allowing the circuit board to be safely inserted or removed from a live backplane. The device provides a system reset signal to indicate when board supply voltage drops below a predetermined level, as well as a dual function fault monitor.

### OUTPUT VOLTAGE MONITOR

The LTC4211 uses a 1.236V bandgap reference, precision voltage comparator and an external resistor divider to monitor the output supply voltage as shown in Figure 1.

The operation of the supply monitor in normal mode is illustrated in Figure 2. When the supply voltage at the FB pin drops below its reset threshold (1.236V), the comparator COMP2 output goes high. After passing through a glitch filter, $\overline{\text{RESET}}$ is pulled low (Time Point N2). When the voltage at the FB pin rises above its reset threshold (1.239V), COMP2's output goes low and a timing cycle starts (Time Point N4). After a complete timing cycle, $\overline{\text{RESET}}$ is pulled high by the external pull-up resistor. If the FB pin rises above the reset threshold for less than a timing cycle, the $\overline{\text{RESET}}$ output remains low (Time Point N3).

As shown in Figure 5, the LTC4211's $\overline{\text{RESET}}$ pin is logic low during any undervoltage lockout condition and during the initial insertion of a PC board. Under normal operation, $\overline{\text{RESET}}$ goes to logic high at the end of the soft-start cycle only after the FB pin voltage rises above its reset threshold of 1.239V.

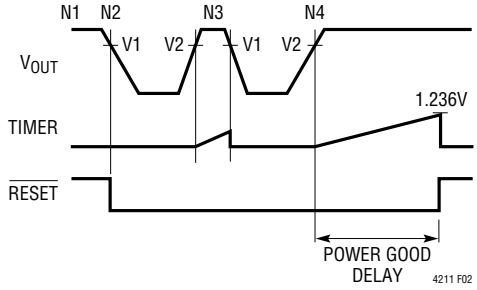



**Figure 2. Supply Monitor Waveforms in Normal Mode**

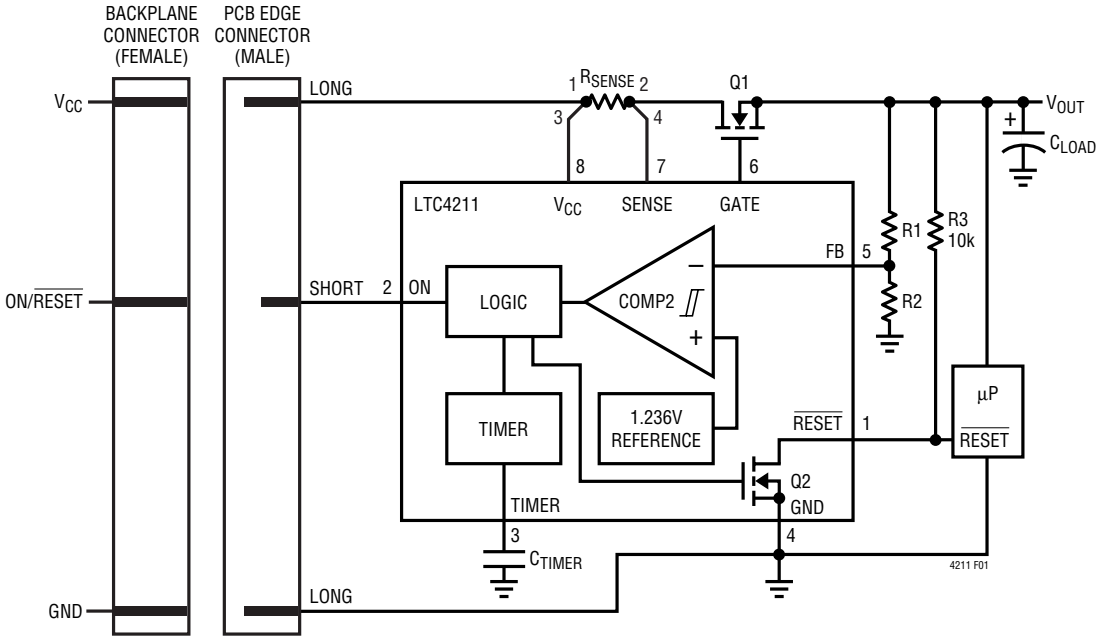



**Figure 1. Supply Voltage Monitor Block Diagram**

## OPERATION

### INTERNAL UNDERVOLTAGE LOCKOUT (UVLO)

The LTC4211's power-on reset circuit initializes the start-up condition and ensures the chip is in the proper state if the input supply voltage is too low. If the supply voltage falls below 2.18V, the LTC4211 is in undervoltage lockout (UVLO) mode, and the GATE pin is pulled low by an internal 200µA current source. Since the UVLO circuitry uses hysteresis, the chip restarts after the supply voltage rises above 2.3V and the ON pin goes high.

In addition, users can utilize the ON comparator (COMP1) or the $\overline{\text{FAULT}}$ comparator (COMP6) to effectively program a higher undervoltage lockout level. If the $\overline{\text{FAULT}}$ comparator is used for this purpose, the system will wait for the input voltage to increase above the level set by the user before starting the second timing cycle. Also, if the input voltage drops below the set level in normal operating mode, the user must cycle the ON pin or $V_{CC}$ to restart the system.

### GLITCH FILTER FOR $\overline{\text{RESET}}$

The LTC4211 has a glitch filter to prevent $\overline{\text{RESET}}$ from generating a system reset if there are transients on the FB pin. The relationship between glitch filter time and the feedback transient voltage is shown in Figure 3.

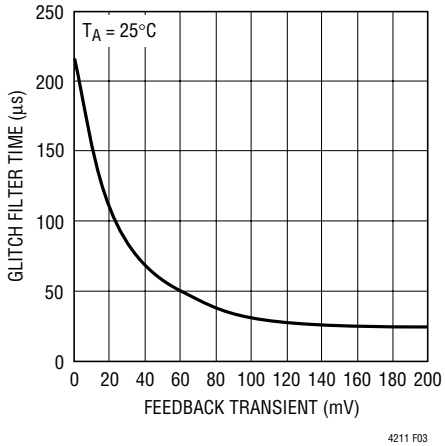



**Figure 3. FB Comparator Glitch Filter Time vs Feedback Transient Voltage**

### SYSTEM TIMING

System timing for the LTC4211 is generated in the equivalent circuit shown in Figure 4. If the LTC4211's internal timing circuit is off, an internal N-channel FET connects the TIMER pin to GND. If the timing circuit is enabled, an internal 2µA current source is then connected to the TIMER pin to charge $C_{TIMER}$ at a rate given by Equation 1:

$$C_{TIMER}\ \text{Charge-Up Rate} = \frac{2\mu A}{C_{TIMER}} \quad (1)$$

When the TIMER pin voltage reaches COMP4's threshold of 1.236V, the TIMER pin is reset to GND. Equation 2 gives an expression for the timer period:

$$t_{TIMER} = 1.236V \bullet \frac{C_{TIMER}}{2\mu A} \quad (2)$$

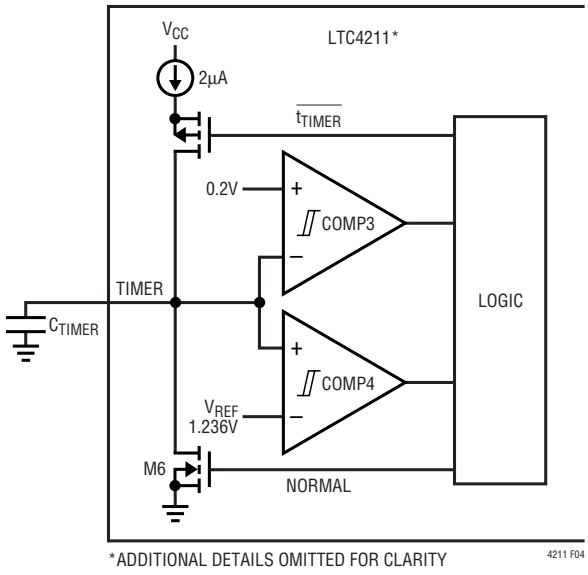



**Figure 4. LTC4211 System Timing Block Diagram**

As a design aid, the LTC4211's timer period as a function of the $C_{TIMER}$ using standard values from 0.01µF to 1µF is shown in Table 1.

## OPERATION

**Table 1. $t_{TIMER}$ vs $C_{TIMER}$**

| $C_{TIMER}$ | $t_{TIMER}$ |
|---|---|
| 0.01µF | 6.2ms |
| 0.022µF | 13.62ms |
| 0.033µF | 20.41ms |
| 0.047µF | 29.07ms |
| 0.068µF | 42.04ms |
| 0.082µF | 50.7ms |
| 0.1µF | 61.82ms |
| 0.22µF | 136ms |
| 0.33µF | 203.9ms |
| 0.47µF | 290.5ms |
| 0.68µF | 420.2ms |
| 0.82µF | 506.8ms |
| 1µF | 618ms |

Ensuring a proper start-up sequence is also dependent on selecting the most appropriate value for $C_{TIMER}$ for the application. Long timing periods affect overall system start-up times. A timing period set too short and the system may never start up. A good starting point is to set $C_{TIMER}$ = 0.1µF and then adjust its value accordingly for the application.

### OPERATING SEQUENCE

#### Power-Up, Start-Up Check and Plug-In Timing Cycle

The sequence of operations for the LTC4211 is illustrated in the timing diagram of Figure 5. When a PC board is first inserted into a live backplane, the LTC4211 first performs

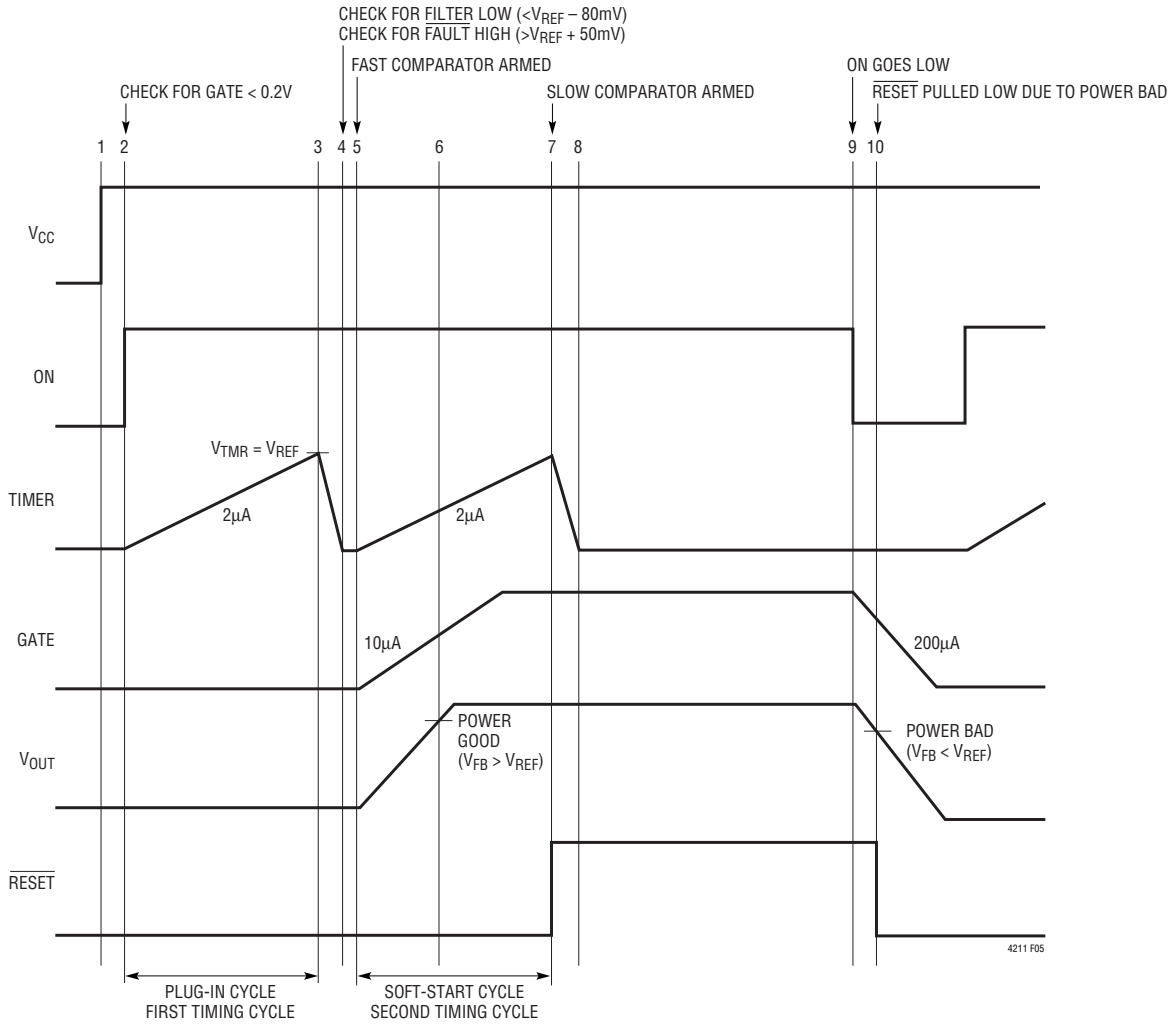



**Figure 5. Normal Power-Up Sequence**

## OPERATION

a start-up check to make sure the supply voltage is above its 2.3V UVLO threshold (see Time Point 1). If the input supply voltage is valid, the gate of the external pass transistor is pulled to ground by the internal 200µA current source connected at the GATE pin. The TIMER pin is held low by an internal N-channel pull-down transistor (see M6, LTC4211 Block Diagram) and the FILTER pin voltage is pulled to ground by an internal 10µA current source.

Once $V_{CC}$ and ON (the ON pin is >1.316) are valid, the LTC4211 checks to make sure that GATE is OFF ($V_{GATE}$ < 0.2V) at Time Point 2. An internal timing circuit is enabled and the TIMER pin voltage ramps up at the rate described by Equation 1. At Time Point 3 (the timing period programmed by $C_{TIMER}$), the TIMER pin voltage equals $V_{TMR}$ (1.236V). Next, the TIMER pin voltage ramps down to Time Point 4 where the LTC4211 performs two checks: (1) FILTER pin voltage is low ($V_{FILTER}$ < 1.156V) and (2) $\overline{FAULT}$ pin voltage is high ($V_{\overline{FAULT}}$ > 1.286V). If both conditions are met, the LTC4211 begins a second timing (soft-start) cycle.

### Second Timing (Soft-Start) Cycle

At the beginning of the second timing cycle (Time Point 5), the LTC4211's FAST COMP is armed and an internal 10µA current source working with an internal charge pump provides the gate drive to the external pass transistor. An expression for the GATE voltage slew rate is given by Equation 3:

$$V_{GATE}\ \text{Slew Rate},\ \frac{dV_{GATE}}{dt} = \frac{10\mu A}{C_{GATE}} \qquad (3)$$

where $C_{GATE}$ = Power MOSFET gate input capacitance ($C_{ISS}$).

For example, a Si4410DY (a 30V N-channel power MOSFET) exhibits an approximate $C_{GATE}$ of 3300pF at $V_{GS}$ = 10V. The LTC4211's GATE voltage rate-of-change (slew rate) for this example would be:

$$V_{GATE}\ \text{Slew Rate},\ \frac{dV_{GATE}}{dt} = \frac{10\mu A}{3300pF} = 3.03\frac{V}{ms}$$

The inrush current being delivered to the load while the GATE is ramping is dependent on $C_{LOAD}$ and $C_{GATE}$. Equation 4 gives an expression for the inrush current during the second timing cycle:

$$I_{INRUSH} = \frac{dV_{GATE}}{dt} \bullet C_{LOAD} = 10\mu A \bullet \frac{C_{LOAD}}{C_{GATE}} \qquad (4)$$

For example, if $C_{GATE}$ = 3300pF and $C_{LOAD}$ = 2000µF, the inrush current charging $C_{LOAD}$ is:

$$I_{INRUSH} = 10\mu A \bullet \frac{2000\mu F}{0.0033\mu F} = 6.06A \qquad (5)$$

At Time Point 6, the output voltage trips COMP2's threshold, signaling an output voltage "power good" condition. At Time Point 7, $\overline{RESET}$ is asserted high, SLOW COMP is armed and the LTC4211 enters a fault monitor mode. The TIMER voltage then ramps down to Time Point 8.

### Power-Off Cycle

As shown at Time Point 9, an external hard reset is initiated by pulling the ON pin low ($V_{ON}$ < 1.236V). The GATE pin voltage is ramped to ground by the internal 200µA current source, discharging $C_{GATE}$ and turning off the pass transistor. As $C_{LOAD}$ discharges, the output voltage crosses COMP2's threshold, signaling a "power bad" condition at Time Point 10. At this point, $\overline{RESET}$ is asserted low.

### SOFT-START WITH CURRENT LIMITING

During the second timing cycle, the inrush current was described by Equation 4. Note that there is a one-to-one correspondence in the inrush current to $C_{LOAD}$. If the inrush current is large enough to cause a voltage drop greater than 50mV across the sense resistor, an internal servo loop controls the operation of the 10µA current source at the GATE pin to regulate the load current to:

$$I_{LIMIT(SOFTSTART)} = \frac{50mV}{R_{SENSE}} \qquad (6)$$

For example, the inrush current is limited to 5A when $R_{SENSE}$ = 0.01Ω.

In this fashion, the inrush current is controlled and $C_{LOAD}$ is charged up slowly during the soft-start cycle.

## OPERATION

The timing diagram in Figure 6 illustrates the operation of the LTC4211 in a normal power-up sequence with limited inrush current as described by Equation 6. At Time Point 5, the GATE pin voltage begins to ramp indicating that the power MOSFET is beginning to charge $C_{LOAD}$. At Time Point 5A, the inrush current causes a 50mV voltage drop across $R_{SENSE}$ and the internal servo loop engages, limiting the inrush current to a fixed level. At Time Point 6, the GATE pin voltage continues to ramp as $C_{LOAD}$ charges until $V_{OUT}$ reaches its final value. The charging current reduces, and the internal servo loop disengages. At the end of the soft-start cycle (Time Point 7), $\overline{RESET}$ is high and SLOW COMP is armed.

### FREQUENCY COMPENSATION AT SOFT-START

If the external gate input capacitance ($C_{ISS}$) is greater than 600pF, no external gate capacitor is required at GATE to stabilize the internal current-limiting loop during soft-start. The servo loop that controls the external MOSFET during current limiting has a unity-gain frequency of about 105kHz and phase margin of 80° for external MOSFET gate input capacitances to 2.5nF.

### USING AN EXTERNAL GATE CAPACITOR

The LTC4211 automatically limits the inrush current in one of two ways: by controlling the GATE pin voltage slew rate

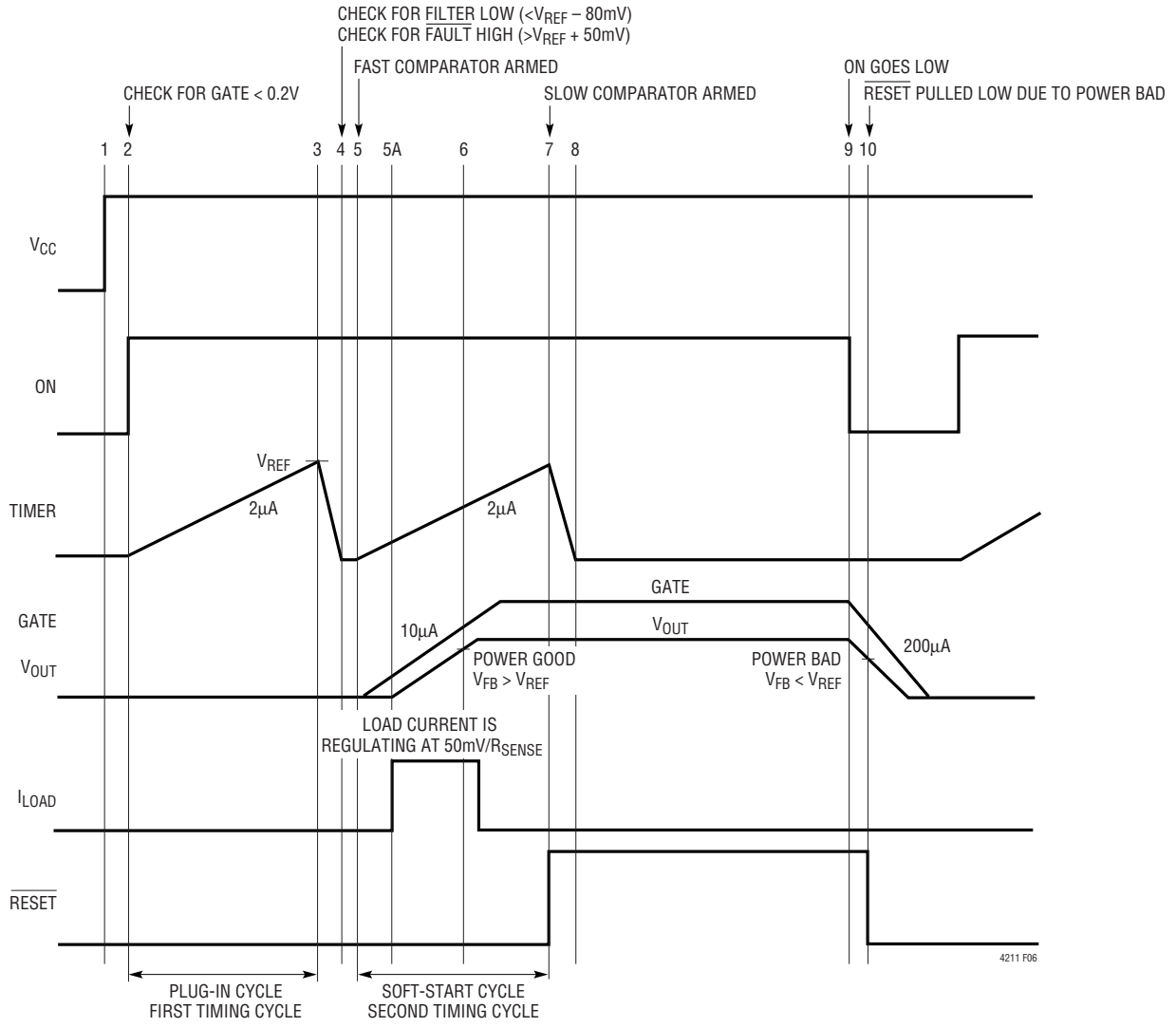



**Figure 6. Normal Power-Up Sequence (With Current Limiting in Second Timing Cycle)**

## OPERATION

or by actively limiting the inrush current. The LTC4211 uses GATE voltage slew rate limiting when $C_{LOAD}$ is small and/or the inrush current limit is set high. If GATE voltage slew rate control is preferred with large $C_{LOAD}$, an external capacitor ($C_{GX}$) can be used from GATE to ground, as shown in Figure 7. According to Equation 3, adding $C_{GX}$ slows the GATE voltage slew rate at the expense of slower system turn-on and turn-off time. Should this technique be used, values for $C_{GX}$ less than 150nF are recommended.

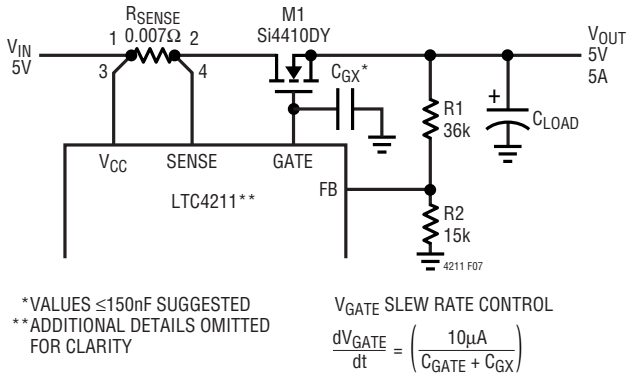



**Figure 7. Using an External Capacitor at GATE for GATE Voltage Slew Rate Control and Large $C_{LOAD}$**

An external gate capacitor may also be useful to decrease or eliminate current spikes through the MOSFET when power is first applied. At power-up, the instantaneous input voltage step attempts to pull the MOSFET gate up through the MOSFET's drain-to-gate capacitance. If the MOSFET's $C_{ISS}$ is small, the gate can be pulled up high enough to turn on the MOSFET, thereby allowing a current spike to the output. This event occurs during the time that the LTC4211 is coming out of UVLO and getting its intelligence to hold the GATE pin low. An external capacitor attenuates the voltage to which the GATE is pulled up and eliminates the current spike. The value required is dependent on the MOSFET capacitance specifications. In typical applications, this capacitor is not required.

### ELECTRONIC CIRCUIT BREAKER

The LTC4211 features an electronic circuit breaker function that protects against supply overvoltage, externally-generated fault conditions and shorts or excessive load current conditions on the supply. If the circuit breaker trips, the GATE pin is immediately pulled to ground, the external N-channel MOSFET is quickly turned OFF and $\overline{FAULT}$ is latched low.

The circuit breaker trips whenever the voltage across the sense resistor exceeds two different levels, each level set by the LTC4211's SLOW COMP and FAST COMP (see Block Diagram). The SLOW COMP trips the circuit breaker if the voltage across the SENSE resistor ($V_{CC} – V_{SENSE} = V_{CB}$) is greater than 50mV for 20µs. There may be applications where this comparator's response time is not long enough, for example, because of excessive supply voltage noise. To adjust the response time of the SLOW COMP, the MS10 version of the LTC4211 is chosen and a capacitor is used at the LTC4211's FILTER pin (see section on Adjusting SLOW Comp's Response Time). The FAST COMP trips the circuit breaker to protect against fast load overcurrents if the transient voltage across the sense resistor is greater than 150mV for 300ns. The response time of the LTC4211's FAST COMP is fixed.

The timing diagram of Figure 6 illustrates when the LTC4211's electronic circuit breaker is armed. After the first timing cycle, the LTC4211's FAST COMP is armed at Time Point 5. Arming FAST COMP at Time Point 5 ensures that the system is protected against a short-circuit condition during the second timing cycle after $C_{LOAD}$ has been fully charged. At Time Point 7, SLOW COMP is armed when the internal control loop is disengaged.

The timing diagrams in Figures 8 and 9 illustrate the operation of the LTC4211 when the load current conditions exceed the thresholds of the FAST COMP ($V_{CB(FAST)}$ > 150mV) and SLOW COMP ($V_{CB(SLOW)}$ > 50mV), respectively.

### RESETTING THE ELECTRONIC CIRCUIT BREAKER

Once the LTC4211's circuit breaker is tripped, $\overline{FAULT}$ is asserted low and the GATE pin is pulled to ground. The LTC4211 remains latched OFF in this fault state until the external fault is cleared. To clear the internal fault detect circuitry and to restart the LTC4211, its ON pin must be driven low ($V_{ON}$ < 1.236V) for at least 150µs, after which time $\overline{FAULT}$ goes high. Toggling the ON pin from low to high ($V_{ON}$ > 1.316V) initiates a restart sequence in the LTC4211. The timing diagram in Figure 10 illustrates a

## OPERATION

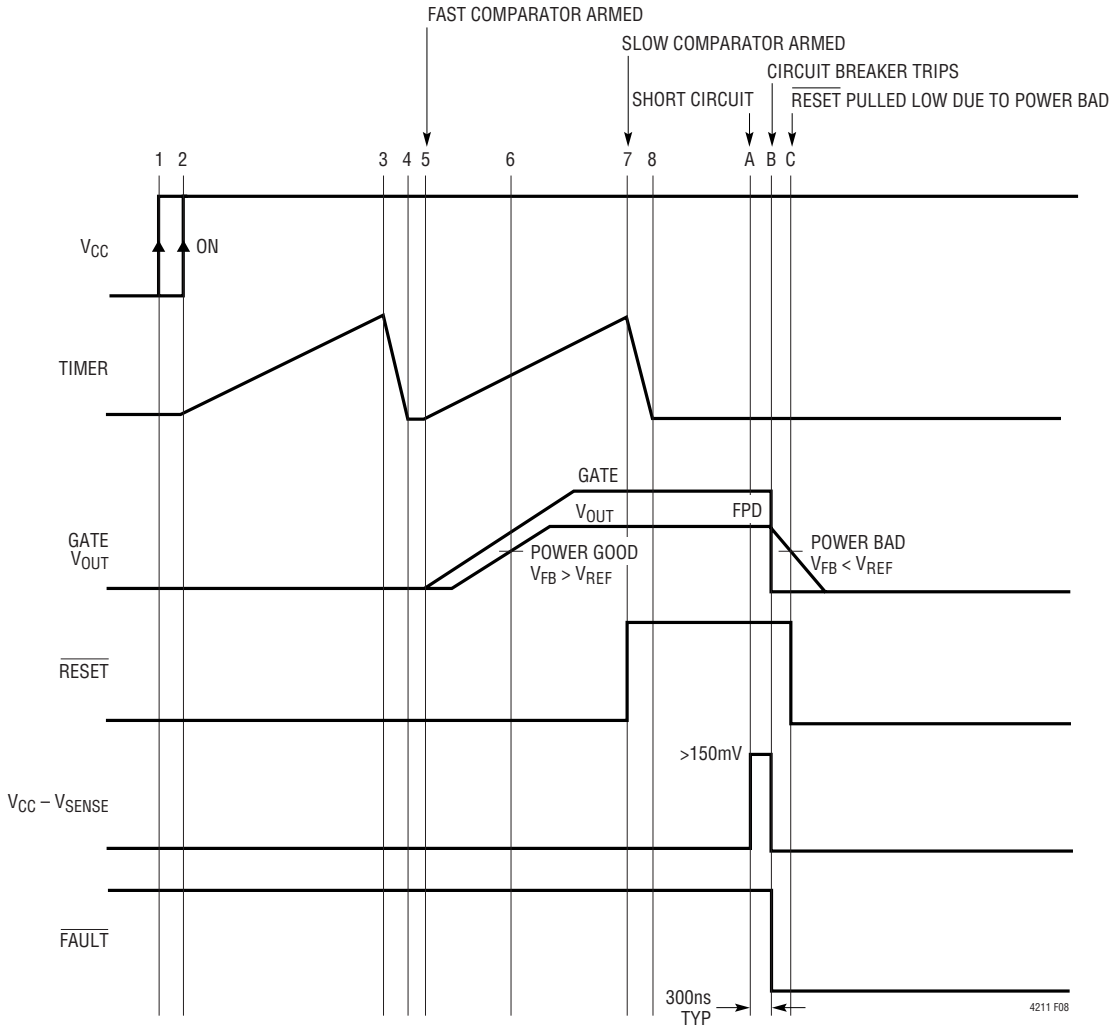



**Figure 8. Output Short Circuit Causes Fast Comparator to Trip the Circuit Breaker**

## OPERATION

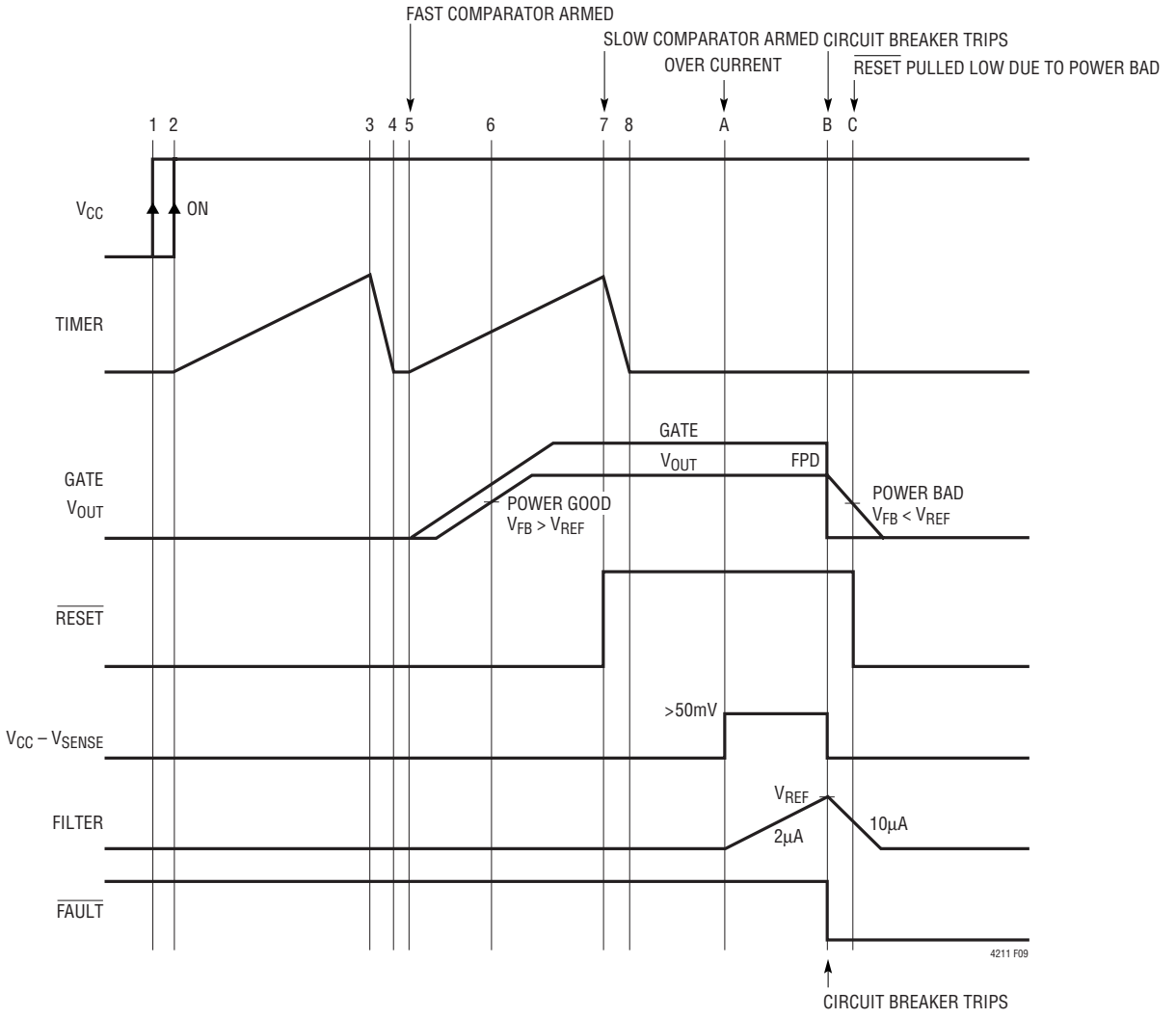



**Figure 9. Mild Overcurrent Slow Comparator Trips the Circuit Breaker After Filter Programming Period**

## OPERATION

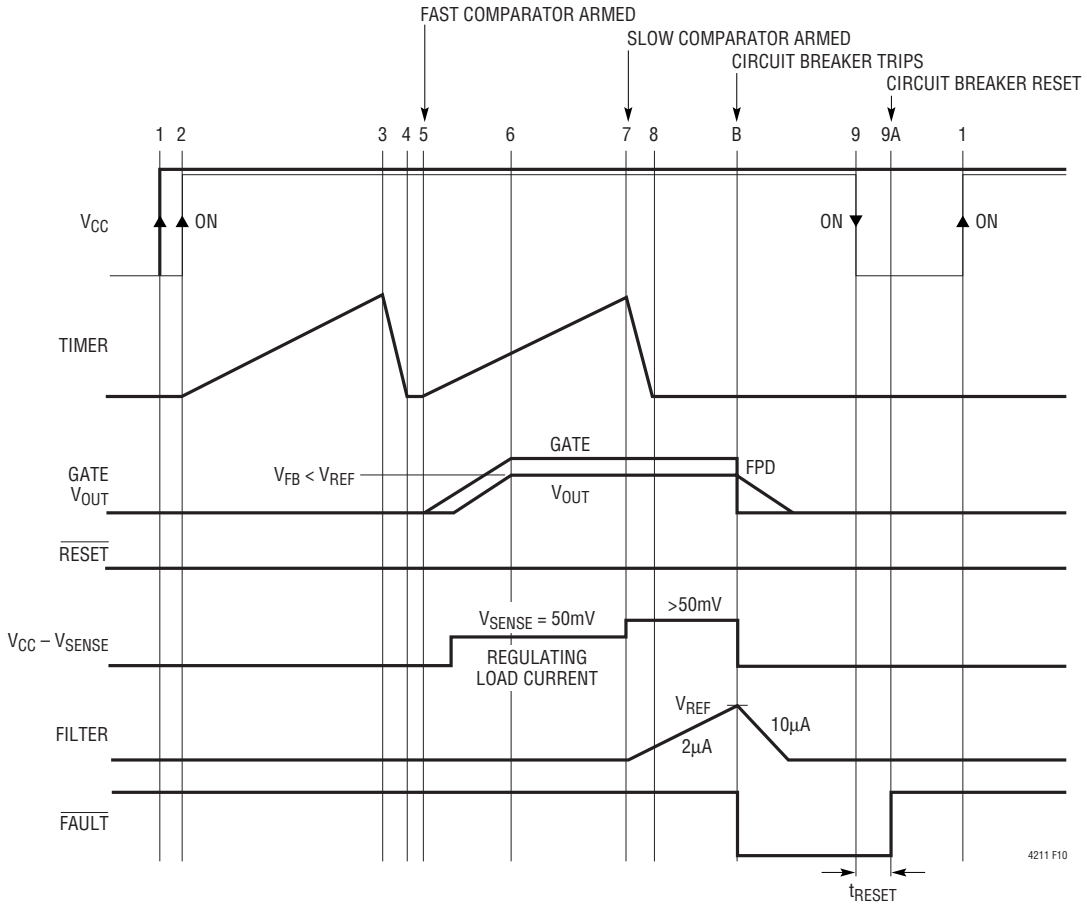



**Figure 10. Power-Up in Overcurrent, Slow Comparator Trips the Circuit Breaker**

start-up sequence where the LTC4211 is powered up into a load overcurrent condition. Note that the circuit breaker trips at Time Point B and is reset at Time Point 9A.

### ADJUSTING SLOW COMP'S RESPONSE TIME

The response time of SLOW COMP is adjusted using a capacitor connected from the LTC4211's FILTER pin to ground. If this pin is left unused, SLOW COMP's delay defaults to 20µs. During normal operation, the FILTER output pin is held low as an internal 10µA pull-down current source is connected to this pin by transistor M4. This pull-down current source is turned off when an overcurrent load condition is detected by SLOW COMP. During an overcurrent condition, the internal 2µA pull-up current source is connected to the FILTER pin by transistor M5, thereby charging $C_{FILTER}$. As the charge on the capacitor accumulates, the voltage across $C_{FILTER}$ increases. Once the FILTER pin voltage increases to 1.236V, the electronic circuit breaker trips and the LTC4211's GATE pin is switched quickly to ground by transistor M3. After the circuit breaker is tripped, M5 is turned OFF, M4 is turned ON and the 10µA pull-down current then holds the FILTER pin voltage low.

SLOW COMP's response time from an overcurrent fault condition to when the circuit breaker trips (GATE OFF) is given by Equation 7:

$$t_{SLOWCOMP} = 1.236V \bullet \frac{C_{FILTER}}{2\mu A} + 20\mu s \qquad (7)$$

For example, if $C_{FILTER}$ = 1000pF, SLOW COMP's response time = 638µs. As a design aid, SLOW COMP's delay time ($t_{SLOW\,COMP}$) versus $C_{FILTER}$ for standard values of $C_{FILTER}$ from 100pF to 1000pF is illustrated in Table 2.

## OPERATION

**Table 2. $t_{SLOWCOMP}$ vs $C_{FILTER}$**

| $C_{FILTER}$ | $t_{SLOWCOMP}$ |
|---|---|
| 100pF | 82µs |
| 220pF | 156µs |
| 330pF | 224µs |
| 470pF | 310µs |
| 680pF | 440µs |
| 820pF | 527µs |
| 1000pF | 638µs |

### SENSE RESISTOR CONSIDERATIONS

The fault current level at which the LTC4211's internal electronic circuit breaker trips is determined by a sense resistor connected between the LTC4211's $V_{CC}$ and SENSE pins and two separate trip points. The first trip point is set by the SLOW COMP's threshold, $V_{CB(SLOW)}$ = 50mV, and occurs should a load current fault condition exist for more than 20µs. The current level at which the electronic circuit breaker trips is given by Equation 8:

$$I_{TRIP(SLOW)} = \frac{V_{CB(SLOW)}}{R_{SENSE}} = \frac{50mV}{R_{SENSE}} \quad (8)$$

The second trip point is set by the FAST COMP's threshold, $V_{CB(FAST)}$ = 150mV, and occurs during fast load current transients that exist for 300ns or longer. The current level at which the circuit breaker trips in this case is given by Equation 9:

$$I_{TRIP(FAST)} = \frac{V_{CB(FAST)}}{R_{SENSE}} = \frac{150mV}{R_{SENSE}} \quad (9)$$

As a design aid, the currents at which electronic circuit breaker trips for common values for $R_{SENSE}$ are shown in Table 3.

**Table 3. $I_{TRIP(SLOW)}$ and $I_{TRIP(FAST)}$ vs $R_{SENSE}$**

| $R_{SENSE}$ | $I_{TRIP(SLOW)}$ | $I_{TRIP(FAST)}$ |
|---|---|---|
| 0.005Ω | 10A | 30A |
| 0.006Ω | 8.3A | 25A |
| 0.007Ω | 7.1A | 21A |
| 0.008Ω | 6.3A | 19A |
| 0.009Ω | 5.6A | 17A |
| 0.01Ω | 5A | 15A |

For proper circuit breaker operation, Kelvin-sense PCB connections between the sense resistor and the LTC4211's $V_{CC}$ and SENSE pins are strongly recommended. The drawing in Figure 11 illustrates the correct way of making connections between the LTC4211 and the sense resistor. PCB layout should be balanced and symmetrical to minimize wiring errors. In addition, the PCB layout for the sense resistor should include good thermal management techniques for optimal sense resistor power dissipation.

The power rating of the sense resistor should accommodate steady-state fault current levels so that the component is not damaged before the circuit breaker trips. Table 4 in the Appendix lists suggested sense resistors that can be used with the LTC4211's circuit breaker.

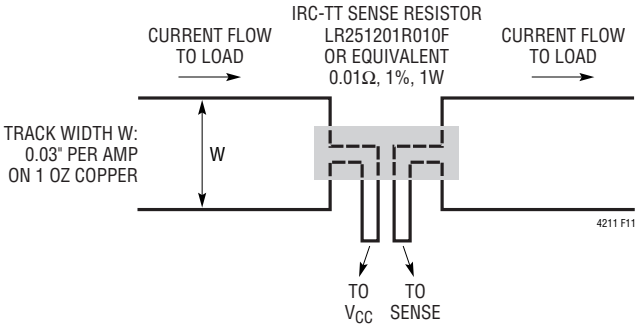



**Figure 11. Making PCB Connections to the Sense Resistor**

### CALCULATING CIRCUIT BREAKER TRIP CURRENT

For a selected $R_{SENSE}$ value, the nominal load current that trips the circuit breaker is given by Equation 10:

$$I_{TRIP(NOM)} = \frac{V_{CB(NOM)}}{R_{SENSE(NOM)}} = \frac{50mV}{R_{SENSE(NOM)}} \quad (10)$$

The minimum load current that trips the circuit breaker is given by Equation 11.

$$I_{TRIP(MIN)} = \frac{V_{CB(MIN)}}{R_{SENSE(MAX)}} = \frac{40mV}{R_{SENSE(MAX)}} \quad (11)$$

where

$$R_{SENSE(MAX)} = R_{SENSE(NOM)} \bullet \left[1 + \left(\frac{R_{TOL}}{100}\right)\right]$$

## OPERATION

The maximum load current that trips the circuit breaker is given in Equation 12.

$$I_{TRIP(MAX)} = \frac{V_{CB(MAX)}}{R_{SENSE(MIN)}} = \frac{60mV}{R_{SENSE(MIN)}} \quad (12)$$

where

$$R_{SENSE(MIN)} = R_{SENSE(NOM)} \bullet \left[1 - \left(\frac{R_{TOL}}{100}\right)\right]$$

For example:

If a sense resistor with 7mΩ ±5% $R_{TOL}$ is used for current limiting, the nominal trip current $I_{TRIP(NOM)}$ = 7.1A. From Equations 11 and 12, $I_{TRIP(MIN)}$ = 5.4A and $I_{TRIP(MAX)}$ = 9.02A respectively.

For proper operation and to avoid the circuit breaker tripping unnecessarily, the minimum trip current ($I_{TRIP(MIN)}$) must exceed the circuit's maximum operating load current. For reliability purposes, the operation at the maximum trip current ($I_{TRIP(MAX)}$) must be evaluated carefully. If necessary, two resistors with the same $R_{TOL}$ can be connected in parallel to yield an $R_{SENSE(NOM)}$ value that fits the circuit requirements.

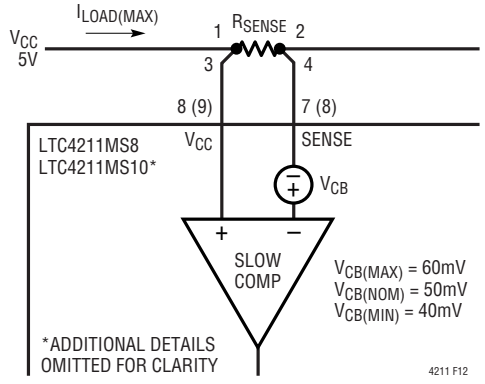



**Figure 12. Circuit Breaker Equivalent Circuit for Calculating $R_{SENSE}$**

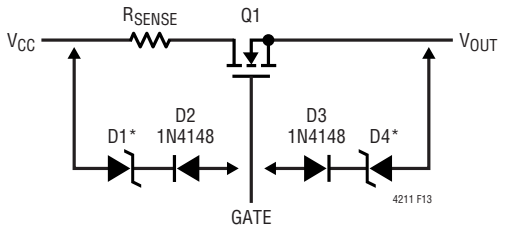
### POWER MOSFET SELECTION CRITERIA

To start the power MOSFET selection process, choose the maximum drain-to-source voltage, $V_{DS(MAX)}$, and the maximum drain current, $I_{D(MAX)}$ of the MOSFET. The $V_{DS(MAX)}$ rating must exceed the maximum input supply voltage (including surges, spikes, ringing, etc.) and the $I_{D(MAX)}$ rating must exceed the maximum short-circuit current in the system during a fault condition. In addition, consider three other key parameters: 1) the required gate-source ($V_{GS}$) voltage drive, 2) the voltage drop across the drain-to-source on resistance, $R_{DS(ON)}$ and 3) the maximum junction temperature rating of the MOSFET.

Power MOSFETs are classified into two categories: standard MOSFETs ($R_{DS(ON)}$ specified at $V_{GS}$ = 10V) and logic-level MOSFETs ($R_{DS(ON)}$ specified at $V_{GS}$ = 5V). The absolute maximum rating for $V_{GS}$ is typically ±20V for standard MOSFETs. However, the $V_{GS}$ maximum rating for logic-level MOSFETs ranges from ±8V to ±20V depending upon the manufacturer and the specific part number. The LTC4211's gate overdrive as a function of $V_{CC}$ is illustrated in the Typical Performance curves. Logic-level MOSFETs are recommended for low supply voltage applications and standard MOSFETs can be used for applications where supply voltage is greater than 4.75V.

Note that in some applications, the gate of the external MOSFET can discharge faster than the output voltage when the circuit breaker is tripped. This causes a negative $V_{GS}$ voltage on the external MOSFET. Usually, the selected external MOSFET should have a $\pm V_{GS(MAX)}$ rating that is higher than the operating input supply voltage to ensure that the external MOSFET is not destroyed by a negative $V_{GS}$ voltage. In addition, the $\pm V_{GS(MAX)}$ rating of the MOSFET must be higher than the gate overdrive voltage. Lower $\pm V_{GS(MAX)}$ rating MOSFETs can be used with the LTC4211 if the GATE overdrive is clamped to a lower voltage. The circuit in Figure 13 illustrates the use of Zener diodes to clamp the LTC4211's GATE overdrive signal if

## OPERATION




*USER SELECTED VOLTAGE CLAMP
(A LOW BIAS CURRENT ZENER DIODE IS RECOMMENDED)
1N4688 (5V)
1N4692 (7V): LOGIC-LEVEL MOSFET
1N4695 (9V)
1N4702 (15V): STANDARD-LEVEL MOSFET

**Figure 13. Optional Gate Clamp for Lower $V_{GS(MAX)}$ MOSFETs**

lower voltage MOSFETs are used. The clamp network is connected from $V_{CC}$ to GATE or from GATE to $V_{OUT}$ — only one network is necessary, not both.

The $R_{DS(ON)}$ of the external pass transistor should be low to make its drain-source voltage ($V_{DS}$) a small percentage of $V_{CC}$. At a $V_{CC}$ = 2.5V, $V_{DS}$ + $V_{RSENSE}$ = 0.1V yields 4% error at the output voltage. This restricts the choice of MOSFETs to very low $R_{DS(ON)}$. At higher $V_{CC}$ voltages, the $V_{DS}$ requirement can be relaxed in which case MOSFET package dissipation ($P_D$ and $T_J$) may limit the value of $R_{DS(ON)}$. Table 5 lists some power MOSFETs that can be used with the LTC4211.

Power MOSFET junction temperature is dependent on four parameters: current delivered to the load, $I_{LOAD}$, $R_{DS(ON)}$, junction-to-ambient thermal resistance, $\theta_{JA}$, and the maximum ambient temperature to which the circuit will be exposed, $T_{A(MAX)}$. For reliable circuit operation, the maximum junction temperature ($T_{J(MAX)}$) for a power MOSFET should not exceed the manufacturer's recommended value. This includes normal mode operation, start-up, current-limit and autoretry mode in a fault condition. For a given set of conditions, the junction temperature of a power MOSFET is given by Equation 13:

MOSFET Junction Temperature,

$$T_{J(MAX)} \leq T_{A(MAX)} + \theta_{JA} \bullet P_D \quad (13)$$

where

$$P_D = (I_{LOAD})^2 \bullet R_{DS(ON)}$$

PCB layout techniques for optimal thermal management of power MOSFET power dissipation help to keep device $\theta_{JA}$ as low as possible. See the section on PCB Layout Considerations for more information.

### USING STAGGERED PIN CONNECTORS

The LTC4211 can be used on either a printed circuit board or on the backplane side of the connector, and examples for both are shown in Figure 14. Printed circuit board edge connectors with staggered pins are recommended as the insertion and removal of circuit boards do sequence the pin connections. Supply voltage and ground connections on the printed circuit board should be wired to the edge connector's long pins or blades. Control and status signals (like $\overline{\text{RESET}}$, $\overline{\text{FAULT}}$ and ON) passing through the card's edge connector should be wired to short length pins or blades.

### PCB CONNECTION SENSE

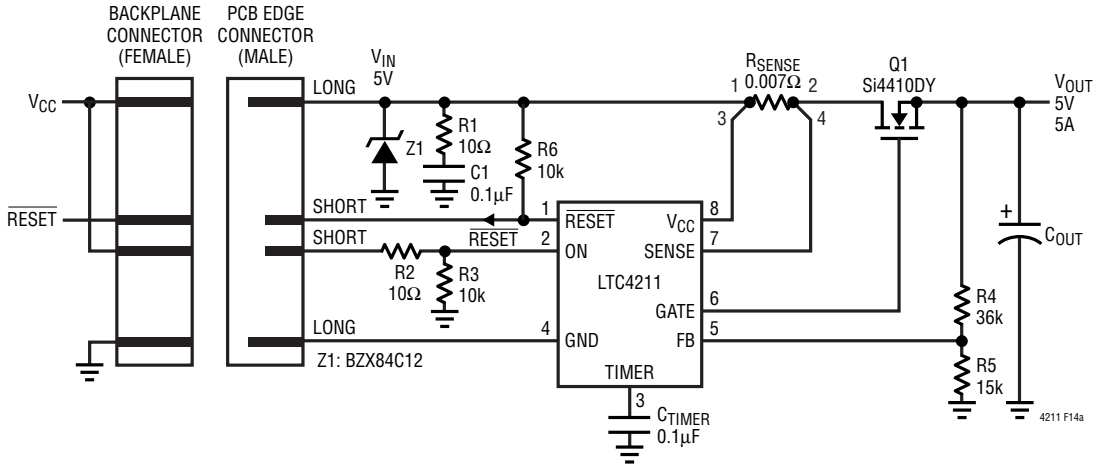
There are a number of ways to use the LTC4211's ON pin to detect whether the printed circuit board has been fully seated in the backplane before the LTC4211 commences a start-up cycle.

The first example is shown in the schematic on the front page of this data sheet. In this case, the LTC4211 is mounted on the PCB and a 10k resistive divider is connected to the ON pin. On the edge connector, R1 is wired to a short pin. Until the connectors are fully mated, the ON pin is held low, keeping the LTC4211 in an OFF state. Once the connectors are mated, the resistive divider is connected to $V_{CC}$, $V_{ON}$ > 1.316V and the LTC4211 begins a start-up cycle.

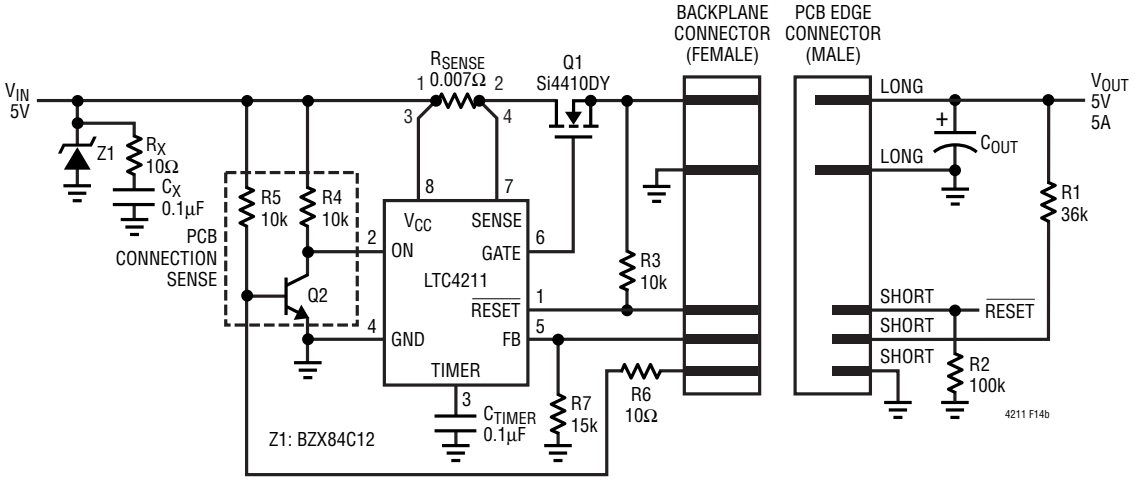
In Figure 14a, an LTC4211 is illustrated in a basic configuration on a PCB daughter card. The ON pin is connected directly to $V_{CC}$ on the backplane once the card is seated into the backplane. R2 and R3 are provided to bleed off any potential static charge which might exist on the backplane, the connector or during card installation.

A third example is shown in Figure 14b where the LTC4211 is mounted on the backplane. In this example, a 2N2222

## APPLICATIONS INFORMATION




**14a. Hot Swap Controller On Daughter Board**




**14b. Hot Swap Controller on Backplane**

**Figure 14. Staggered Pin Connections**

transistor and a pair of resistors (R4, R5) form the PCB connection sense circuit. With the card out of the chassis, Q2's base is biased to $V_{CC}$ through R5, biasing Q2 ON and driving the LTC4211's ON pin low. The base of Q2 is also wired to a socket on the backplane connector. When a card is firmly seated into the backplane, the base of Q2 is then grounded through a short pin connection on the card. Q2 is biased OFF, the LTC4211's ON pin is pulled-up to $V_{CC}$ and a start-up cycle begins.

In the previous three examples, the connection sense was hard wired with no processor (low) interrupt capability. As illustrated in Figure 15, the addition of an inexpensive logic-level discrete MOSFET and a couple of resistors offers processor interrupt control to the connection sense. R4 keeps the gate of M2 at $V_{CC}$ until the card is firmly mated to the backplane. A logic low for the $\overline{ON}$/OFF signal turns M2 OFF, allows the ON pin to pull high and turns on the LTC4211.

A more elaborate connection sense scheme is shown in Figure 16. The bases of Q1 and Q2 are wired to short pins located on opposite ends of the edge connector because

## APPLICATIONS INFORMATION

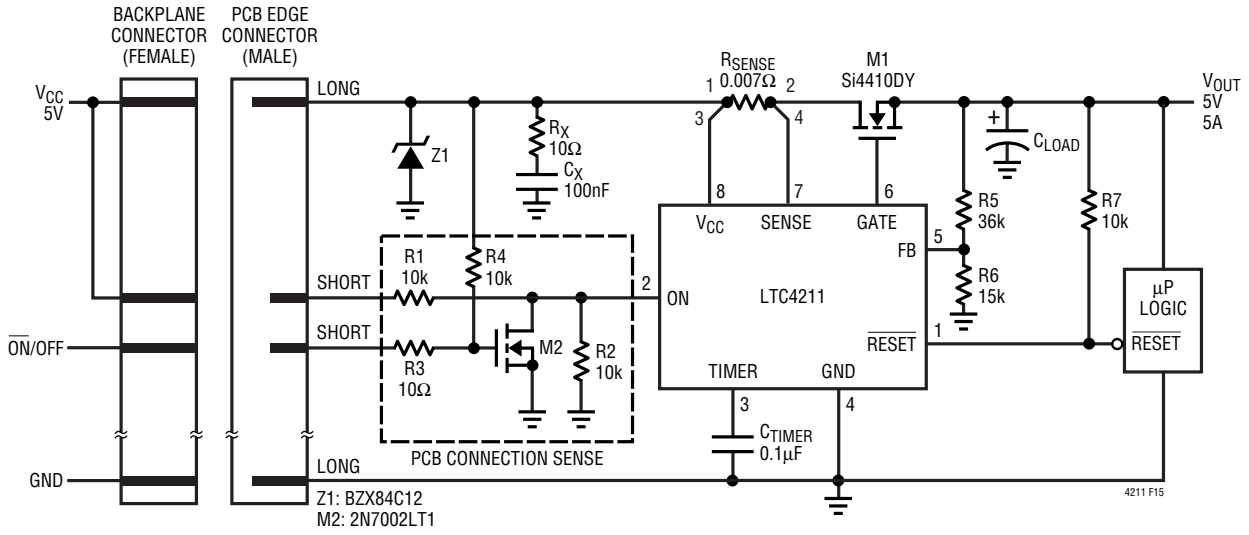



**Figure 15. Connection Sense with $\overline{ON}$/OFF Control**

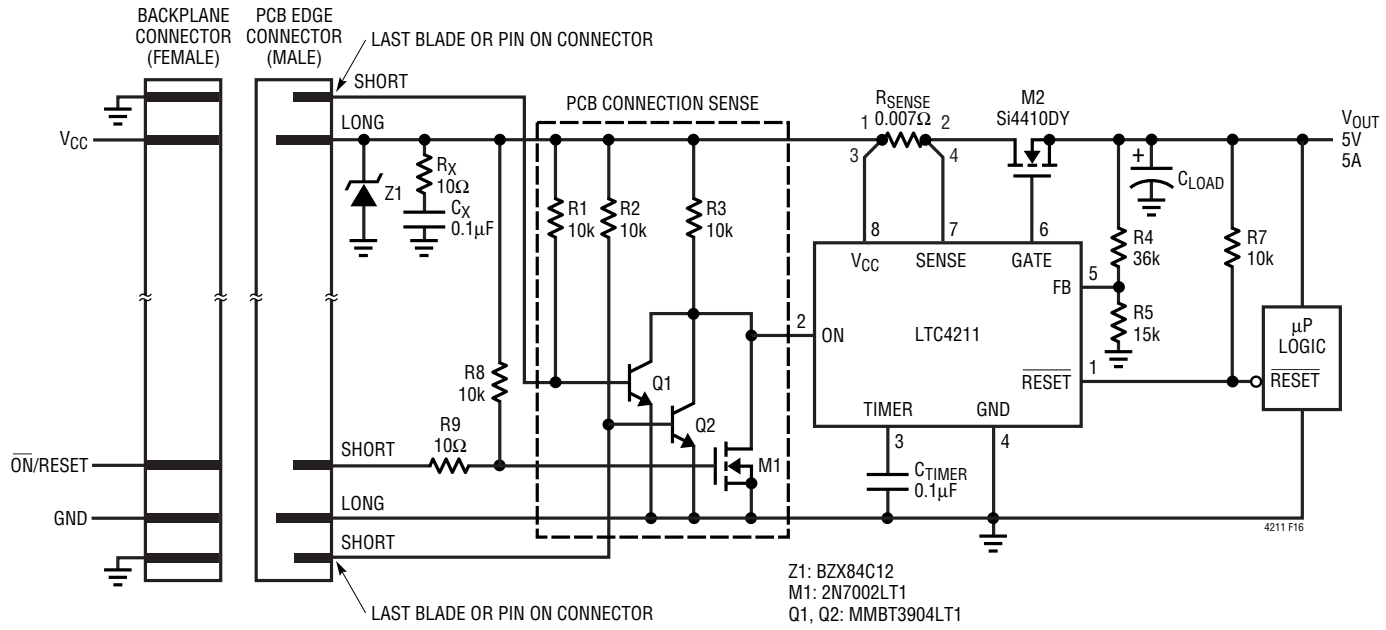



**Figure 16. Connection Sense for Rocking the Daughter Board Back and Forth**

the installation/removal of printed circuit cards generally requires rocking the card back and forth. When $V_{CC}$ makes connection, the bases of transistors Q1 and Q2 are pulled high, biasing them ON. When both are ON, the LTC4211's ON pin is held low, keeping the LTC4211 OFF. When the short base connector pins of Q1 and Q2 finally mate to the backplane, their bases are grounded, biasing the transistors OFF. The ON pin voltage is then pulled high by R3 enabling the LTC4211 and a power-up cycle begins.

A software-initiated power-down cycle can be started by momentarily driving transistor M1 with a logic high signal. This in turn will drive the LTC4211's ON pin low. If the ON pin is held low for more than 8µs, the LTC4211's GATE pin is switched to ground.

## APPLICATIONS INFORMATION

### HIGH SUPPLY VOLTAGE OPERATION CONSIDERATIONS

The LTC4211 can be used with supply voltages ranging from 2.5V to 16.5V. At high input supply voltages, the internal charge pump produces a minimum gate drive voltage of 8V for $V_{CC}$ > 15V. This minimum voltage drive is derived by an internal Zener diode clamp circuit, as shown in Figure 17. During PC board insertion or removal, sufficient transient current may flow through this Zener diode. To limit the amount of current during transient events, an optional small resistor between the LTC4211's GATE pin and the gate of the external FET can be used, as shown in Figure 17. A secondary benefit of this component is to minimize the possibility of high frequency parasitic oscillations in the power MOSFET.

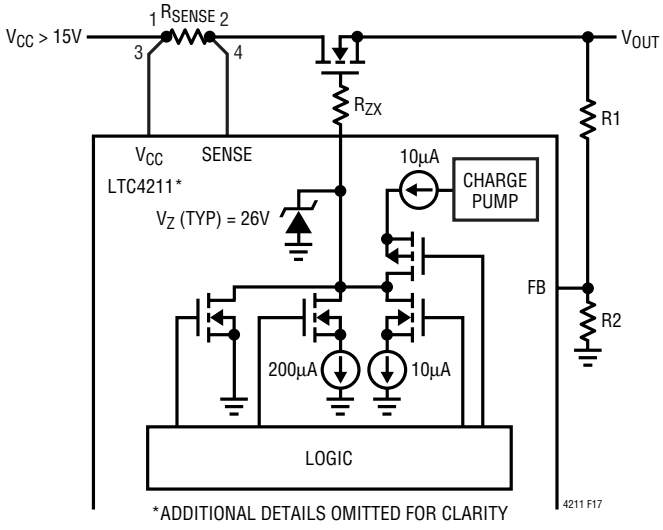



**Figure 17. Using an External Resistor to Limit Zener Current in High $V_{CC}$ Applications**

### AUTORETRY AFTER A FAULT

To configure the LTC4211 to automatically retry after a fault condition, the $\overline{FAULT}$ and ON pins can be connected to a pull-up resistor ($R_{AUTO}$) to the supply, as shown in Figure 18. In this case, the autoretry circuitry will attempt to restart the LTC4211 with a 50% duty cycle, as shown in the timing diagram of Figure 19. To prevent overheating the external MOSFET and other components during the autoretry sequence, adding a capacitor ($C_{AUTO}$) to the circuit introduces an RC time constant ($t_{OFF}$) that adjusts the autoretry duty cycle. Equation 14 gives the autoretry duty cycle, modified by this external time constant:

$$\text{Autoretry Duty Cycle} \approx \frac{t_{TIMER}}{t_{OFF} + 2 \bullet t_{TIMER}} \bullet 100\% \quad (14)$$

where $t_{TIMER}$ = LTC4211 system time constant (see TIMER function) and $t_{OFF}$ = External RC network time constant.

For the values shown, the external RC time constant is set at 1 second, the $t_{TIMER}$ delay equals 29ms and the autoretry duty cycle drops from 50% to 8%.

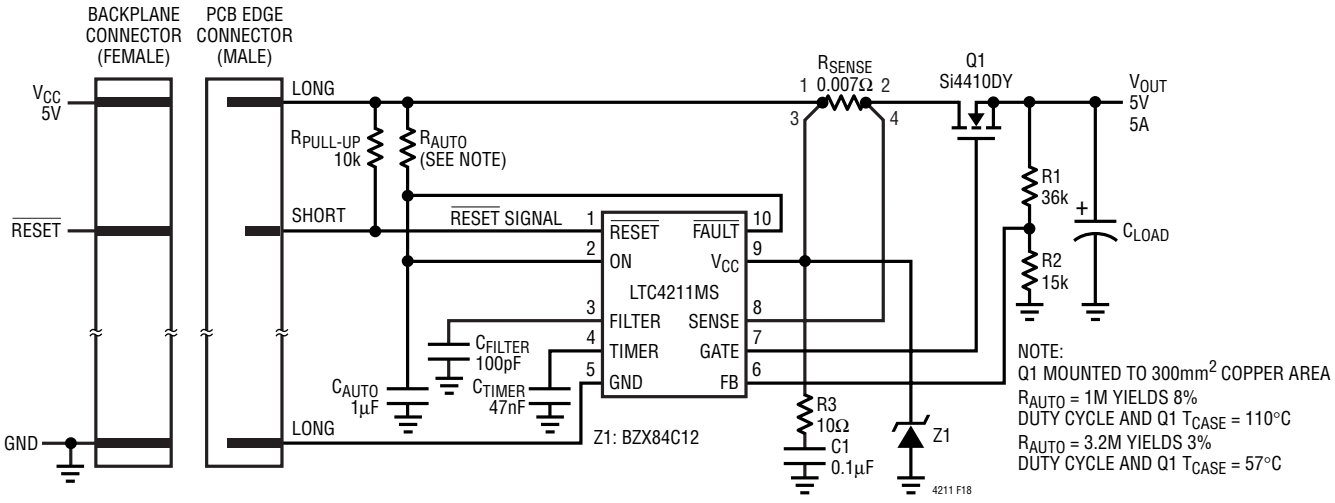



**Figure 18. LTC4211MS Autoretry Application**

## APPLICATIONS INFORMATION

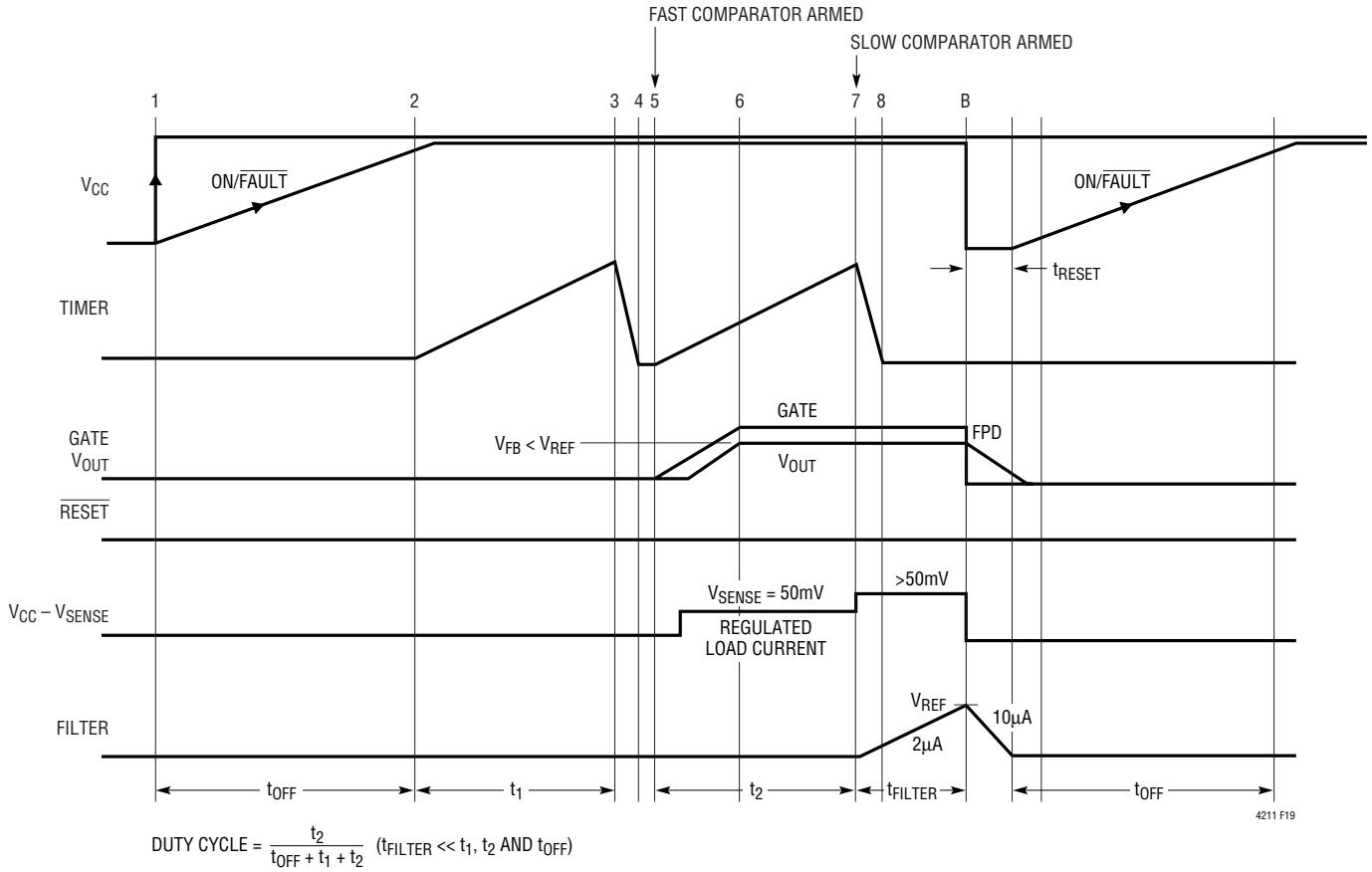



**Figure 19. Autoretry Timing**

To increase the RC delay, the user may either increase $C_{AUTO}$ or $R_{AUTO}$. However, increasing $C_{AUTO}$ > 2µF will actually limit the RC delay due to the reset sink-current capability of the FAULT pin. Therefore, in order to increase the RC delay, it is more effective to either increase $R_{AUTO}$ or to put a bleed resistor in parallel with $C_{AUTO}$ to GND. As an example, increasing $R_{AUTO}$ from 1M to 3.2M decreases duty cycle to 3%.

### HOT SWAPPING TWO SUPPLIES

Using two external pass transistors, the LTC4211 can switch two supply voltages. In some cases, it is necessary to bring up the dominant supply first during power-up but ramp them down together during the power-down phase. The circuit in Figure 20 shows how to program two different delays for the pass transistors. The 5V supply is powered up first. R1 and C3 are used to set the rise and fall times on the 5V supply. Next, the 3.3V supply ramps up with 20ms delay set by R6 and C2. On the falling edge, both supplies ramp down together because D1 and D2 bypass R1 and R6.

### OVERVOLTAGE TRANSIENT PROTECTION

Good engineering practice calls for bypassing the supply rail of any analog circuit. Bypass capacitors are often placed at the supply connection of every active device, in addition to one or more large value bulk bypass capacitors per supply rail. If power is connected abruptly, the large bypass capacitors slow the rate of rise of the supply voltage and heavily damp any parasitic resonance of lead or PC track inductance working against the supply bypass capacitors.

The opposite is true for LTC4211 Hot Swap circuits mounted on plug-in cards. In most cases, there is no supply bypass capacitor present on the powered supply

## APPLICATIONS INFORMATION

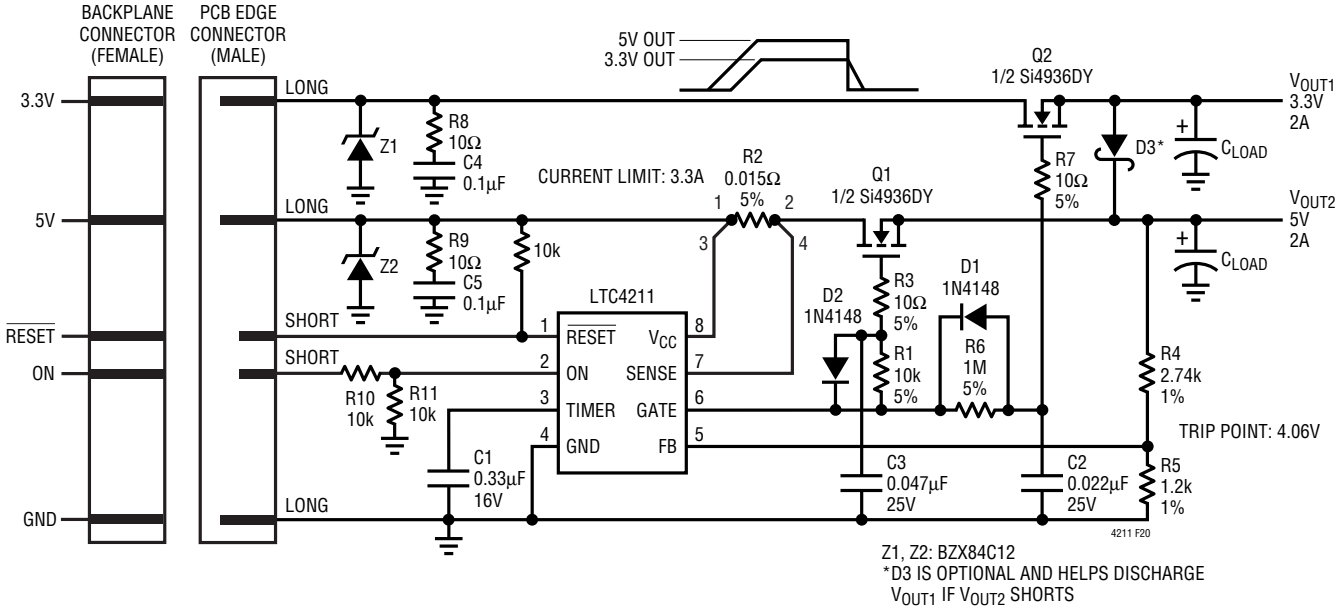



**Figure 20. Switching 5V and 3.3V**

voltage side of the MOSFET switch. An abrupt connection, produced by inserting the board into a backplane connector, results in a fast rising edge applied on the supply line of the LTC4211.

Since there is no bulk capacitance to damp the parasitic track inductance, supply voltage transients excite parasitic resonant circuits formed by the power MOSFET capacitance and the combined parasitic inductance from the wiring harness, the backplane and the circuit board traces. These ringing transients appear as a fast edge on the input supply line, exhibiting a peak overshoot to 2.5 times the steady-state value. This peak is followed by a damped sinusoidal response whose duration and period are dependent on the resonant circuit parameters. Since the absolute maximum supply voltage of the LTC4211 is 17V, transient protection against $V_{CC}$ > 6.8V supply voltage spikes and ringing is highly recommended.

In these applications, there are two methods for eliminating these supply voltage transients: using Zener diodes (or TransZorbs®) to clip the transient to a safe level and snubber networks. Snubber networks are series RC networks whose time constants are experimentally determined based on the board's parasitic resonance circuits. As a starting point, the capacitors in these networks are chosen to be 10× to 100× the power MOSFET's $C_{OSS}$ under bias. The series resistor is a value determined experimentally and ranges from 1Ω to 50Ω, depending on the parasitic resonance circuit. Note that in all LTC4211 circuit schematics, Zener diodes and snubber networks have been added to each 3.3V and 5V supply rail and should *always* be used. These protection networks should be mounted very close to the LTC4211's supply voltage using short lead lengths to minimize lead inductance. This is shown schematically in Figure 21, and a recommended layout of the transient protection devices around the LTC4211 is shown in Figure 22.

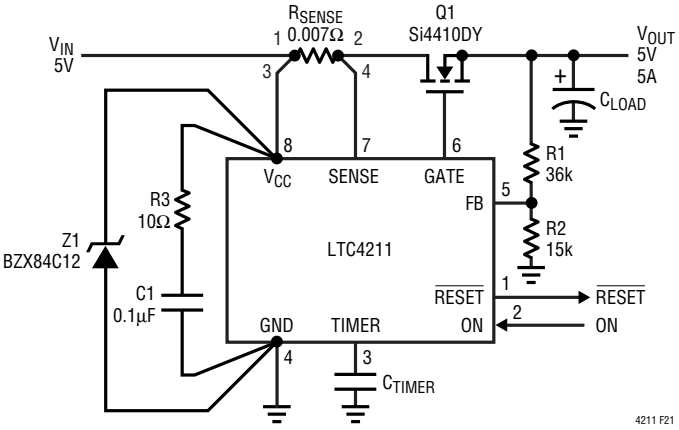
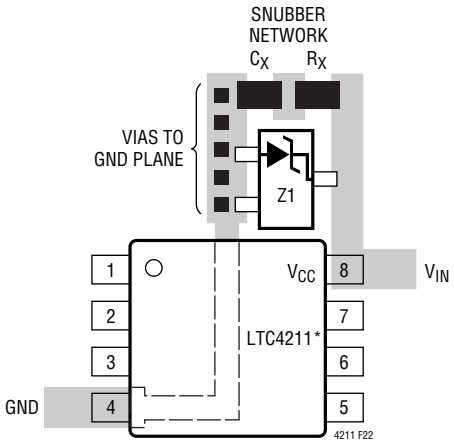



**Figure 21. Placing Transient Protection Devices Close to the LTC4211**

TransZorb is a registered trademark of General Instruments, GSI

# APPLICATIONS INFORMATION




NOTE: DRAWING IS NOT TO SCALE!
*ADDITIONAL DETAILS OMITTED FOR CLARITY

**Figure 22. Recommended Layout for Transient Protection Devices**

## ADDITIONAL SUPPLY OVERVOLTAGE DETECTION/PROTECTION

In addition to using external protection devices around the LTC4211 for large scale transient protection, low power Zener diodes can be used with the LTC4211's FILTER pin to act as a supply overvoltage detection/protection circuit on either the high side (input) or low side (output) of the external pass transistor. Recall that internal control circuitry keeps the LTC4211 GATE voltage from ramping up if $V_{FILTER}$ > 1.156V, or when an external fault condition ($V_{FILTER}$ > 1.236V) causes $\overline{FAULT}$ to be asserted low.

### High Side (Input) Overvoltage Protection

As shown in Figure 23, a low power Zener diode can be used to sense an overvoltage condition on the input (high) side of the main 5V supply. In this example, a low bias current 1N4691 Zener diode is chosen to protect the system. Here, the Zener diode is connected from $V_{CC}$ to the LTC4211's FILTER pin (Pin 3 MS10). If the input voltage to the system is greater than 6.8V during start-up, the voltage on the FILTER pin is pulled higher than its 1.156V threshold. As a result, the GATE pin is not allowed to ramp and the second timing cycle will not commence until the supply overvoltage condition is removed. Should the supply overvoltage condition occur during normal operation, internal control logic would trip the electronic circuit breaker and the GATE would be pulled to ground, shutting OFF the external pass transistor. If a lower supply overvoltage threshold is desired, use a Zener diode with a smaller breakdown voltage.

A timing diagram for illustrating LTC4211 operation under a high side overvoltage condition is shown in Figure 24. The start-up sequence in this case (between Time Points 1 and 2) is identical to any other start-up sequence under normal operating conditions. At Time Point 2A, the input supply voltage causes the Zener diode to conduct thereby forcing $V_{FILTER}$ > 1.156V. At Time Point 3, $\overline{FAULT}$ is asserted low and the TIMER pin voltage ramps down. At Time Point 4, the LTC4211 checks if $V_{FILTER}$ < 1.156V.

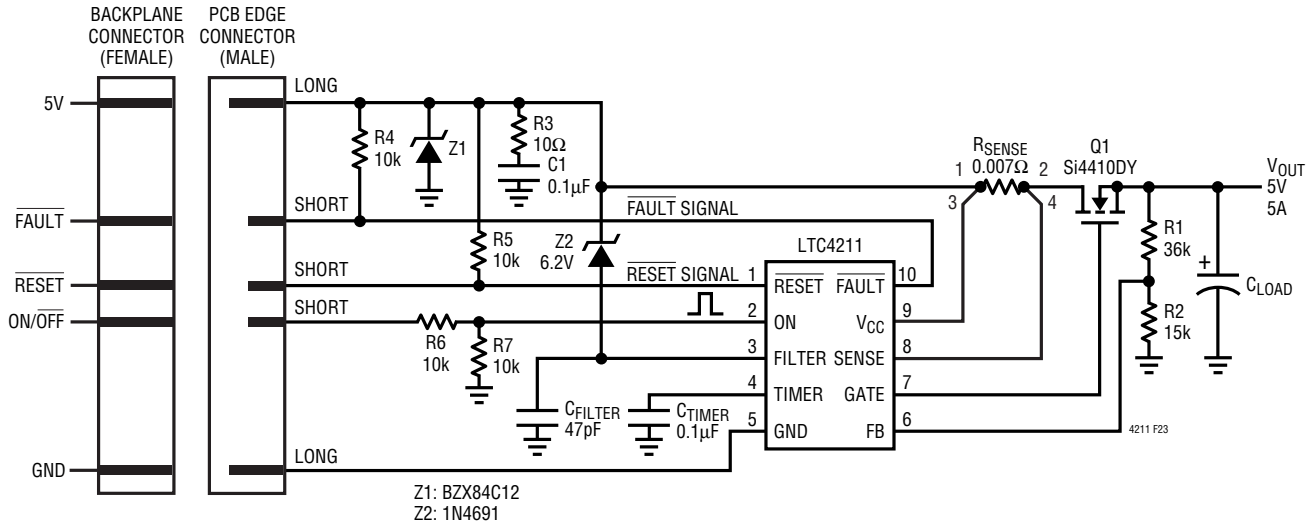



**Figure 23. LTC4211MS High Side Overvoltage Protection Implementation**

## APPLICATIONS INFORMATION

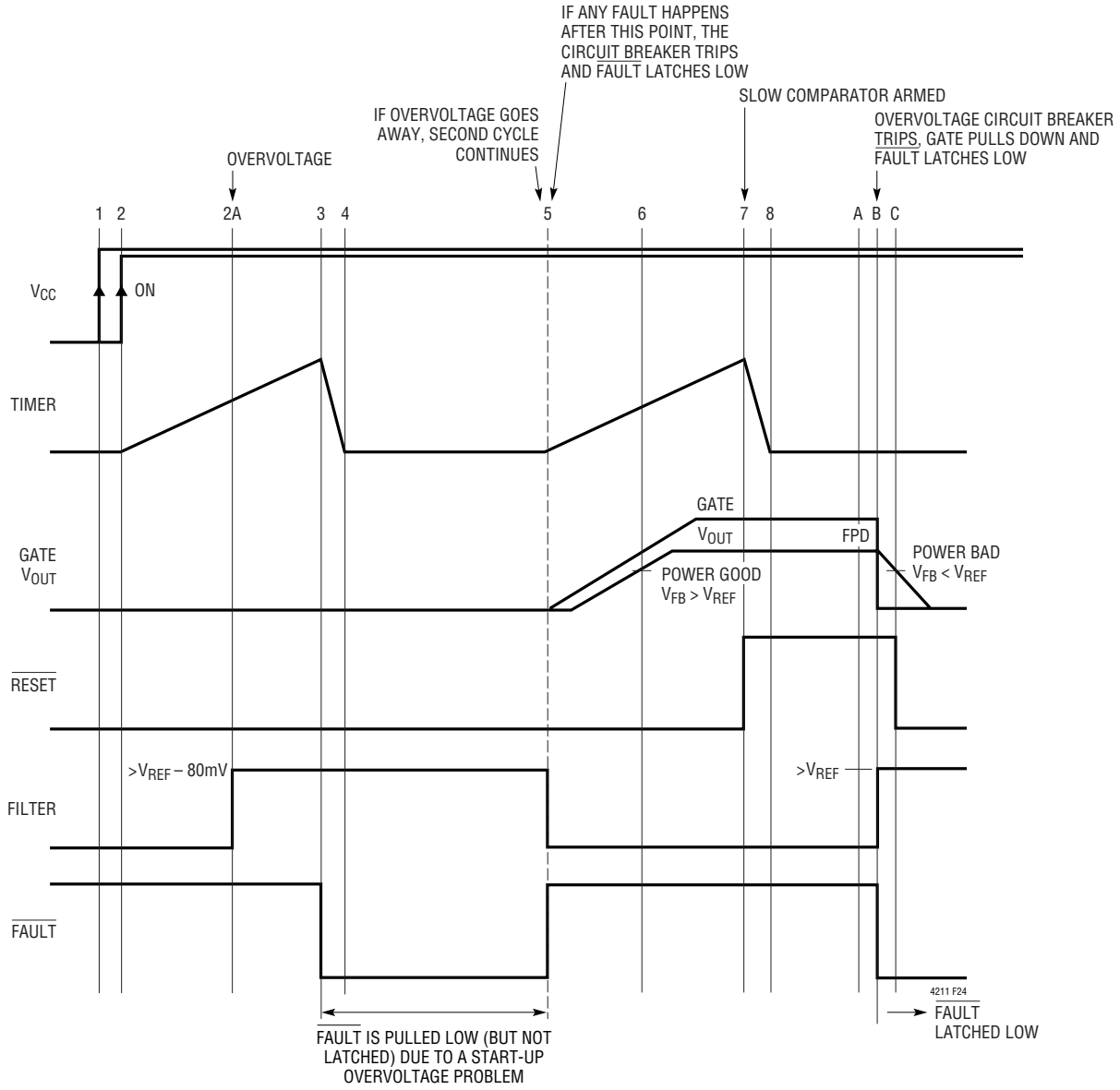



**Figure 24. High Side Overvoltage Protection**

FAULT is asserted low (but not latched) to indicate a start-up failure. Only if the input overvoltage condition is removed before Time Point 5 does the start-up sequence resume at the second timing cycle. At this point in time, the GATE pin voltage is allowed to ramp up, FAULT is pulled to logic high and the circuit breaker is armed. Should, at any time after Time Point 5, a supply overvoltage condition develop ($V_{FILTER}$ > 1.236V), the electronic circuit breaker will trip, the GATE will be pulled low to turn off the external MOSFET and FAULT will be asserted low and latched. This sequence is shown in detail at Time Point B.

### Low Side (Output) Overvoltage Protection

A Zener diode can be used in a similar fashion to detect/protect the system against a supply overvoltage condition on the load (or low) side of the pass transistor. In this case, the Zener diode is connected from the load to the LTC4211's FILTER pin, as shown in Figure 25. Figure 26 illustrates the timing diagram for a low side output overvoltage condition. In this example, the LTC4211 can only sense the overvoltage supply condition after Time Point 5 and the GATE pin has ramped up to its nominal operating value.

## APPLICATIONS INFORMATION

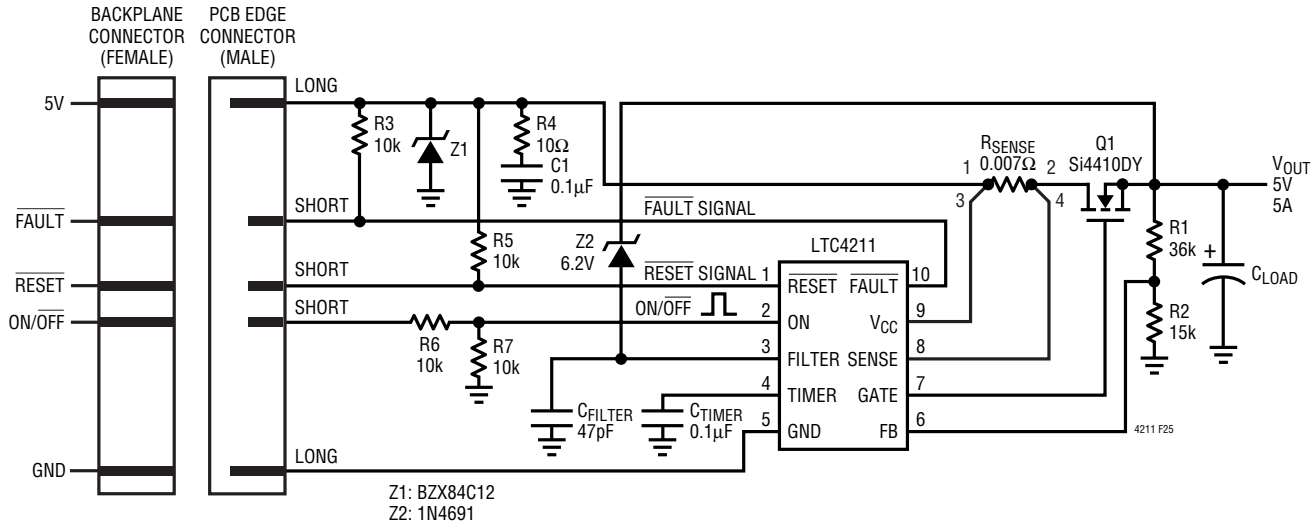



**Figure 25. LTC4211MS Low Side Overvoltage Protection Implementation**

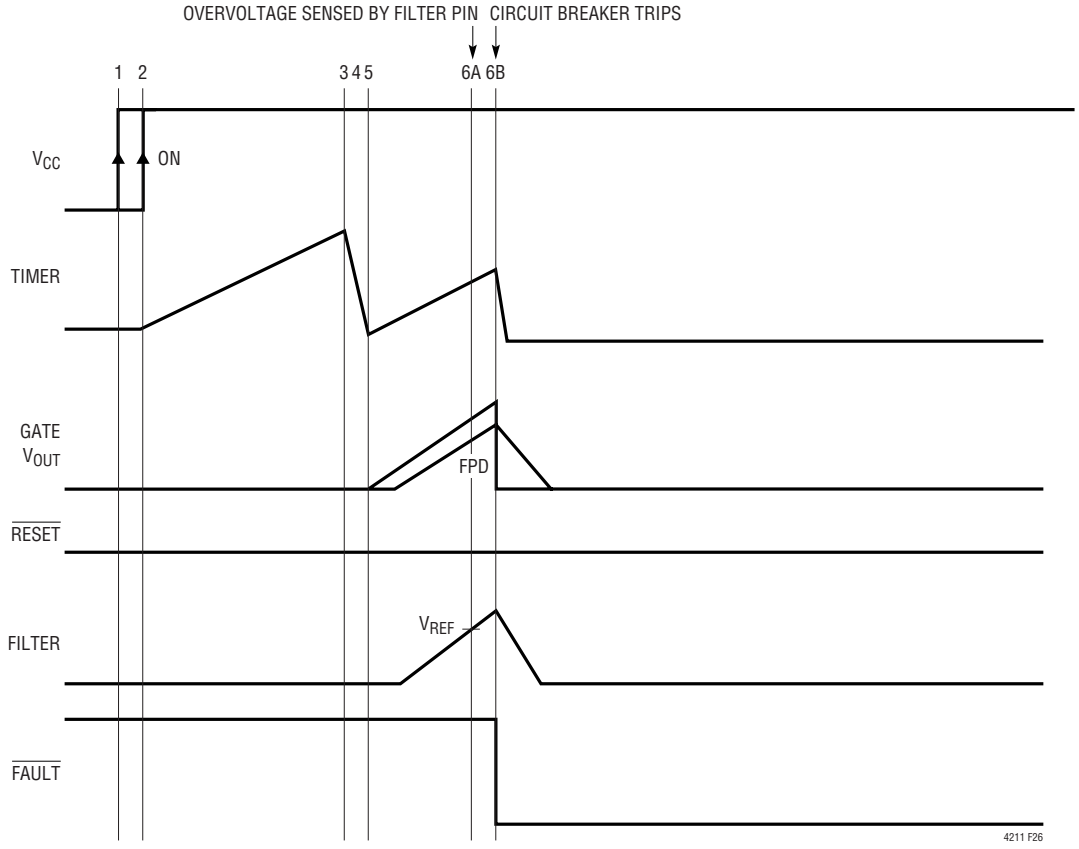



**Figure 26. Low Side Overvoltage Protection**

## APPLICATIONS INFORMATION

After Time Point 5, a supply voltage fault occurs at the load and the Zener diode begins to conduct, causing $V_{FILTER}$ to increase. At Time Point 6A, $V_{FILTER}$ is greater than 1.236V, the circuit breaker is tripped, the GATE pin voltage is pulled to ground and $\overline{FAULT}$ is asserted low and latched.

In either case, the LTC4211 can be configured to automatically initiate a start-up sequence. Please refer to the section on AutoRetry After a Fault for additional information.

### POWER SUPPLY SEQUENCING

A circuit that forces two supply voltages to power up together is shown in Figure 27. The input supply voltages may power up in any sequence, but both input voltages must be within tolerance before Q1 and Q2 turn on. Back-to-back transistors Q1 and Q2 ensure isolation between the two supplies.

When the 5V input powers up before 3.3V, Q1 and Q2 remain off and the 5V output remains off until the 3.3V input is within tolerance as sensed by resistors R1 and R2. When the 3.3V input powers up before 5V, diode D1 will pull up the 5V supply output with it. Once the 5V input powers up and is within tolerance as sensed by R4 and R5, Q1 and Q2 will turn on with a delay time programmable by C1 and pull the 5V output up to its final voltage.

### PCB LAYOUT CONSIDERATIONS

For proper operation of the LTC4211's circuit breaker function, a 4-wire Kelvin connection to the sense resistors is highly recommended. A recommended PCB layout for the sense resistor, the power MOSFET and the GATE drive components around the LTC4211 is illustrated in Figure 28. In Hot Swap applications where load currents can reach 10A or more, narrow PCB tracks exhibit more resistance than wider tracks and operate at more elevated temperatures. Since the sheet resistance of 1 ounce copper foil is approximately 0.54mΩ/square, track resistances add up quickly in high current applications. Thus, to keep PCB track resistance and temperature rise to a minimum, PCB track width must be appropriately sized. Consult Appendix A of LTC Application Note 69 for details on sizing and calculating trace resistances as a function of copper thickness.

In the majority of applications, it will be necessary to use plated-through vias to make circuit connections from component layers to power and ground layers internal to the PC board. For 1 ounce copper foil plating, a good starting point is 1A of DC current per via, making sure the via is properly dimensioned so that solder completely fills any void. For other plating thicknesses, check with your PCB fabrication facility.

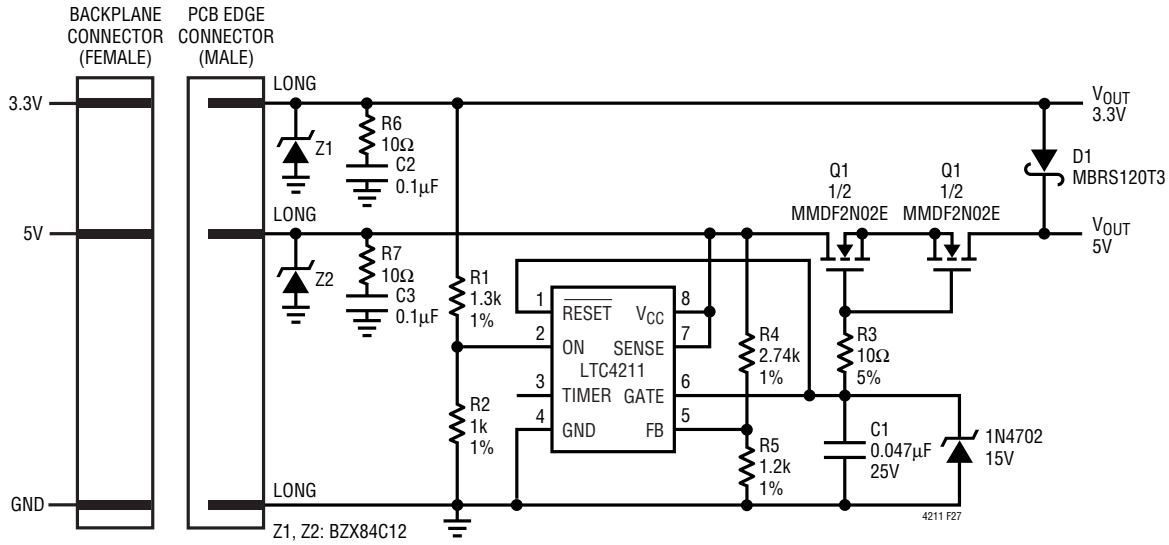



**Figure 27. Power Supply Sequencer**

## APPLICATIONS INFORMATION

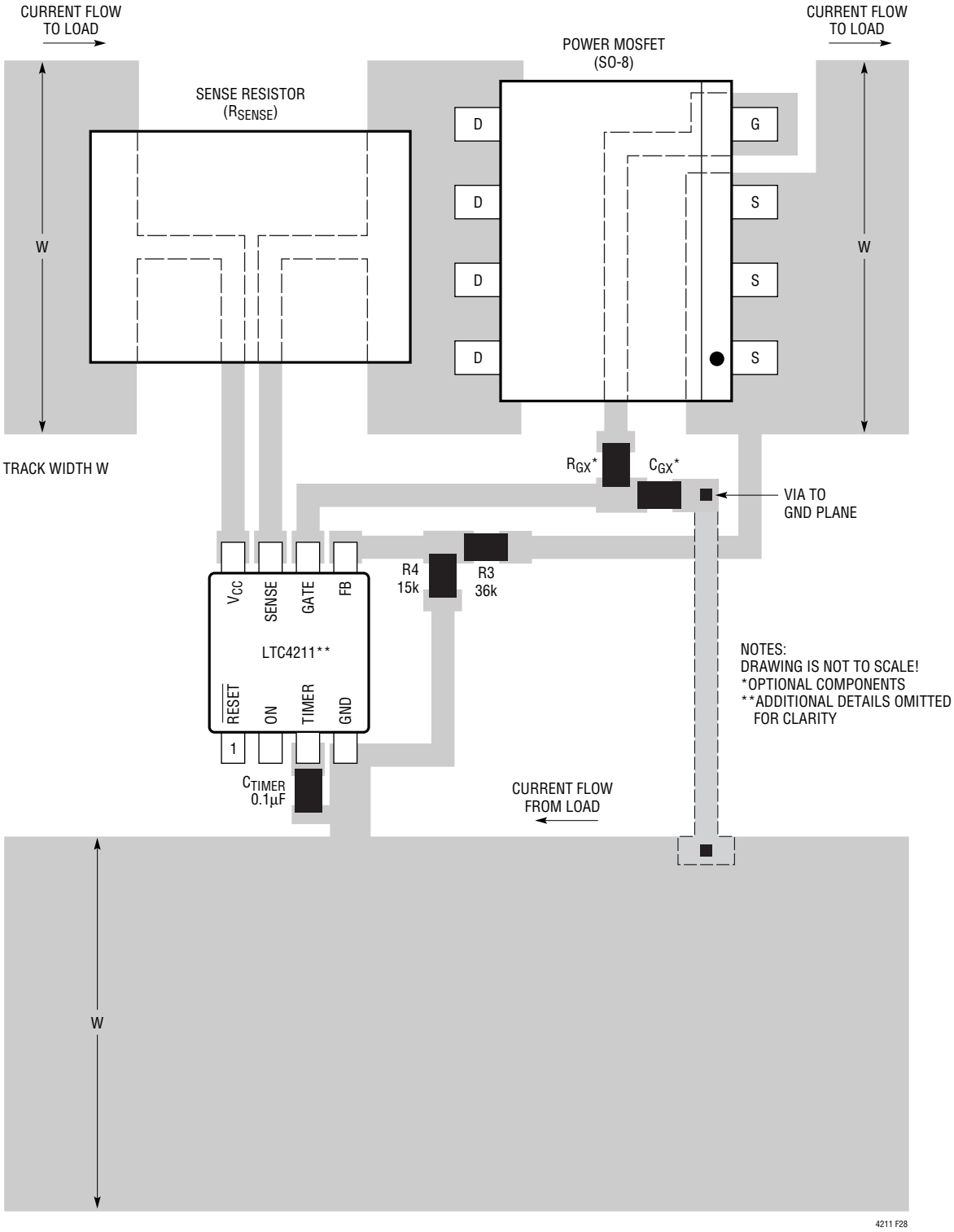



**Figure 28. Recommended Layout for LTC4211 $R_{SENSE}$, Power MOSFET and Feedback Network**

## APPENDIX

Table 4 lists some current sense resistors that can be used with the circuit breaker. Table 5 lists some power MOSFETs that are available. Table 6 lists the web sites of several manufacturers. Since this information is subject to change, please verify the part numbers with the manufacturer.

**Table 4. Sense Resistor Selection Guide**

| CURRENT LIMIT VALUE | PART NUMBER | DESCRIPTION | MANUFACTURER |
|---|---|---|---|
| 1A | LR120601R050 | 0.05Ω 0.5W 1% Resistor | IRC-TT |
| 2A | LR120601R025 | 0.025Ω 0.5W 1% Resistor | IRC-TT |
| 2.5A | LR120601R020 | 0.02Ω 0.5W 1% Resistor | IRC-TT |
| 3.3A | WSL2512R015F | 0.015Ω 1W 1% Resistor | Vishay-Dale |
| 5A | LR251201R010F | 0.01Ω 1.5W 1% Resistor | IRC-TT |
| 10A | WSR2R005F | 0.005Ω 2W 1% Resistor | Vishay-Dale |

**Table 5. N-Channel Selection Guide**

| CURRENT LEVEL (A) | PART NUMBER | DESCRIPTION | MANUFACTURER |
|---|---|---|---|
| 0 to 2 | MMDF3N02HD | Dual N-Channel SO-8<br>$R_{DS(ON)}$ = 0.1Ω, $C_{ISS}$ = 455pF | ON Semiconductor |
| 2 to 5 | MMSF5N02HD | Single N-Channel SO-8<br>$R_{DS(ON)}$ = 0.025Ω, $C_{ISS}$ = 1130pF | ON Semiconductor |
| 5 to 10 | MTB50N06V | Single N-Channel DD Pak<br>$R_{DS(ON)}$ = 0.028Ω, $C_{ISS}$ = 1570pF | ON Semiconductor |
| 10 to 20 | MTB75N05HD | Single N-Channel DD Pak<br>$R_{DS(ON)}$ = 0.0095Ω, $C_{ISS}$ = 2600pF | ON Semiconductor |

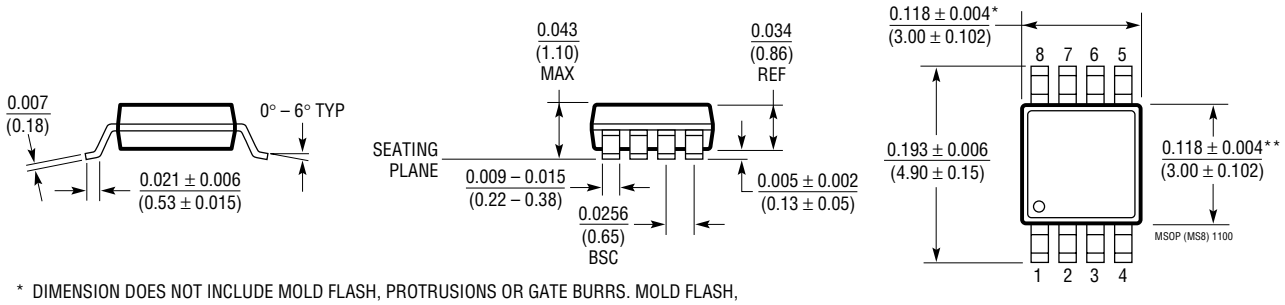
**Table 6. Manufacturers' Web Sites**

| MANUFACTURER | WEB SITE |
|---|---|
| TEMIC Semiconductor | www.temic.com |
| International Rectifier | www.irf.com |
| ON Semiconductor | www.onsemi.com |
| Harris Semiconductor | www.semi.harris.com |
| IRC-TT | www.irctt.com |
| Vishay-Dale | www.vishay.com |
| Vishay-Siliconix | www.vishay.com |
| Diodes, Inc. | www.diodes.com |

## PACKAGE DESCRIPTION

**Dimension in inches (millimeters) unless otherwise noted.**

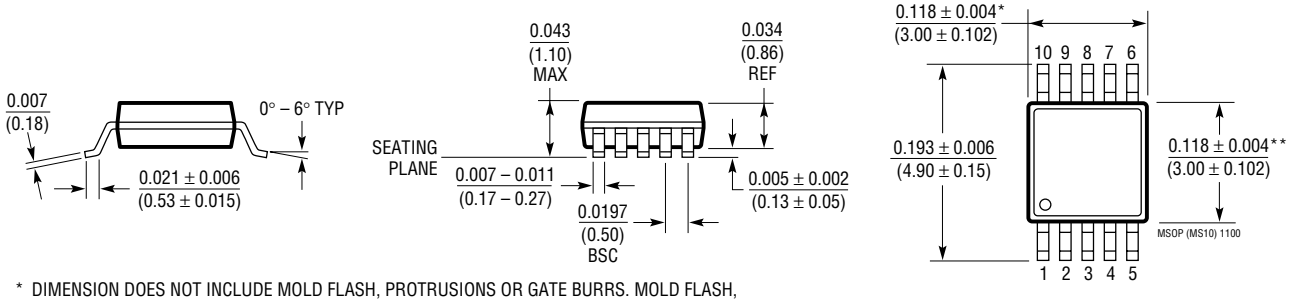
### MS8 Package
### 8-Lead Plastic MSOP
(LTC DWG # 05-08-1660)




* DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

** DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

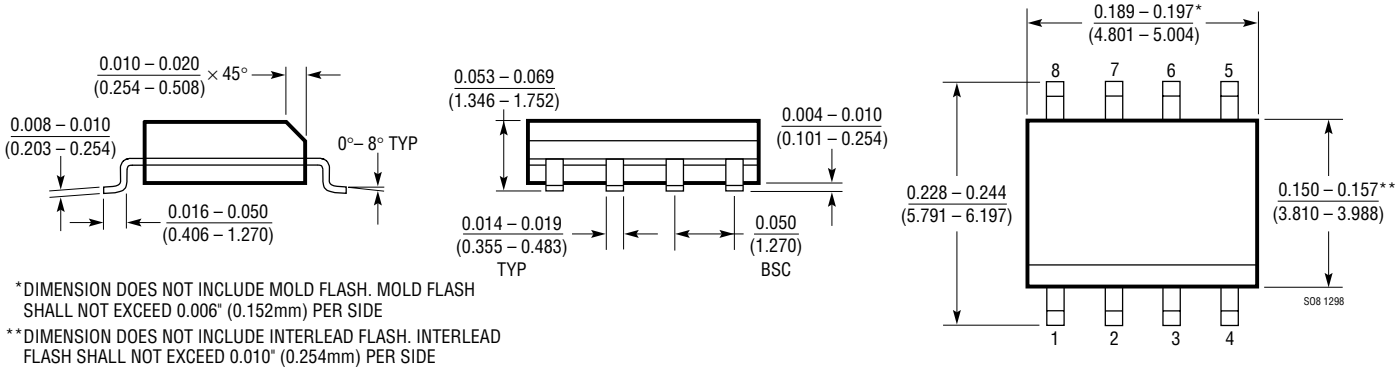
### MS10 Package
### 10-Lead Plastic MSOP
(LTC DWG # 05-08-1661)




* DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

** DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

### S8 Package
### 8-Lead Plastic Small Outline (Narrow 0.150)
(LTC DWG # 05-08-1610)




*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

# TYPICAL APPLICATIONS

### LOW COST OVERVOLTAGE PROTECTION

There is an alternative method to implementing the overvoltage protection using a resistor divider at the FILTER pin (see Figures 29 and 30). In this implementation, the SLOW COMP is NULL in Normal Mode. Only the FAST COMP circuit breaker is available and the current limit level is 150mV/$R_{SENSE}$. During the soft-cycle, the inrush current servo loop is at 50mV/$R_{SENSE}$. So, the heavy load should only turn on at/after the end of second cycle where the $\overline{RESET}$ pin goes high.

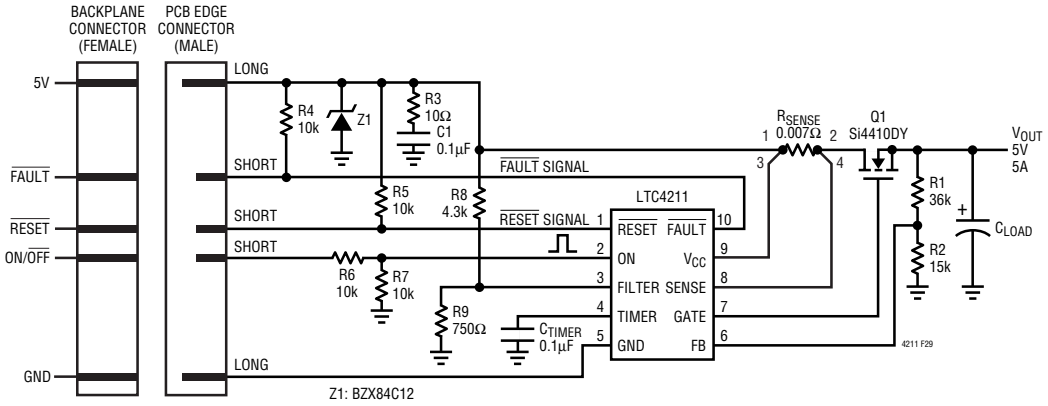



**Figure 29. LTC4211MS High Side Overvoltage Protection Implementation (In Normal Mode, SLOW COMP is Disabled, In Soft-Start Cycle, $I_{SOFTSTART}$ is Still 50mV/$R_{SENSE}$)**

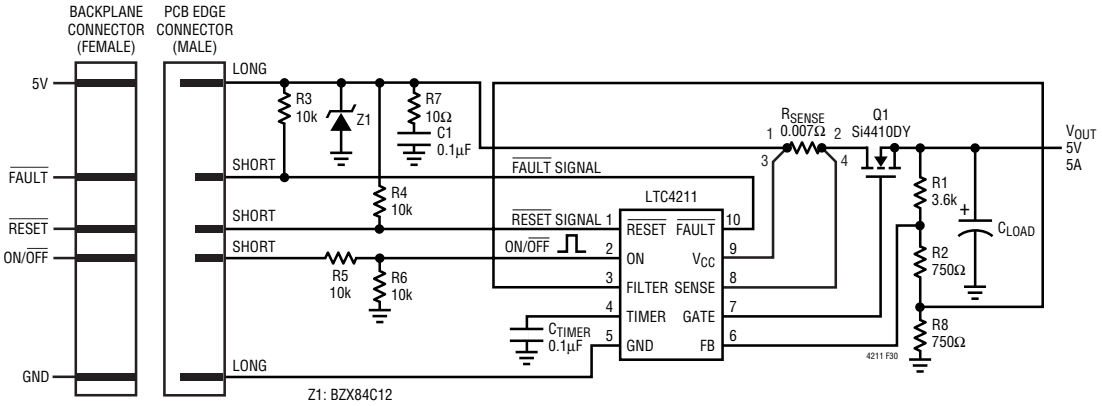



**Figure 30. LTC4211MS Low Side Overvoltage Protection Implementation (In Normal Mode, SLOW COMP is Disabled, In Soft-Start Cycle, $I_{SOFTSTART}$ is Still 50mV/$R_{SENSE}$)**

# RELATED PARTS

| PART NUMBER | DESCRIPTION | COMMENTS |
|---|---|---|
| LTC1421 | Two Channels, Hot Swap Controller | 24-Pin, Operates from 3V to 12V and Supports –12V |
| LTC1422 | Single Channel, Hot Swap Controller | 8-Pin, Operates from 2.7V to 12V |
| LT1640L/LT1640H | Negative Voltage Hot Swap Controller | 8-Pin, Operates from –10V to –80V |
| LT1641 | Positive Voltage Hot Swap Controller | 8-Pin, Operates from 9V to 80V |
| LTC1642 | Single Channel, Hot Swap Controller | 16-Pin, Overvoltage Protection |
| LTC1643L/LTC1643H | PCI Hot Swap Controller | 16-Pin, 3.3V, 5V and ±12V |
| LTC1647 | Dual Channel, Hot Swap Controller | 8-Pin, 16-Pin, Operates from 2.7V to 16.5V |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