LP3941A Cellular Phone Power Management Unit

Check for Samples: LP3941

FEATURES

- **11 low dropout, low noise LDOs.**
- **Dedicated low current LDO for real time clock supply.**
- **Back-up battery charger**
- **A constant current / constant voltage battery charger controller with charge status indication via I^2C compatible interface.**
- **Three open drain drivers to control a RGB LED**
- **I^2C compatible serial interface for maximum flexibility**

APPLICATIONS

- **GSM/EDGE cellular handsets**
- **Wideband CDMA cellular handsets**

DESCRIPTION

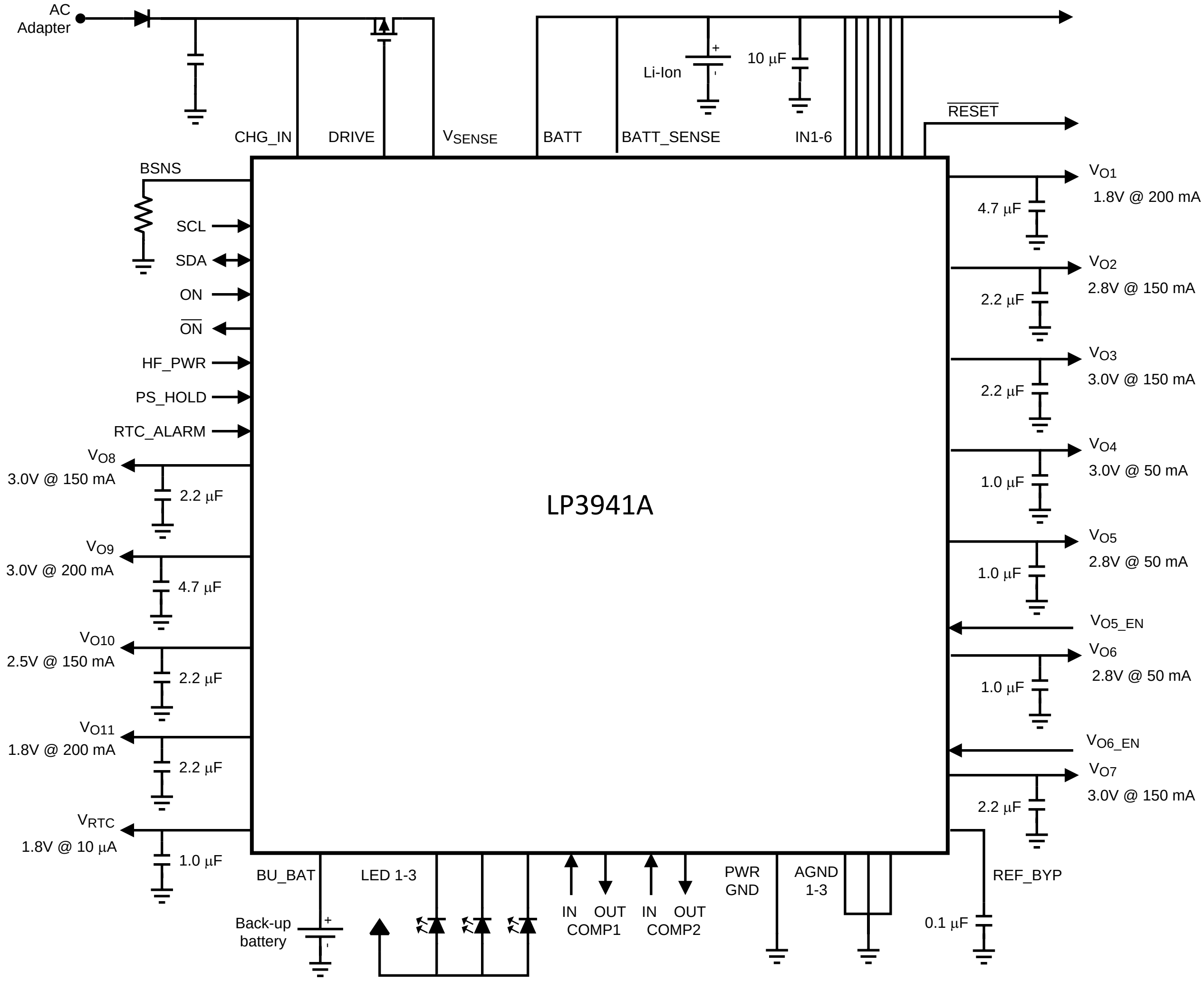
LP3941A is a complete power management IC designed for a cellular phone. It contains 11 low noise low dropout regulators, a linear charger for Li-Ion battery, a backup battery charger, real time clock supply regulator, three open drain drivers, two comparators and high speed I^2C compatible serial interface to program individual regulator output voltages as well as on/off control.

LP3941 is available in a LLP48 package.

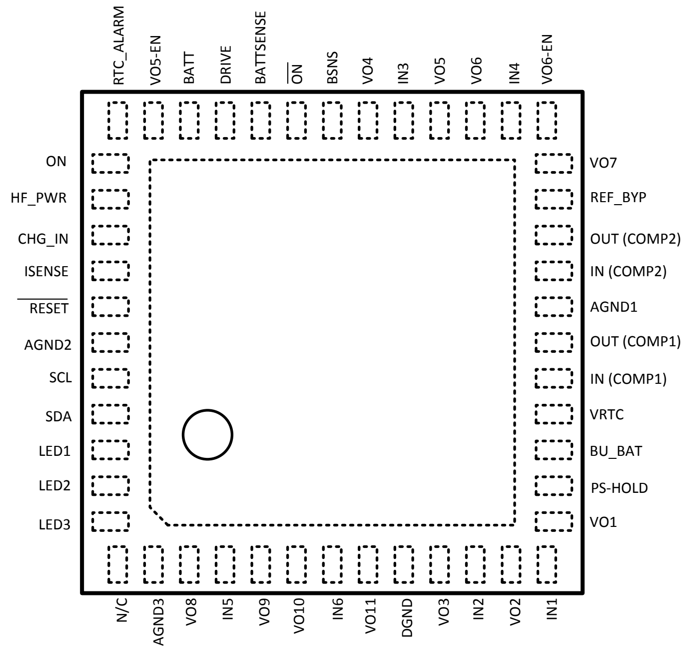
Table 1. Key Specifications

		VALUE	UNIT
3.0V to 5.5V Input Voltage Range			
27 μV_{RMS} Output noise			
2% (typical) Output Voltage Accuracy			
1% Charger Voltage Accuracy			

Typical Application



Connection Diagrams and Package Mark Information



Note: Circle marks pin 1 position. Pin 1 name is N/C.

Figure 1. Top View
48-Pin Leadless Leadframe Package

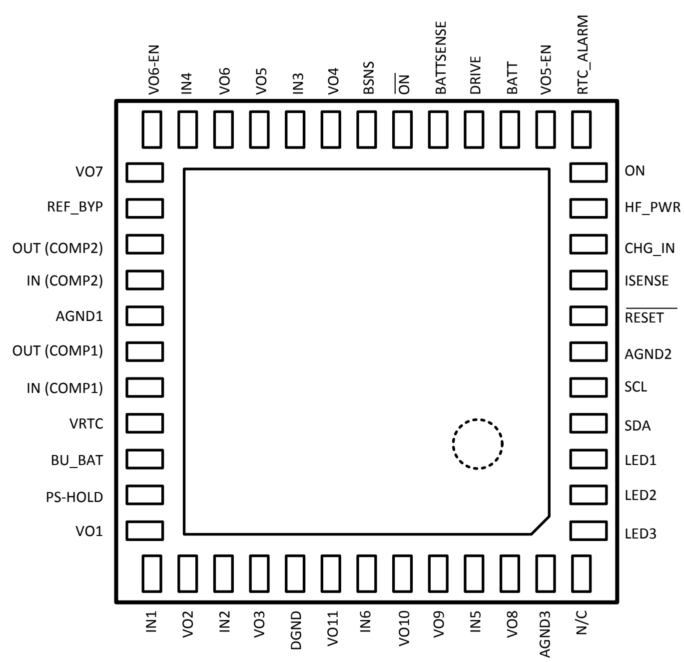
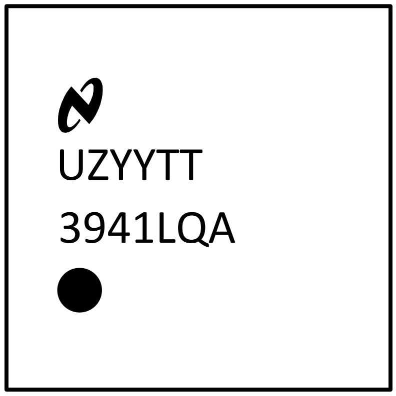


Figure 2. Bottom View
48-Pin Leadless Leadframe Package



Note: The actual physical placement of the package marking will vary from part to part. The package markings "UZYY" designate assembly and manufacturing information. "TT" is a NSC internal code for die traceability. Both will vary considerably. "3941LQA" identifies the device.

Figure 3. Package Mark—Top View

Table 2. Pin Descriptions

Pin #	Name	I/O	Type	Description
1	N/C	-	-	Not used. Connect to ground.
2	AGND3	G	G	Analog ground pin.
3	V_{O8}	O	A	LDO 8 Output
4	IN5	I	P	Input power terminal to LDO's. Must be connected to IN1–4 and IN6.
5	V_{O9}	O	A	LDO 9 output.
6	V_{O10}	O	A	LDO 10 output.
7	IN6	I	P	Input power terminal to LDO's. Must be connected to IN1–5.
8	V_{O11}	O	A	LDO 11 output.
9	DGND	G	G	Ground pin.
10	V_{O3}	O	A	LDO 3 output.
11	IN2	I	P	Input power terminal to LDO's. Must be connected to IN1 and IN3–6.
12	V_{O2}	O	A	LDO 2 output.
13	IN1	I	P	Input power terminal to LDO's. Must be connected to IN2–6.
14	V_{O1}	O	A	LDO 1 output.
15	PS-HOLD	I	D	Active low off key initiated by the micro controller.
16	BU_BAT	I	A	Back-up battery connection.
17	VRTC	O	A	RTC_LDO output.
18	IN (COMP1)	I	A	Non-inverting inout of the comparator 1.
19	OUT (COMP1)	O	A	Output of the comparator 1.
20	AGND1	G	G	Analog ground pin.
21	IN (COMP2)	I	A	Non-inverting input of the comparator 2.
22	OUT (COMP2)	O	A	Output of the comparator 2.
23	REF-BYP	I	A	Reference bypass capacitor.
24	V_{O7}	O	A	LDO 7 output.
25	V_{O6}-EN	I	D	LDO 6 on/off pin. Internal pull-down resistor of 1 MΩ.
26	IN4	I	P	Input power terminal to LDO's. Must be connected to IN1–3 and IN5–6.
27	V_{O6}	O	A	LDO 6 output.

Table 2. Pin Descriptions (continued)

Pin #	Name	I/O	Type	Description
28	V_{O5}	O	A	LDO 5 output.
29	IN3	I	P	Input power terminal to LDO's. Must be connected to IN1–2 and IN4–6.
30	V_{O4}	O	A	LDO 4 output.
31	BSNS	I	A	Main battery ID resistor connection.
32	$\overline{ON}$	O	OD	Inverted open drain output signal of the ON input. Pulled low when ON is pulled high and open drain when $\overline{ON}$ is pulled low. There is no significant delay between the ON signal going high and $\overline{ON}$ pin going low. The delay between ON signal going low and $\overline{ON}$ pin is determined by the pull up current and capacitance connected to this pin.
33	$BATT_{SENSE}$	I	A	Battery voltage sense pin. Should be connected as close to the battery's + terminal as possible.
34	Drive	O	A	Gate drive to the external MOSFET.
35	BATT	O	A	Battery supply input terminal. Must have 10 µF ceramic capacitor to GND.
36	V_{O5}-EN	I	D	LDO 5 on/off pin. Internal pull down resistor of 1 MΩ.
37	RTC_ALARM	I	D	RTC_ALARM input.
38	ON	I	D	Active high power On/Off key. This pin is pulled to GND by an internal 200 kΩ resistor.
39	HF_PWR	I	D	Active high Hands Free connection signal. This pin has an internal 200 kΩ pull down resistor.
40	CHG_IN	I	P	Charger input from a current limited power source. Must have a 1 µF ceramic capacitor to GND.
41	I_{SENSE}	O	A	Charge current sense resistor.
42	$\overline{RESET}$	O	OD	Reset output. Active low. (See Power Up Timing Diagram.)
43	AGND2	G	G	Analog ground pin.
44	SCL	I	D	Serial interface clock input.
45	SDA	I/O	D	Serial interface data input/output.
46	LED1	O	OD	LED driver output pin.
47	LED2	O	OD	LED driver output pin.
48	LED3	O	OD	LED driver output pin.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1) (2)

CHG-IN	−0.3V to +12V
IN1–6, BATT, SDA, SCL, ON, HF-PWR, PS-HOLD, SYS, COMP1_IN, COMP2_IN, CHG_IN, BSNS, V_{O5}-EN, V_{O6}-EN, LED1–3, RTC_ALARM, BU_BAT, V_{RTC}, $\overline{RESET}$, $BATT_{SENSE}$.	−0.3V to +6V
REFBYP, $\overline{ON}$, PS-HOLD, COMP1_OUT, COMP2_OUT to GND	−0.3V to $+V_{BAT}$ + 0.3V
V_{O1} to GND	−0.3V to $+V_{IN1}$ + 0.3V
V_{O2}, V_{O3} to GND	−0.3V to $+V_{IN2}$ + 0.3V
V_{O4}, V_{O5} to GND	−0.3V to $+V_{IN3}$ + 0.3V
V_{O6}, V_{O7} to GND	−0.3V to $+V_{IN4}$ + 0.3V
V_{O8}, V_{O9} to GND	−0.3V to $+V_{IN5}$ + 0.3V
V_{O10}, V_{O11} to GND	−0.3V to $+V_{IN6}$ + 0.3V
GND to GND SLUG	±0.3V
Maximum Continuous Power Dissipation	
(P_{D_MAX}) (3)	3.07W
Junction Temperature (T_{J-MAX})	150°C
Storage Temperature Range	−65°C to +150°C
Maximum Lead Temperature (Soldering)	(4)
ESD Ratings (5)	
All Pins	2 kV HBM 200V MM

(1) All voltages are with respect to the potential at the GND pin.
(2) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics tables.
(3) The amount of Absolute Maximum power dissipation allowed for the device depends on the ambient temperature and can be calculated using the formula $P = (T_J – T_A)/\theta_{JA}$, where T_J is the junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.Junction-to-ambient thermal resistance is highly application and board-layout dependent. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design.Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J = 150ºC (typ.) and disengages at T_J = 140ºC (typ.).
(4) For detailed soldering specifications and information, please refer to National Semiconductor Application Note 1187: Leadless Leadframe Package (LLP) (AN-1187).
(5) The Human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. (MIL-STD-883 3015.7) The machine model is a 200 pF capacitor discharged directly into each pin. (EAIJ)

Operating Ratings (1) (2)

V_{IN}	3.0V to 6.0V
V_{EN}	0V to (V_{IN} + 0.3V)
Junction Temperature (T_J) Range	−40°C to +125°C
Ambient Temperature (T_A) Range (3)	−40°C to +85°C

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics tables.
(2) All voltages are with respect to the potential at the GND pin.
(3) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature ($T_{J-MAX-OP}$ = 125°C), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A-MAX} = T_{J-MAX-OP} − (\theta_{JA} \times P_{D-MAX})$.

Table 3. Thermal Properties (1)

Junction-to-Ambient Thermal Resistance (θ_{JA})	26°C/W

(1) Junction-to-ambient thermal resistance (θ_{JA}) is taken from a thermal modeling result, performed under the conditions and guidelines set forth in the JEDEC standard JESD51–7. The test board is a 4-layer FR-4 board measuring 102 mm x 76 mm x 1.6 mm with a 2x1 array of thermal vias. The ground plane on the board is 50 mm x 50 mm. Thickness of copper layers are 36 µm/1.8 µm/18 µm/36 µm (1.5 oz/1 oz/1 oz/1.5 oz). Ambient temperature in simulation is 22°C, still air. Power dissipation is 1W.Junction-to-ambient thermal resistance is highly application and board-layout dependent. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design.The value of θ_{JA} of this product can vary significantly, depending on PCB material, layout, and environmental conditions. In applications where high maximum power dissipation exists (high V_{IN}, high I_{OUT}), special care must be paid to thermal dissipation issues. For more information on these topics, please refer to *Application Note 1187: Leadless Leadframe Package (LLP) and the Power Efficiency and Power Dissipation* section of this datasheet.

Electrical Characteristics

Unless otherwise noted, V_{IN} = 2.5V to 5.5V, C_{IN} (IN1–6) = 4.7 µF, C_{OUT} (V_{O1} and V_{O9}) = 4.7 µF, C_{OUT} (V_{O2}, V_{O3}, V_{O7}, V_{O8}, V_{O10} and V_{O11}) = 2.2 µF, C_{OUT} (V_{O4} to V_{O6}) = 1 µF, C_{OUT} (V_{RTC}) = 1 µF ceramic, C_{BYP} = 0.1 µF. Typical values and limits appearing in normal type apply for T_J = 25°C. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, −40 to +125°C. (1) (2) (3) (4)

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_Q	Shutdown Supply Current	V_{BATT} = 2.1V, UVLO on, internal logic generator on, V_{RTC} off, all other circuits off.		14		µA
	No Load Supply Current, LDO 1 & 3 & 5 on	V_{BATT} = 3.6V, LDOs V_{O1}, V_{O3} and V_{O5} on, back-up battery charger and V_{RTC} on, charger disconnected, comparator 1 & 2 on.		310		µA
	No Load Supply Current	V_{BATT} = 3.6V, All LDOs on, charger disconnected.		500		µA
BATTERY UNDER VOLTAGE LOCKOUT						
V_{UVLO-R}	Under Voltage Lock-Out	V_{BATT} Rising	**2.91**	3.1	**3.32**	V
V_{UVLO-F}	Under Voltage Lock-Out	V_{BATT} Falling	**2.15**	2.49	**2.85**	V
V_{TH-POR}	Power-On Reset Threshold	V_{BATT} Falling Edge	**1**	1.7	**2.3**	V
THERMAL SHUTDOWN						
	Threshold Hysteresis			160 10		°C
OUTPUT CAPACITORS						
C_{OUT}	Capacitance ESR		**1** **5**		**20** **500**	µF mΩ
LOGIC AND CONTROL INPUTS						
V_{IL}	Input Low Level	PS-HOLD, ON, BSNS, HF-PWR, RTC_ALARM, SDA, SCL, V_{O5}-EN, V_{O6}-EN. 2.5V ≤ V_{BATT} ≤ 5.5V			**0.4**	V
V_{IH}	Input High Level	PS-HOLD, ON, BSNS, HF-PWR, RTC_ALARM, SDA, SCL, V_{O5}-EN, V_{O6}-EN. 2.5V ≤ V_{BATT} ≤ 5.5V	**2.0**			V
I_{IL}	Logic Input Current	SDA, SCL 0V ≤ V_{IN} ≤ 5.5V	**−5**		**+5**	µA
	PS-HOLD Input Current	0V ≤ V_{IN} ≤ V_{BATT}	**−5**		**+5**	µA
R_{IN}	ON, HF_PWR Pull-Down Resistance to GND			200		kΩ
	V_{O5}-EN, V_{O6}-EN, RTC_ALARM Pull Down Resistance to GND			1700		kΩ
LOGIC AND CONTROL OUTPUTS						
V_{OL}	$\overline{ON}$ Output Low Level	I_{SINK} = 1 mA			**0.4**	V
$I_{LEAKAGE}$	$\overline{ON}$ Open Drain Leakage	$V_{\overline{ON}}$ = 4.2V			**5**	µA
I_{O-MAX}	$\overline{ON}$, $\overline{RESET}$, OUT (COMP1), OUT (COMP2) Output Maximum Sink/Source Current				**5**	mA

(1) All voltages are with respect to the potential at the GND pin.
(2) All limits are guaranteed by design, test and/or statistical analysis. All electrical characteristics having room-temperature limits are tested during production with T_J = 25°C. All hot and cold limits are guaranteed by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(3) Capacitors: Low-ESR Surface-Mount Ceramic Capacitors are (MLCCs) used in setting electrical characteristics.
(4) Guaranteed by design.

V_{O1} LDO Electrical Characteristics

Unless otherwise noted, $V_{IN} = V_{BATT} = 3.6V$. Typical values and limits appearing in normal type apply for $T_J = 25°C$. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, −40 to +85°C. (1) (2) (3)

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OUT} Accuracy	Output Voltage	1 mA ≤ I_{OUT} ≤ 200 mA, V_{OUT} = 2.2V 3.0V ≤ V_{BATT} = V_{IN} ≤ 5.5V	**−3**	±1.0	**+3**	%
V_{OUT} Range	Programmable Output Voltage Range	0 µA ≤ I_{OUT} ≤ 200 mA Programming Resolution = 100 mV	**1.5**	1.8	**3.0**	V
I_{OUT}	Output Current	$(V_{OUT} + 0.25V, 3.0V)_{MAX}$ ≤ V_{BATT} V_{BATT} = V_{IN} ≤ 5.5V			**200**	mA
	Output Current Limit	V_{OUT} = 0V		780		
V_{IN}–V_{OUT}	Dropout Voltage	I_{OUT} = 100 mA		70	**254**	mV
ΔV_{OUT}	Line Regulation	$(V_{OUT} + 0.25V, 3.0V)_{MAX}$ ≤ V_{BATT} V_{BATT} = V_{IN} ≤ 5.5V, I_{OUT} = 100 mA		3		mV
	Load Regulation	V_{IN} = 3.6V, 1 mA ≤ I_{OUT} ≤ 200 mA		10		
e_N	Output Noise Voltage	10 Hz ≤ f ≤ 100 kHz, C_{OUT} = 4.7 µF		27		μV_{RMS}
PSRR	Power Supply Ripple Rejection Ratio	f = 217 Hz, C_{OUT} = 4.7 µF		60		dB
C_{OUT}	Output Capacitance	1 mA ≤ I_{OUT} ≤ 200 mA	**2**		**20**	µF
	Output Capacitor ESR		**5**		**500**	mΩ
$t_{START-UP}$	Start-Up Time from Shutdown ON-signal	C_{OUT} = 4.7 µF, I_{OUT} = 200 mA (4)	**80**	120	**180**	µs

(1) All voltages are with respect to the potential at the GND pin.
(2) All limits are guaranteed by design, test and/or statistical analysis. All electrical characteristics having room-temperature limits are tested during production with T_J = 25°C. All hot and cold limits are guaranteed by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(3) Capacitors: Low-ESR Surface-Mount Ceramic Capacitors are (MLCCs) used in setting electrical characteristics.
(4) Guaranteed by design.

V_{O2} LDO Electrical Characteristics

Unless otherwise noted, $V_{IN} = V_{BATT} = 3.6V$. Typical values and limits appearing in normal type apply for $T_J = 25°C$. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, −40 to +125°C. (1) (2) (3)

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OUT} Accuracy	Output Voltage	1 mA ≤ I_{OUT} ≤ 200 mA, V_{OUT} = 2.2V 3.0V ≤ V_{BATT} = V_{IN} ≤ 5.5V	**−3**	±1.0	**+3**	%
V_{OUT} Range	Programmable Output Voltage Range	0 µA ≤ I_{OUT} ≤ 200 mA Programming Resolution = 100 mV	**1.5**	2.8	**3.0**	V
I_{OUT}	Output Current	$(V_{OUT} + 0.25V, 3.0V)_{MAX} \le V_{BATT}$ $V_{BATT} = V_{IN} \le 5.5V$			**150**	mA
	Output Current Limit	V_{OUT} = 0V		540		
V_{IN}–V_{OUT}	Dropout Voltage	I_{OUT} = 75 mA		30	**174**	mV
ΔV_{OUT}	Line Regulation	$(V_{OUT} + 0.25V, 3.0V)_{MAX} \le V_{BATT}$ $V_{BATT} = V_{IN} \le 5.5V$, I_{OUT} = 75 mA		3		mV
	Load Regulation	V_{IN} = 3.6V, 1 mA ≤ I_{OUT} ≤ 150 mA		12	**41**	
e_N	Output Noise Voltage	10 Hz ≤ f ≤ 100 kHz, C_{OUT} = 2.2 µF		27		μV_{RMS}
PSRR	Power Supply Ripple Rejection Ratio	f = 217 Hz, C_{OUT} = 2.2 µF		57		dB
I_{GND}	Ground Current	I_{OUT} = 100 µA		30		µA
C_{OUT}	Output Capacitance	0 mA ≤ I_{OUT} ≤ 150 mA	**2**		**20**	µF
	Output Capacitor ESR		**5**		**500**	mΩ
$t_{START-UP}$	Start-Up Time from Shutdown	C_{OUT} = 2.2 µF, I_{OUT} = 150 mA (4)		60		µs

(1) All voltages are with respect to the potential at the GND pin.
(2) All limits are guaranteed by design, test and/or statistical analysis. All electrical characteristics having room-temperature limits are tested during production with T_J = 25°C. All hot and cold limits are guaranteed by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(3) Capacitors: Low-ESR Surface-Mount Ceramic Capacitors are (MLCCs) used in setting electrical characteristics.
(4) Guaranteed by design.

V_{O3} LDO Electrical Characteristics

Unless otherwise noted, $V_{IN} = V_{BATT}$ = 3.6V. Typical values and limits appearing in normal type apply for T_J = 25°C. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, −40 to +125°C. [1] [2] [3]

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OUT} Accuracy	Output Voltage	1 mA ≤ I_{OUT} ≤ 150 mA, V_{OUT} = 2.7V 3.0V ≤ $V_{BATT} = V_{IN}$ ≤ 5.5V	**−3**	±1.0	**+3**	%
V_{OUT} Range	Programmable Output Voltage Range	0 µA ≤ I_{OUT} ≤ 150 mA Programming Resolution = 100 mV	**2.5**	3.0	**3.2**	V
I_{OUT}	Output Current	$(V_{OUT}$ + 0.25V, 3.0V$)_{MAX}$ ≤ V_{BATT} $V_{BATT} = V_{IN}$ ≤ 5.5V			**150**	mA
	Output Current Limit	V_{OUT} = 0V		520		mA
V_{IN}–V_{OUT}	Dropout Voltage	I_{OUT} = 75 mA		30	**156**	mV
ΔV_{OUT}	Line Regulation	$(V_{OUT}$ + 0.25V, 3.0V$)_{MAX}$ ≤ V_{BATT} $V_{BATT} = V_{IN}$ ≤ 5.5V, I_{OUT} = 75 mA		3		mV
	Load Regulation	V_{IN} = 3.6V, 1 mA ≤ I_{OUT} ≤ 150 mA		12	**41**	mV
e_N	Output Noise Voltage	10 Hz ≤ f ≤ 100 kHz, C_{OUT} = 2.2 µF		27		μV_{RMS}
PSRR	Power Supply Ripple Rejection Ratio	f = 217 Hz, C_{OUT} = 2.2 µF		56		dB
I_{GND}	Ground Current	I_{OUT} = 500 µA		30		µA
C_{OUT}	Output Capacitance	0 mA ≤ I_{OUT} ≤ 150 mA	**2**		**20**	µF
	Output Capacitor ESR		**5**		**500**	mΩ
$t_{START-UP}$	Start-Up Time from Shutdown	C_{OUT} = 2.2 µF, I_{OUT} = 150 mA [4]		60		µs

(1) All voltages are with respect to the potential at the GND pin.
(2) All limits are guaranteed by design, test and/or statistical analysis. All electrical characteristics having room-temperature limits are tested during production with T_J = 25°C. All hot and cold limits are guaranteed by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(3) Capacitors: Low-ESR Surface-Mount Ceramic Capacitors are (MLCCs) used in setting electrical characteristics.
(4) Guaranteed by design.

V_{O4} LDO Electrical Characteristics

Unless otherwise noted, $V_{IN} = V_{BATT} = 3.6V$. Typical values and limits appearing in normal type apply for $T_J = 25°C$. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, −40 to +125°C. [1] [2] [3]

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OUT} Accuracy	Output Voltage	1 mA ≤ I_{OUT} ≤ 50 mA, V_{OUT} = 2.2V 3.0V ≤ $V_{BATT} = V_{IN}$ ≤ 5.5V	**−3**	±1.0	**+3**	%
V_{OUT} Range	Programmable Output Voltage Range	0 µA ≤ I_{OUT} ≤ 50 mA Programming Resolution = 100 mV	**1.5**	3.0	**3.0**	V
I_{OUT}	Output Current	$(V_{OUT} + 0.25V, 3.0V)_{MAX} \le V_{BATT}$ $V_{BATT} = V_{IN}$ ≤ 5.5V			**50**	mA
	Output Current Limit	V_{OUT} = 0V		140		mA
$V_{IN}–V_{OUT}$	Dropout Voltage	I_{OUT} = 25 mA		7	**90**	mV
ΔV_{OUT}	Line Regulation	$(V_{OUT} + 0.25V, 3.0V)_{MAX} \le V_{BATT}$ $V_{BATT} = V_{IN}$ ≤ 5.5V, I_{OUT} = 25 mA		3		mV
	Load Regulation	V_{IN} = 3.6V, 1 mA ≤ I_{OUT} ≤ 50 mA		4	**31**	mV
e_N	Output Noise Voltage	10 Hz ≤ f ≤ 100 kHz, C_{OUT} = 1.0 µF		27		$µV_{RMS}$
PSRR	Power Supply Ripple Rejection Ratio	f = 217 Hz, C_{OUT} = 1.0 µF		56		dB
I_{GND}	Ground Current	I_{OUT} = 100 µA		30		µA
C_{OUT}	Output Capacitance	0 µA ≤ I_{OUT} ≤ 50 mA	**1**		**20**	µF
	Output Capacitor ESR		**5**		**500**	mΩ
$t_{START-UP}$	Start-Up Time from Shutdown	C_{OUT} = 1.0 µF, I_{OUT} = 50 mA [4]		60		µs

(1) All voltages are with respect to the potential at the GND pin.
(2) All limits are guaranteed by design, test and/or statistical analysis. All electrical characteristics having room-temperature limits are tested during production with $T_J = 25°C$. All hot and cold limits are guaranteed by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(3) Capacitors: Low-ESR Surface-Mount Ceramic Capacitors are (MLCCs) used in setting electrical characteristics.
(4) Guaranteed by design.

V_{O5} LDO Electrical Characteristics

Unless otherwise noted, V_{IN} = V_{BATT} = 3.6V. Typical values and limits appearing in normal type apply for T_J = 25°C. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, −40 to +125°C. (1) (2) (3)

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OUT} Accuracy	Output Voltage	1 mA ≤ I_{OUT} ≤ 50 mA, V_{OUT} = 2.2V 3.0V ≤ V_{BATT} = V_{IN} ≤ 5.5V	**−3**	±1.0	**+3**	%
V_{OUT} Range	Programmable Output Voltage Range	0 µA ≤ I_{OUT} ≤ 50 mA Programming Resolution = 100 mV	**2.5**	2.8	**3.2**	V
I_{OUT}	Output Current	(V_{OUT} + 0.25V, 3.0V)$_{MAX}$ ≤ V_{BATT} V_{BATT} = V_{IN} ≤ 5.5V			**50**	mA
	Output Current Limit	V_{OUT} = 0V		160		
V_{IN}–V_{OUT}	Dropout Voltage	I_{OUT} = 25 mA		7	**90**	mV
ΔV_{OUT}	Line Regulation	(V_{OUT} + 0.25V, 3.0V)$_{MAX}$ ≤ V_{BATT} V_{BATT} = V_{IN} ≤ 5.5V, I_{OUT} = 25 mA		3		mV
	Load Regulation	V_{IN} = 3.6V, 1 mA ≤ I_{OUT} ≤ 50 mA		4	**31**	
e_N	Output Noise Voltage	10 Hz ≤ f ≤ 100 kHz, C_{OUT} = 1.0 µF		27		μV_{RMS}
PSRR	Power Supply Ripple Rejection Ratio	f = 217 Hz, C_{OUT} = 1.0 µF		56		dB
I_{GND}	Ground Current	I_{OUT} = 100 µA		30		µA
C_{OUT}	Output Capacitance	0 µA ≤ I_{OUT} ≤ 50 mA	**1**		**20**	µF
	Output Capacitor ESR		**5**		**500**	mΩ
$t_{START-UP}$	Start-Up Time from Shutdown	C_{OUT} = 1.0 µF, I_{OUT} = 50 mA (4)		60		µs

(1) All voltages are with respect to the potential at the GND pin.
(2) All limits are guaranteed by design, test and/or statistical analysis. All electrical characteristics having room-temperature limits are tested during production with T_J = 25°C. All hot and cold limits are guaranteed by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(3) Capacitors: Low-ESR Surface-Mount Ceramic Capacitors are (MLCCs) used in setting electrical characteristics.
(4) Guaranteed by design.

V_{O6} LDO Electrical Characteristics

Unless otherwise noted, V_{IN} = V_{BATT} = 3.6V. Typical values and limits appearing in normal type apply for T_J = 25°C. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, −40 to +125°C. (1) (2) (3)

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OUT} Accuracy	Output Voltage	1 mA ≤ I_{OUT} ≤ 50 mA, V_{OUT} = 2.7V 3.0V ≤ V_{BATT} = V_{IN} ≤ 5.5V	**−3**	±1.0	**+3**	%
V_{OUT} Range	Programmable Output Voltage Range	0 µA ≤ I_{OUT} ≤ 50 mA Programming Resolution = 100 mV	**2.5**	2.8	**3.2**	V
I_{OUT}	Output Current	$(V_{OUT}$ + 0.25V, 3.0V$)_{MAX}$ ≤ V_{BATT} V_{BATT} = V_{IN} ≤ 5.5V			**50**	mA
	Output Current Limit	V_{OUT} = 0V		170		mA
V_{IN}–V_{OUT}	Dropout Voltage	I_{OUT} = 25 mA		7	**90**	mV
ΔV_{OUT}	Line Regulation	$(V_{OUT}$ + 0.25V, 3.0V$)_{MAX}$ ≤ V_{BATT} V_{BATT} = V_{IN} ≤ 5.5V, I_{OUT} = 25 mA		3		mV
	Load Regulation	V_{IN} = 3.6V, 1 mA ≤ I_{OUT} ≤ 50 mA		4	**31**	mV
e_N	Output Noise Voltage	10 Hz ≤ f ≤ 100 kHz, C_{OUT} = 1.0 µF		27		μV_{RMS}
PSRR	Power Supply Ripple Rejection Ratio	f = 217 Hz, C_{OUT} = 1.0 µF		56		dB
I_{GND}	Ground Current	I_{OUT} = 100 µA		30		µA
C_{OUT}	Output Capacitance	0 µA ≤ I_{OUT} ≤ 50 mA	**1**		**20**	µF
	Output Capacitor ESR		**5**		**500**	mΩ
$t_{START-UP}$	Start-Up Time from Shutdown	C_{OUT} = 1.0 µF, I_{OUT} = 50 mA (4)		60		µs

(1) All voltages are with respect to the potential at the GND pin.
(2) All limits are guaranteed by design, test and/or statistical analysis. All electrical characteristics having room-temperature limits are tested during production with T_J = 25°C. All hot and cold limits are guaranteed by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(3) Capacitors: Low-ESR Surface-Mount Ceramic Capacitors are (MLCCs) used in setting electrical characteristics.
(4) Guaranteed by design.

V_{O7} LDO Electrical Characteristics

Unless otherwise noted, V_{IN} = V_{BATT} = 3.6V. Typical values and limits appearing in normal type apply for T_J = 25°C. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, −40 to +125°C. (1) (2) (3)

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OUT} Accuracy	Output Voltage	1 mA ≤ I_{OUT} ≤ 150 mA, V_{OUT} = 2.7V 3.0V ≤ V_{BATT} = V_{IN} ≤ 5.5V	**−3**	±1.0	**+3**	%
V_{OUT} Range	Programmable Output Voltage Range	0 µA ≤ I_{OUT} ≤ 150 mA Programming Resolution = 100 mV	**2.5**	3.0	**3.2**	V
I_{OUT}	Output Current	(V_{OUT} + 0.25V, 3.0V)$_{MAX}$ ≤ V_{BATT} V_{BATT} = V_{IN} ≤ 5.5V			**150**	mA
	Output Current Limit	V_{OUT} = 0V		500		
V_{IN}–V_{OUT}	Dropout Voltage	I_{OUT} = 75 mA		30	**173**	mV
ΔV_{OUT}	Line Regulation	(V_{OUT} + 0.25V, 3.0V)$_{MAX}$ ≤ V_{BATT} V_{BATT} = V_{IN} ≤ 5.5V, I_{OUT} = 75 mA		3		mV
	Load Regulation	V_{IN} = 3.6V, 1 mA ≤ I_{OUT} ≤ 150 mA		10	**41**	
e_N	Output Noise Voltage	10 Hz ≤ f ≤ 100 kHz, C_{OUT} = 2.2 µF		27		μV_{RMS}
PSRR	Power Supply Ripple Rejection Ratio	f = 217 Hz, C_{OUT} = 2.2 µF		57		dB
I_{GND}	Ground Current	I_{OUT} = 100 µA		30		µA
C_{OUT}	Output Capacitance	0 µA ≤ I_{OUT} ≤ 150 mA	**2**		**20**	µF
	Output Capacitor ESR		**5**		**500**	mΩ
$t_{START-UP}$	Start-Up Time from Shutdown	C_{OUT} = 2.2 µF, I_{OUT} = 150 mA Note 10		60		µs

(1) All voltages are with respect to the potential at the GND pin.
(2) All limits are guaranteed by design, test and/or statistical analysis. All electrical characteristics having room-temperature limits are tested during production with T_J = 25°C. All hot and cold limits are guaranteed by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(3) Capacitors: Low-ESR Surface-Mount Ceramic Capacitors are (MLCCs) used in setting electrical characteristics.

V_{O8} LDO Electrical Characteristics

Unless otherwise noted, V_{IN} = V_{BATT} = 3.6V. Typical values and limits appearing in normal type apply for T_J = 25°C. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, −40 to +125°C. (1) (2) (3)

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OUT} Accuracy	Output Voltage	1 mA ≤ I_{OUT} ≤ 150 mA, V_{OUT} = 2.7V 3.0V ≤ V_{BATT} = V_{IN} ≤ 5.5V	**−3**	±1.0	**+3**	%
V_{OUT} Range	Programmable Output Voltage Range	0 µA ≤ I_{OUT} ≤ 150 mA Programming Resolution = 100 mV	**2.5**	3.0	**3.2**	V
I_{OUT}	Output Current	$(V_{OUT}$ + 0.25V, 3.0V$)_{MAX}$ ≤ V_{BATT} V_{BATT} = V_{IN} ≤ 5.5V			**150**	mA
	Output Current Limit	V_{OUT} = 0V		510		
V_{IN}–V_{OUT}	Dropout Voltage	I_{OUT} = 75 mA		30	**173**	mV
ΔV_{OUT}	Line Regulation	$(V_{OUT}$ + 0.25V, 3.0V$)_{MAX}$ ≤ V_{BATT} V_{BATT} = V_{IN} ≤ 5.5V, I_{OUT} = 75 mA		3		mV
	Load Regulation	V_{IN} = 3.6V, 1 mA ≤ I_{OUT} ≤ 150 mA		12	**41**	
e_N	Output Noise Voltage	10 Hz ≤ f ≤ 100 kHz, C_{OUT} = 2.2 µF		27		μV_{RMS}
PSRR	Power Supply Ripple Rejection Ratio	f = 217 Hz, C_{OUT} = 2.2 µF		57		dB
I_{GND}	Ground Current	I_{OUT} = 100 µA		30		µA
C_{OUT}	Output Capacitance	0 µA ≤ I_{OUT} ≤ 150 mA	**2**		**20**	µF
	Output Capacitor ESR		**5**		**500**	mΩ
$t_{START-UP}$	Start-Up Time from Shutdown	C_{OUT} = 2.2 µF, I_{OUT} = 150 mA (4)		60		µs

(1) All voltages are with respect to the potential at the GND pin.
(2) All limits are guaranteed by design, test and/or statistical analysis. All electrical characteristics having room-temperature limits are tested during production with T_J = 25°C. All hot and cold limits are guaranteed by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(3) Capacitors: Low-ESR Surface-Mount Ceramic Capacitors are (MLCCs) used in setting electrical characteristics.
(4) Guaranteed by design.

V_{O9} LDO Electrical Characteristics

Unless otherwise noted, $V_{IN} = V_{BATT} = 3.6V$. Typical values and limits appearing in normal type apply for $T_J = 25°C$. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, −40 to +125°C. [1] [2] [3]

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OUT} Accuracy	Output Voltage	1 mA ≤ I_{OUT} ≤ 200 mA, V_{OUT} = 2.2V 3.0V ≤ $V_{BATT} = V_{IN}$ ≤ 5.5V	**−3**	±1.0	**+3**	%
V_{OUT} Range	Programmable Output Voltage Range	0 µA ≤ I_{OUT} ≤ 200 mA Programming Resolution = 100 mV	**1.5**	3.0	**3.0**	V
I_{OUT}	Output Current	$(V_{OUT} + 0.25V, 3.0V)_{MAX} \le V_{BATT}$ $V_{BATT} = V_{IN}$ ≤ 5.5V			**200**	mA
	Output Current Limit	V_{OUT} = 0V		770		
V_{IN}–V_{OUT}	Dropout Voltage	I_{OUT} = 100 mA		50	**288**	mV
ΔV_{OUT}	Line Regulation	$(V_{OUT} + 0.25V, 3.0V)_{MAX} \le V_{BATT}$ $V_{BATT} = V_{IN}$ ≤ 5.5V, I_{OUT} = 100 mA		3		mV
	Load Regulation	V_{IN} = 3.6V, 1 mA ≤ I_{OUT} ≤ 200 mA		15	**44**	
e_N	Output Noise Voltage	10 Hz ≤ f ≤ 100 kHz, C_{OUT} = 4.7 µF		27		μV_{RMS}
PSRR	Power Supply Ripple Rejection Ratio	f = 217 Hz, C_{OUT} = 4.7 µF		60		dB
I_{GND}	Ground Current	I_{OUT} = 100 µA		30		µA
C_{OUT}	Output Capacitance	1 µA ≤ I_{OUT} ≤ 200 mA	**2**		**20**	µF
	Output Capacitor ESR		**5**		**500**	mΩ
$t_{START-UP}$	Start-Up Time from Shutdown	C_{OUT} = 4.7 µF, I_{OUT} = 200 mA [4]		60		µs

(1) All voltages are with respect to the potential at the GND pin.
(2) All limits are guaranteed by design, test and/or statistical analysis. All electrical characteristics having room-temperature limits are tested during production with $T_J = 25°C$. All hot and cold limits are guaranteed by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(3) Capacitors: Low-ESR Surface-Mount Ceramic Capacitors are (MLCCs) used in setting electrical characteristics.
(4) Guaranteed by design.

V_{O10} LDO Electrical Characteristics

Unless otherwise noted, $V_{IN} = V_{BATT}$ = 3.6V. Typical values and limits appearing in normal type apply for T_J = 25°C. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, −40 to +125°C. (1) (2) (3)

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OUT} Accuracy	Output Voltage	1 mA ≤ I_{OUT} ≤ 150 mA, V_{OUT} = 2.2V 3.0V ≤ $V_{BATT} = V_{IN}$ ≤ 5.5V	**−3**	±1.0	**+3**	%
V_{OUT} Range	Programmable Output Voltage Range	0 µA ≤ I_{OUT} ≤ 150 mA Programming Resolution = 100 mV	**1.5**	2.5	**3.0**	V
I_{OUT}	Output Current	$(V_{OUT} + 0.25V, 3.0V)_{MAX} \le V_{BATT}$ $V_{BATT} = V_{IN}$ ≤ 5.5V			**150**	mA
	Output Current Limit	V_{OUT} = 0V		610		
V_{IN}–V_{OUT}	Dropout Voltage	I_{OUT} = 75 mA		30	**204**	mV
ΔV_{OUT}	Line Regulation	$(V_{OUT} + 0.25V, 3.0V)_{MAX} \le V_{BATT}$ $V_{BATT} = V_{IN}$ ≤ 5.5V, I_{OUT} = 75 mA		3		mV
	Load Regulation	V_{IN} = 3.6V, 1 mA ≤ I_{OUT} ≤ 150 mA		12	**41**	
e_N	Output Noise Voltage	10 Hz ≤ f ≤ 100 kHz, C_{OUT} = 2.2 µF		27		μV_{RMS}
PSRR	Power Supply Ripple Rejection Ratio	f = 217 Hz, C_{OUT} = 2.2 µF		57		dB
I_{GND}	Ground Current	I_{OUT} = 100 µA		30		µA
C_{OUT}	Output Capacitance	0 µA ≤ I_{OUT} ≤ 150 mA	**2**		**20**	µF
	Output Capacitor ESR		**5**		**500**	mΩ
$t_{START-UP}$	Start-Up Time from Shutdown	C_{OUT} = 2.2 µF, I_{OUT} = 150 mA (4)		60		µs

(1) All voltages are with respect to the potential at the GND pin.
(2) All limits are guaranteed by design, test and/or statistical analysis. All electrical characteristics having room-temperature limits are tested during production with T_J = 25°C. All hot and cold limits are guaranteed by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(3) Capacitors: Low-ESR Surface-Mount Ceramic Capacitors are (MLCCs) used in setting electrical characteristics.
(4) Guaranteed by design.

V_{O11} LDO Electrical Characteristics

Unless otherwise noted, V_{IN} = V_{BATT} = 3.6V. Typical values and limits appearing in normal type apply for T_J = 25°C. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, −40 to +125°C. (1) (2) (3)

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OUT} Accuracy	Output Voltage	1 mA ≤ I_{OUT} ≤ 200 mA, V_{OUT} = 2.7V 3.0V ≤ V_{BATT} = V_{IN} ≤ 5.5V	**−2**	±2.0	**+5**	%
V_{OUT} Range	Programmable Output Voltage Range	0 µA ≤ I_{OUT} ≤ 200 mA Programming Resolution = 100 mV	**1.8**	1.8	**3.3**	V
I_{OUT}	Output Current	(V_{OUT} + 0.25V, 3.0V)$_{MAX}$ ≤ V_{BATT} V_{BATT} = V_{IN} ≤ 5.5V			**200**	mA
	Output Current Limit	V_{OUT} = 0V		900		
V_{IN}–V_{OUT}	Dropout Voltage	I_{OUT} = 100 mA		50	**302**	mV
ΔV_{OUT}	Line Regulation	(V_{OUT} + 0.25V, 3.0V)$_{MAX}$ ≤ V_{BATT} V_{BATT} = V_{IN} ≤ 5.5V, I_{OUT} = 100 mA		3		mV
	Load Regulation	V_{IN} = 3.6V, 1 mA ≤ I_{OUT} ≤ 200 mA		15	**44**	
e_N	Output Noise Voltage	10 Hz ≤ f ≤ 100 kHz, C_{OUT} = 4.7 µF		27		µV_{RMS}
PSRR	Power Supply Ripple Rejection Ratio	f = 217 Hz, C_{OUT} = 4.7 µF		60		dB
I_{GND}	Ground Current	I_{OUT} = 100 µA		30		µA
C_{OUT}	Output Capacitance	1 mA ≤ I_{OUT} ≤ 200 mA	**2**		**20**	µF
	Output Capacitor ESR		**5**		**500**	mΩ
$t_{START-UP}$	Start-Up Time from Shutdown	C_{OUT} = 4.7 µF, I_{OUT} = 200 mA (3)		60		µs

(1) All voltages are with respect to the potential at the GND pin.
(2) All limits are guaranteed by design, test and/or statistical analysis. All electrical characteristics having room-temperature limits are tested during production with T_J = 25°C. All hot and cold limits are guaranteed by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(3) Guaranteed by design.

V_{RTC} LDO Electrical Characteristics

Unless otherwise noted, 2.5V < V_{BU_BAT} < 3.3V. Typical values and limits appearing in normal type apply for T_J = 25°C. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, −40 to +125°C. [1] [2] [3]

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OUT} Accuracy	Output Voltage	I_{OUT} ≤ 50 µA, V_{OUT} = 1.8V 2.15V ≤ V_{BU-BAT} ≤ 3.3V	**1.6**	1.8	**2.0**	V
I_Q	Quiescent Current	I_{OUT} = 6 µA		2.6	**6**	µA
I_{OUT}	Output Current	2.15V ≤ V_{BU-BAT} ≤ 3.3V		10	**50**	µA
	Output Current Limit	V_{OUT} = 0V	**1000**	2000	**10000**	
V_{IN}–V_{RTC}	Dropout Voltage	I_{OUT} = 50 mA		150	**190**	mV
PSRR	Power Supply Ripple Rejection Ratio	f = 100 Hz, C_{OUT} = 1.0 µF		20		dB
C_{OUT}	Output Capacitance	1 mA ≤ I_{OUT} ≤ 200 mA	**0.75**	1.0	**2.2**	µF
	Output Capacitor ESR		**5**		**500**	mΩ

(1) All voltages are with respect to the potential at the GND pin.
(2) All limits are guaranteed by design, test and/or statistical analysis. All electrical characteristics having room-temperature limits are tested during production with T_J = 25°C. All hot and cold limits are guaranteed by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(3) Capacitors: Low-ESR Surface-Mount Ceramic Capacitors are (MLCCs) used in setting electrical characteristics.

Back-Up Charger Electrical Characteristics

Unless otherwise noted, V_{IN} = V_{BATT} = 3.6V. Typical values and limits appearing in normal type apply for T_J = 25°C. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, −40 to +125°C. [(1)] [(2)] [(3)]

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IN}	Operational Voltage Range			V_{OUT} + 0.4	**5.5**	V
V_{OUT} Accuracy	Output Voltage	I_{OUT} ≤ 50 µA, V_{OUT} = 3.15V V_{OUT} + 0.4 ≤ V_{BATT} ≤ 5.5V	**3.0**	3.15	**3.3**	V
I_Q	Quiescent Current	I_{OUT} < 50 µA		25		µA
I_{OUT}	Output Current	V_{OUT} + 0.4 ≤ V_{BATT} = V_{IN} ≤ 5.5V, V_{OUT} = 3.0V		70	**150**	µA
	Output Current Limit	3.2V ≤ V_{BATT} = V_{IN} ≤ 5.5V V_{OUT} = 0V	**0.7**	1.5	**2**	mA
PSRR	Power Supply Ripple Rejection Ratio	I_{OUT} ≤ 50 µA, V_{OUT} = 3.15V V_{OUT} + 0.4 ≤ V_{BATT} = V_{IN} ≤ 5.5V f < 10 kHz		15		dB
C_{OUT}	Output Capacitance	0 µA ≤ I_{OUT} ≤ 100 µA		0.1		µF
	Output Capacitor ESR		**5**		**500**	mΩ

(1) All voltages are with respect to the potential at the GND pin.
(2) All limits are guaranteed by design, test and/or statistical analysis. All electrical characteristics having room-temperature limits are tested during production with T_J = 25°C. All hot and cold limits are guaranteed by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(3) Capacitors: Low-ESR Surface-Mount Ceramic Capacitors are (MLCCs) used in setting electrical characteristics.

Comparators' Electrical Characteristics

Unless otherwise noted, V_{BATT} = +2.5V to 5.5V, V_{O3} = 3.0V, V_{CM} = 0.27V. Typical values and limits appearing in normal type apply for T_J = 25°C. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, −40 to +125°C. (1) (2) (3)

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_T	Comparator Trip Voltage		**230**	270	**300**	mV
I_B	Input Bias Current	V_{INV} = 1.3V		0.01	**0.15**	µA
I_{OS}	Input Offset Current			1		nA
PSRR	Power Supply Rejection Ratio	2.7V ≤ V_{BATT} ≤ 5.5V		50		dB
V_{OL}	Output Voltage Low	I_{SINK} = 1 mA		0.24	**0.37**	V
V_{OH}	Output Voltage High	I_{SOURCE} = 1 mA	**2.57**	V_{O3}–0.25	**3**	V
t_{PLH}	Propagation Delay Low to High	Overdrive = 100 mV (4)		5		µs
t_{PHL}	Propagation Delay High to Low	Overdrive = 100 mV (4)		5		µs
t_{LH}	Rise Time Low to High	Overdrive = 100 mV C_{OUT} = 10 pF (4)		5		ns
t_{HL}	Fall Time High to Low	Overdrive = 100 mV C_{OUT} = 10 pF (4)		5		ns
I_Q	Quiescent Current per Comparator			5		µA

(1) All voltages are with respect to the potential at the GND pin.
(2) All limits are guaranteed by design, test and/or statistical analysis. All electrical characteristics having room-temperature limits are tested during production with T_J = 25°C. All hot and cold limits are guaranteed by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(3) Capacitors: Low-ESR Surface-Mount Ceramic Capacitors are (MLCCs) used in setting electrical characteristics.
(4) Guaranteed by design.

$\overline{\text{RESET}}$ Electrical Characteristics

Unless otherwise noted, V_{BATT} = +2.5V to 5.5V. Typical values and limits appearing in normal type apply for T_J = 25°C. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, −40 to +125°C. (1) (2) (3)

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OH}	Output Voltage High	Internal Logic Supply I_{SOURCE} = 0 µA	**V_{O3}–0.2**			V
V_{OL}	Output Voltage Low	Internal Logic Supply I_{SINK} = 500 µA			**0.4**	V
V_{TSHLD}	V_{O1} Threshold	V_{O1} Rising	**90**	93	**96**	%
		V_{O1} Falling	**82**	85	**88**	%
t_{DELAY}	$\overline{\text{RESET}}$ Active Time-Out Period	From V_{O1} ≥ 93% until $\overline{\text{RESET}}$ = High	**34**	40	**47**	ms
$t_{PS\text{-}HOLD}$	PS-HOLD Timer	From $\overline{\text{RESET}}$ = Hi to PS-HOLD = Hi From PS-HOLD = Low to $\overline{\text{RESET}}$ = Low	**29**	35	**41**	ms
t_{RESET}	Shut-Down Timer	From $\overline{\text{RESET}}$ = Low until LDOs turned off (no output regulation)	**51**	60	**70**	ms
R_{PU}	Pull-up Resistance to V_{O1}			14		kΩ
$I_{S\text{-}MAX}$	Maximum Sink Current				**5**	mA

(1) All voltages are with respect to the potential at the GND pin.
(2) All limits are guaranteed by design, test and/or statistical analysis. All electrical characteristics having room-temperature limits are tested during production with T_J = 25°C. All hot and cold limits are guaranteed by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(3) Capacitors: Low-ESR Surface-Mount Ceramic Capacitors are (MLCCs) used in setting electrical characteristics.

LED Driver Electrical Characteristics

Unless otherwise noted, V_{BATT} = +2.5V to 5.5V. Typical values and limits appearing in normal type apply for T_J = 25°C. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, −40 to +125°C. (1) (2) (3)

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OL}	LED1–3 Output Low Level	I_{SINK} = 40 mA		0.17	**0.55**	V
$I_{LEAKAGE}$	LED1–3 Off Leakage Current	V_{DR} = 5.5V		4		µA

(1) All voltages are with respect to the potential at the GND pin.
(2) All limits are guaranteed by design, test and/or statistical analysis. All electrical characteristics having room-temperature limits are tested during production with T_J = 25°C. All hot and cold limits are guaranteed by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(3) Capacitors: Low-ESR Surface-Mount Ceramic Capacitors are (MLCCs) used in setting electrical characteristics.

Main Battery Charger Electrical Characteristics

Unless otherwise noted, V_{CHG-IN} = 5V, V_{BATT} = 4V. Typical values and limits appearing in normal type apply for T_J = 25°C. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, −40 to +125°C. (1) (2) (3) (4)

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{CHG-IN}	Input Voltage Range		**4.5**		**12**	V
	Operating Range	Battery Connected	**4.5**		**6**	
V_{OK_TSHD}	Adapter OK Trip Point (CHG-IN)	V_{CHG-IN}–V_{BATT} Rising		80		mV
		V_{CHG-IN}–V_{BATT} Falling		30		mV
V_{UVLO_TSHD}	Under Voltage Lock-Out Trip Point	V_{CHG-IN} Rising	**3.85**	4.25	**4.65**	V
		V_{CHG-IN} Falling		3.90		V
V_{OVLO_TSHD}	Over Voltage Lock-Out Trip Point	V_{CHG-IN} Rising	**5.46**	6.00	**6.54**	V
		V_{CHG-IN} Falling		5.80		V
$I_{BATTSENSE}$	Leakage Current	V_{BATT} = 4.2V		8		µA
I_{BATT}	Battery Input Current	V_{CHG-IN} ≤ 4V		2		µA
		Charging Complete, charger connected, V_{BATT} = 4.1V			**150**	µA
I_{CHG}	Fast Charge Current Accuracy	I_{CHG} = 700 mA	−10	±5	+10	%
	Fast Charge Current Range		478		937	mA
	Programmable Charging Current Step			43		mA
I_{PRE_CHG}	Pre-Charge Current	V_{BATT} = 2V	**28**	42	**59**	mA
R_{SENSE}	Internal Current Sense Resistance			120		mΩ
	Internal Current Sense Resistor Load Current				**1.2**	A
CHARGING PERFORMANCE						
V_{BATT}	Battery Regulation Voltage (CV Mode, for 4.1V Cell)	T_A −40°C to +85°C	**4.015**	4.1	**4.19**	
	Battery Regulation Voltage CV mode, for 4.2V Cell)	T_A −40°C to +85°C	**4.115**	4.2	**4.289**	
V_{CHG-Q}	Full Charge Qualification Threshold	V_{BATT} Rising, Transition from Pre-Charge to Full Current	**2.8**	3.0	**3.2**	V
$V_{BAT-RST}$	Restart Threshold Voltage (For 4.1V Cell)	V_{BATT} Falling, Transition from EOC, to Pre-Qual State		3.9		V
	Restart Threshold Voltage (For 4.2 Cell)	V_{BATT} Falling, Transition from EOC, to Pre-Qual State		4.0		
t_{EOC}	Time to EOC State	−40°C to +85°C (5)	**4.80**	5.625	**6.55**	Hrs
A/D CONVERTER PERFORMANCE						
	Resolution			8		Bits
INL	Relative Accuracy		**−1**		**+1**	LSB
DNL	Differential Nonlinearity	No Missing Code	**−1**		**+1**	LSB

(1) All voltages are with respect to the potential at the GND pin.
(2) Capacitors: Low-ESR Surface-Mount Ceramic Capacitors are (MLCCs) used in setting electrical characteristics.
(3) All limits are guaranteed by design, test and/or statistical analysis. All electrical characteristics having room-temperature limits are tested during production with T_J = 25°C. All hot and cold limits are guaranteed by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(4) LP3941A is not intended as a Li-Ion battery protection device. Battery used in this application should have an adequate internal protection.
(5) Guaranteed by design.

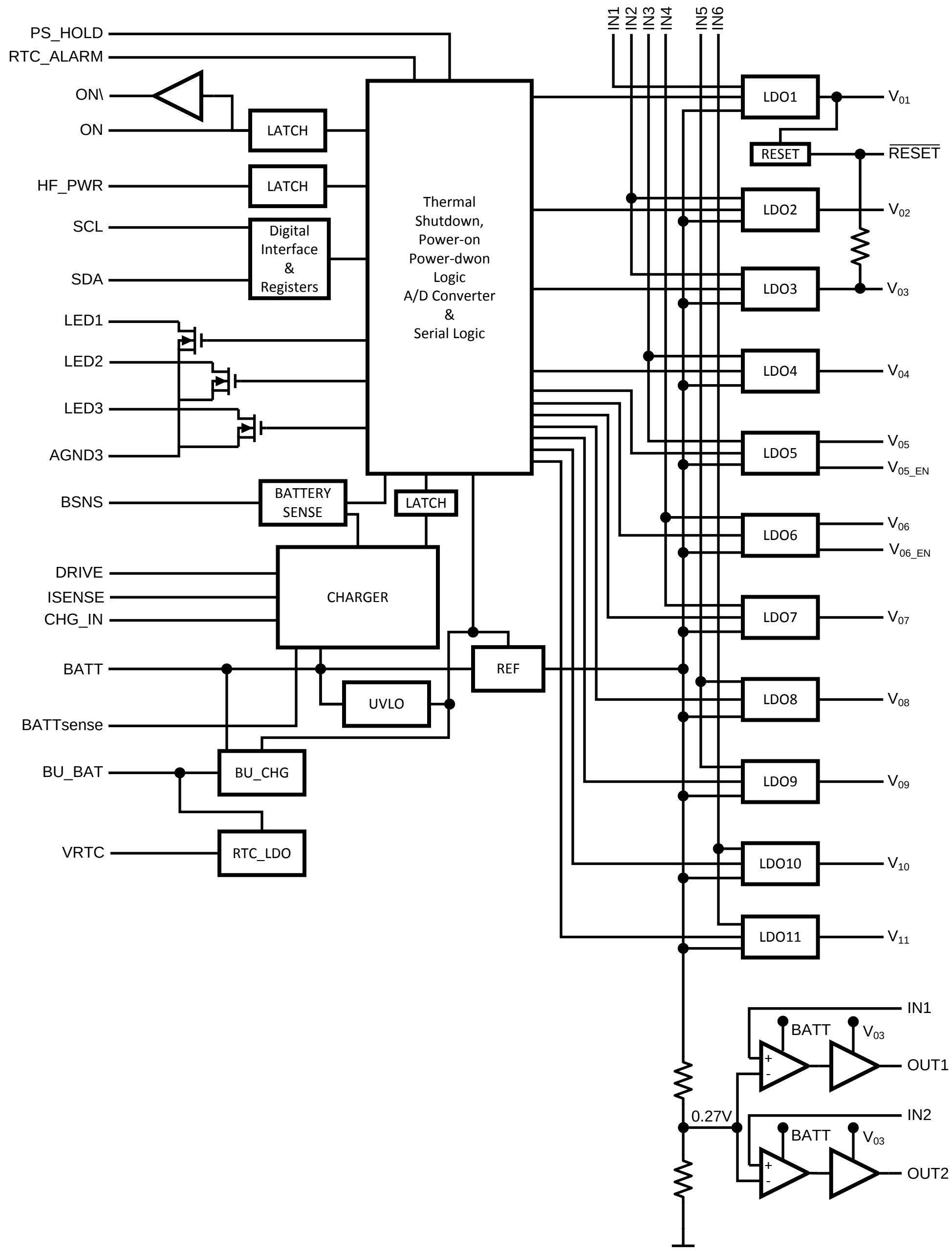
I²C Compatible Interface Electrical Characteristics

Unless otherwise noted, V_{BATT} = +2.5V to 5.5V. Typical values and limits appearing in normal type apply for T_J = 25°C. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, −40 to +125°C. (1) (2) (3)

Symbol	Parameter	Condition	Min	Typ	Max	Units
F_{CLK}	Clock Frequency				**400**	kHz
t_{BF}	Bus-Free Time between START and STOP	(4)	**1.3**			µs
t_{HOLD}	Hold Time Repeated START Condition	(4)	**0.6**			µs
t_{CLK-LP}	CLK Low Period	(4)	**1.3**			µs
t_{CLK-HP}	CLK High Period	(4)	**0.6**			µs
t_{SU}	Set-Up Time Repeated START Condition	(4)	**0.6**			µs
$t_{DATA-HOLD}$	Data Hold Time	(4)	**0**			µs
$t_{DATA-SU}$	Data Set-Up Time	(4)	**100**			ns
t_{SU}	Set-Up Time for STOP Condition	(4)	**0.6**			µs
t_{TRANS}	Maximum Pulse Width of Spikes that must be suppressed by the input filter of both DATA & CLK signals.	(4)		50		ns

(1) All voltages are with respect to the potential at the GND pin.
(2) All limits are guaranteed by design, test and/or statistical analysis. All electrical characteristics having room-temperature limits are tested during production with T_J = 25°C. All hot and cold limits are guaranteed by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(3) Capacitors: Low-ESR Surface-Mount Ceramic Capacitors are (MLCCs) used in setting electrical characteristics.
(4) Guaranteed by design.

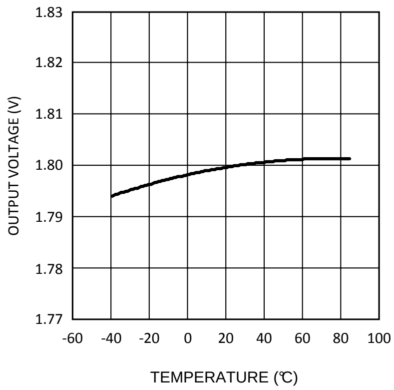
LP3941A Simplified Block Diagram



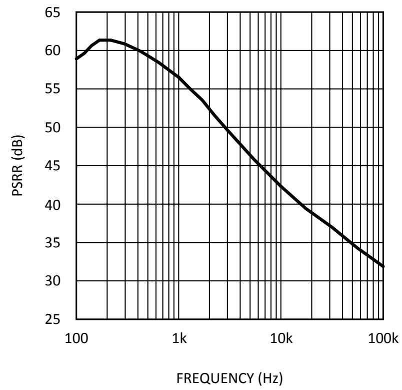
Typical Performance Characteristics

Under nominal conditions. This means, unless otherwise noted, T_A = 25°C, V_{BATT} = 3.6V, V_{BU_BATT} = 3.15V.

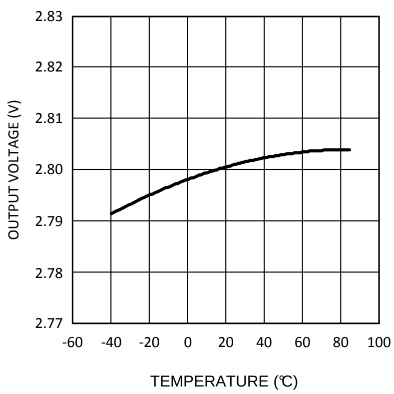
200 mA LDO Output Voltage



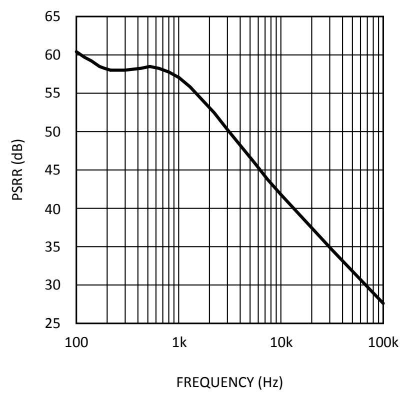
200 mA LDO PSRR



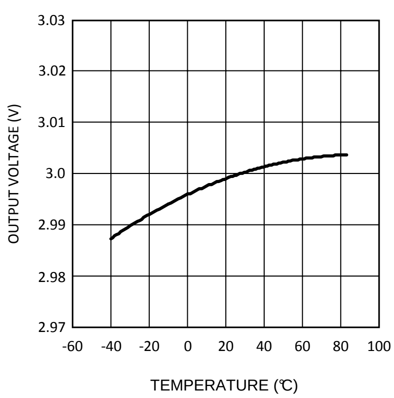
150 mA LDO Output Voltage



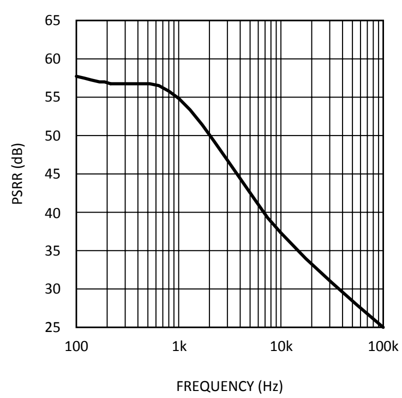
150 mA LDO PSRR



50 mA LDO Output Voltage



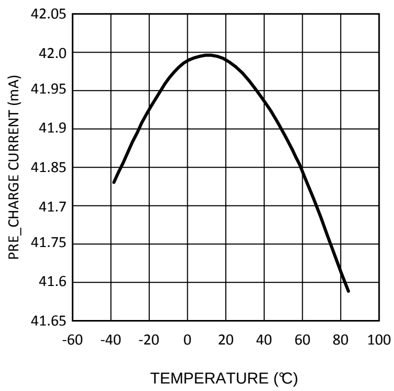
50 mA LDO PSRR



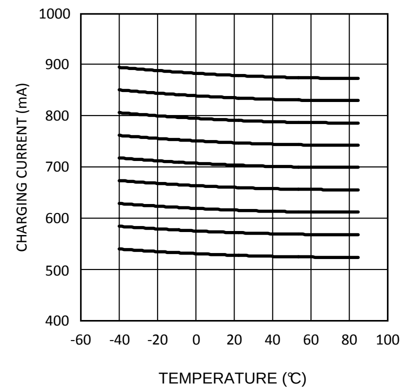
Typical Performance Characteristics (continued)

Under nominal conditions. This means, unless otherwise noted, T_A = 25°C, V_{BATT} = 3.6V, V_{BU_BATT} = 3.15V.

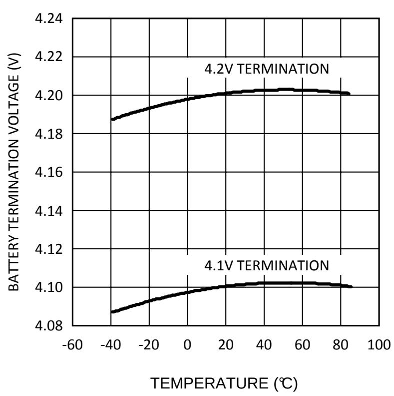
Pre-Charge Current



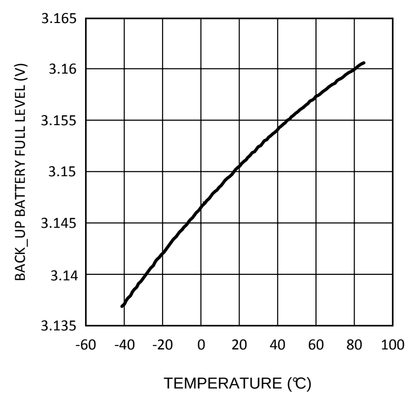
Fast Charging Current



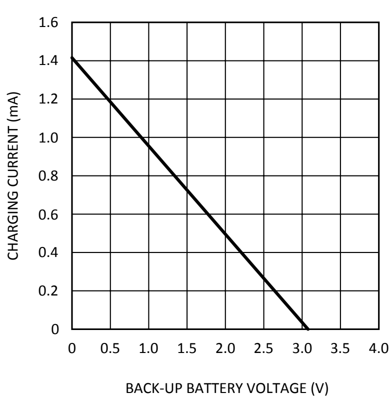
Charging Termination Voltage



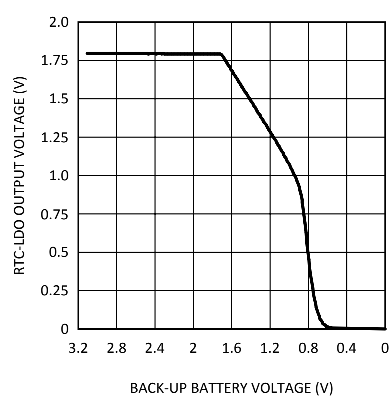
Back-Up Battery Full Voltage



Back-Up Battery Charging Current



RTC-LDO Output Voltage



LP3941A Serial Port Communication Address Code 7h'7E

Numbers in parentheses indicate default setting: (0) bit is set to low state, and (1) bit is set to high state. R/O –Read Only, All other bits are Read and Write.

Table 4. LP3941 Control and Data Codes

Addr	Register	7	6	5	4	3	2	1	0
8h'00	Enable	LDO7–EN (0)	LDO6–EN (0)	LDO5–EN (1)	LDO4–EN (0)	LDO3–EN (1)	LDO2–EN (0)	LDO1–EN (1)	LDO8–EN (0)
8h'01	LDO9/ LDO1 Data Code	LDO9 Code 3 (1)	LDO9 Code 2 (1)	LDO9 Code 1 (1)	LDO9 Code 0 (1)	LDO1 Code 3 (0)	LDO1 Code 2 (0)	LDO1 Code 1 (1)	LDO1 Code 0 (1)
8h'02	LDO10/ LDO2 Data Code	LDO10 Code 3 (1)	LDO10 Code 2 (0)	LDO10 Code 1 (1)	LDO10 Code 0 (0)	LDO2 Code 3 (1)	LDO2 Code 2 (1)	LDO2 Code 1 (0)	LDO2 Code 0 (1)
8h'03	LDO8/ LDO3 Data Code	Not Used (0)	LDO8 Code 2 (1)	LDO8 Code 1 (0)	LDO8 Code 0 (1)	Not Used (0)	LDO3 Code 2 (1)	LDO3 Code 1 (0)	LDO3 Code 0 (1)
8h'04	LDO11/ LDO4 Data Code	LDO11 Code 3 (0)	LDO11 Code 2 (0)	LDO11 Code 1 (0)	LDO11 Code 0 (0)	LDO4 Code 3 (1)	LDO4 Code 2 (1)	LDO4 Code 1 (1)	LDO4 Code 0 (1)
8h'05	LDO5 Data Code	Not Used (0)	Not Used (0)	Not Used (0)	Not Used (0)	Not Used (0)	LDO5 Code 2 (0)	LDO5 Code 1 (1)	LDO5 Code 0 (1)
8h'06	LDO6 Data Code	Not Used (0)	Not Used (0)	Not Used (0)	Not Used (0)	Not Used (0)	LDO6 Code 2 (0)	LDO6 Code 1 (1)	LDO6 Code 0 (1)
8h'07	LDO7 Data Code	Not Used (0)	Not Used (0)	Not Used (0)	Not Used (0)	Not Used (0)	LDO7 Code 2 (1)	LDO7 Code 1 (0)	LDO7 Code 0 (1)
8h'08	Charger Register –1	Not Used (0)	Not Used (0)	Not Used (0)	4.1V/4.2V (1)	Charger Current Code 3 (0)	Charger Current Code 2 (0)	Charger Current Code 1 (0)	Charger Current Code 0 (1)
8h'09	Charger Register –2	Not Used (0)	Not Used (0)	Not Used (0)	EOC R/O	Charging R/O	EOC Sel-1 (0)	EOC Sel-0 (1)	Charger-DIS Off/On (0)
8h'0a	Control/ Enable	LDO9-EN (0)	LDO10-EN (0)	LDO11-EN (0)	Back-Up Battery Charger Enable (1)	RTC_LDO Disable (0)	LED1 Enable (0)	LED2 Enable (0)	LED3 Enable (0)
8h'0b	ADC Control Register	Not Used (0)	Not Used (0)	Not Used (0)	Not Used (0)	ADC Start (0)	ADC EN (0)	ADC Mux-1 (1)	ADC Mux-0 (1)
8h'0c	ADC Output Register	ADC7 R/O	ADC6 R/O	ADC5 R/O	ADC4 R/O	ADC3 R/O	ADC2 R/O	ADC1 R/O	ADC0 R/O
8h'0d	Power-On-Reason Register	R/O (0)	R/O (0)	R/O (0)	R/O (0)	ON R/O	RTC ALARM R/O	CHG_IN R/O	HF_PWR R/O
8h'2e	ADC/ Status Register	COMP2 OUT R/O	COMP1 OUT R/O	ON R/O	RTC Alarm R/O	Charger Present R/O	HF_PWR R/O	ADC Overflow R/O	ADC Data Ready R/O

Regulator Output Voltage Programming

The following table summarizes the supported output voltages for LP3941A. Default voltages after start-up sequence have been highlighted in **bold**.

Data Code	V_{O1} (V)	V_{O2} (V)	V_{O3} (V)	V_{O4} (V)	V_{O5} (V)	V_{O6} (V)	V_{O7} (V)	V_{O8} (V)	V_{O9} (V)	V_{O10} (V)	V_{O11} (V)
4h'00	1.5	1.5	2.5	1.5	2.5	2.5	2.5	2.5	1.5	1.5	**1.8**
4h'01	1.6	1.6	2.6	1.6	2.6	2.6	2.6	2.6	1.6	1.6	1.9
4h'02	1.7	1.7	2.7	1.7	2.7	2.7	2.7	2.7	1.7	1.7	2.0

Data Code	V_{O1} (V)	V_{O2} (V)	V_{O3} (V)	V_{O4} (V)	V_{O5} (V)	V_{O6} (V)	V_{O7} (V)	V_{O8} (V)	V_{O9} (V)	V_{O10} (V)	V_{O11} (V)
4h'03	**1.8**	1.8	2.8	1.8	**2.8**	**2.8**	2.8	2.8	1.8	1.8	2.1
4h'04	1.9	1.9	2.9	1.9	2.9	2.9	2.9	2.9	1.9	1.9	2.2
4h'05	2.0	2.0	**3.0**	2.0	3.0	3.0	**3.0**	**3.0**	2.0	2.0	2.3
4h'06	2.1	2.1	3.1	2.1	3.1	3.1	3.1	3.1	2.1	2.1	2.4
4h'07	2.2	2.2	3.2	2.2	3.2	3.2	3.2	3.2	2.2	2.2	2.5
4h'08	2.3	2.3		2.3					2.3	2.3	2.6
4h'09	2.4	2.4		2.4					2.4	2.4	2.7
4h'0a	2.5	2.5		2.5					2.5	**2.5**	2.8
4h'0b	2.6	2.6		2.6					2.6	2.6	2.9
4h'0c	2.7	2.7		2.7					2.7	2.7	3.0
4h'0d	2.8	**2.8**		2.8					2.8	2.8	3.1
4h'0e	2.9	2.9		2.9					2.9	2.9	3.2
4h'0f	3.0	3.0		**3.0**					**3.0**	3.0	3.3

Register Programming Examples

Example 1. Setting register h'00 value to 8h'ff' will enable LDOs 1–8.

Example 2. Setting register h'01 to 8h'8c' will set LDO9 output to 2.3V and LDO1 output to 2.7V. These voltages will appear at the LDO outputs if the corresponding LDOs have been enabled. Programming a voltage value to a LDO, which is off, will affect the LDO output voltage after the LDO is enabled. Enabling and programming the output voltage are separate operations.

Example 3. Setting register h'09 bit '0' to '1' will disable the main battery charger. Note that all register bits have to be programmed together. It is not possible to program individual bits alone. Writing into read only or unused bit positions does not affect those bits nor does it cause errors. Therefore to disable the main charger and to retain other bits in their default values on would write 8h'03'

ADC and Charger Programming

The following tables show how to select the main battery charger End-Of-Charge current limit, how to set the charger current limit and select a particular input for ADC measurement. Default values have been highlighted in **bold**.

EOC Current Selection Code		
SEL-1	**SEL-0**	**I_{SET} (mA)**
0	1	**0.1C**
1	0	0.15C
1	1	0.2C

A/D Input Selection Code		
MUX-1	**MUX-0**	**Input**
0	0	V_{BATT}
0	1	I_{CHG}
1	0	BATT-ID (20 µA Scale)
1	1	**BATT-ID (200 µA Scale)**

Charger Current Selection Code	
Data Code	**I_{SET} (mA)**
4h'01	**530**
4h'02	574
4h'03	617
4h'04	660

Charger Current Selection Code	
Data Code	**I_{SET} (mA)**
4h'05	703
4h'06	746
4h'07	789
4h'08	832
4h'09	874

The following table is the conversion table for main battery charger current measurement using the on-chip ADC. Temperature dependency is due to the temperature coefficient of the aluminum sense resistor. The ADC itself is temperature compensated as is the charging current in the main battery charger.

A/D Converter's Charge Current Output Code ADC Control Register Code 2h'0X					
Device Temperature −40°C					
I_{CHARGE} (mA)	0	4.97	…	1262	1267
Output Code	h'00	h'01		h'fe	h'ff
Device Temperature +25°C					
I_{CHARGE} (mA)	0	3.95	…	1003	1007
Output Code	h'00	h'01		h'fe	h'ff
Device Temperature +85°C					
I_{CHARGE} (mA)	0	3.27	…	831	834
Output Code	h'00	h'01		h'fe	h'ff

The next table shows the relationship between ADC output code and main battery voltage in ADC Battery Voltage Measurement Mode.

A/D Converter's Battery Voltage Output Code ADC Control Register Code 2h'0X					
Battery Voltage (V)	3.000	3.006	…	4.494	4.500
Output Code	h'00	h'01		h'fe	h'ff

The battery ID resistor value can be determined using the following table in the two ADC Battery ID Modes.

Battery ID Detection Code ADC Control Register Code 2h'0X		
ID Resistor (kΩ)	**Scale 1 (200 µA) Data Code Range**	**Scale 1 (20 µA) Data Code Range**
0.22	h'00–h'12	
0.75	h'13–h'32	
1.8	h'33–h'65	
3.3	h'66–h'a7	
5.1	h'a8–h'ff	
10		h'1e–h'31
15		h'32–h'49
22		h'4a–h'6d
33		h'6e–h'b0
55		h'b1–h'ff

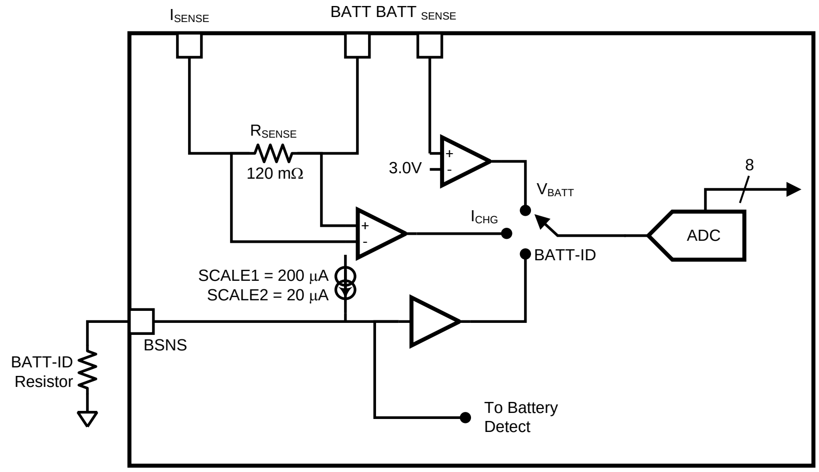
ADC Block Functional Diagram

The ADC block provides four different functions on the LP3941A:

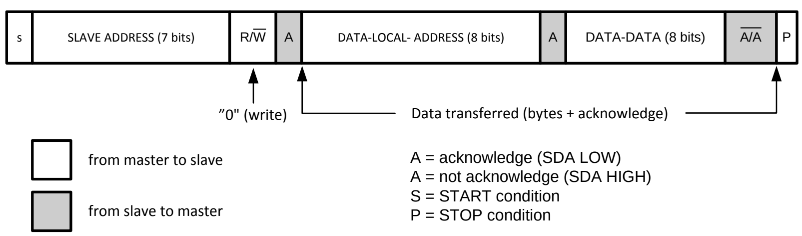
- Main battery voltage measurement
- Main battery charger charging current measurement
- Battery ID resistor resistance measurement with 200 µA sense current

- Battery ID resistor resistance measurement with 20 µA sense current

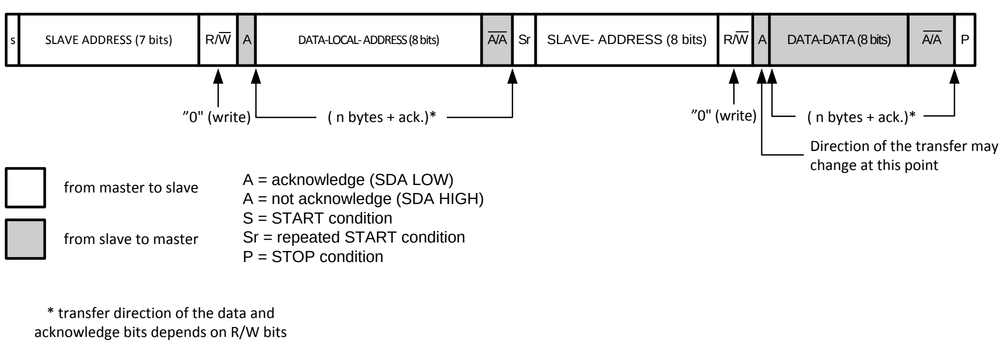
The following picture shows the implementation of these measurements with the ADC.



I²C Read and Write Sequences

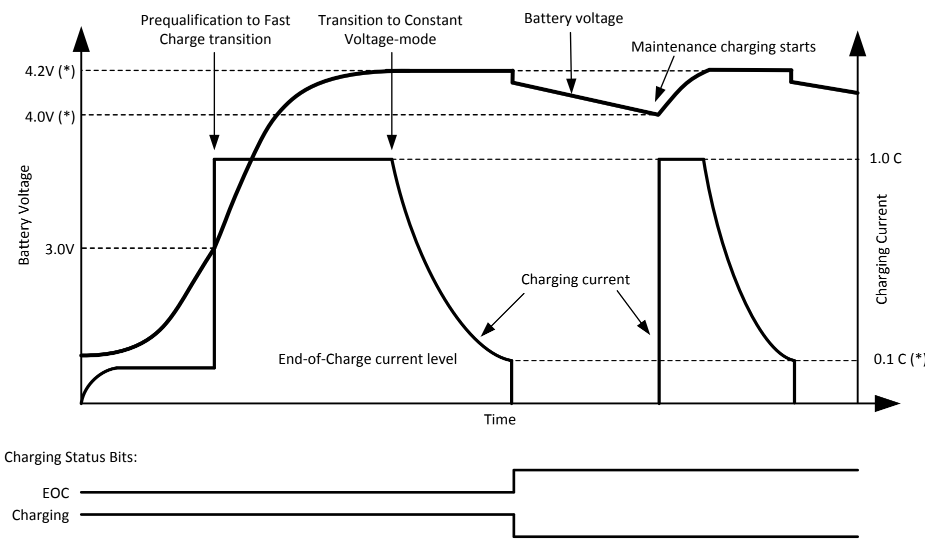


Format to address LP3941A registers



Combined read and write format.

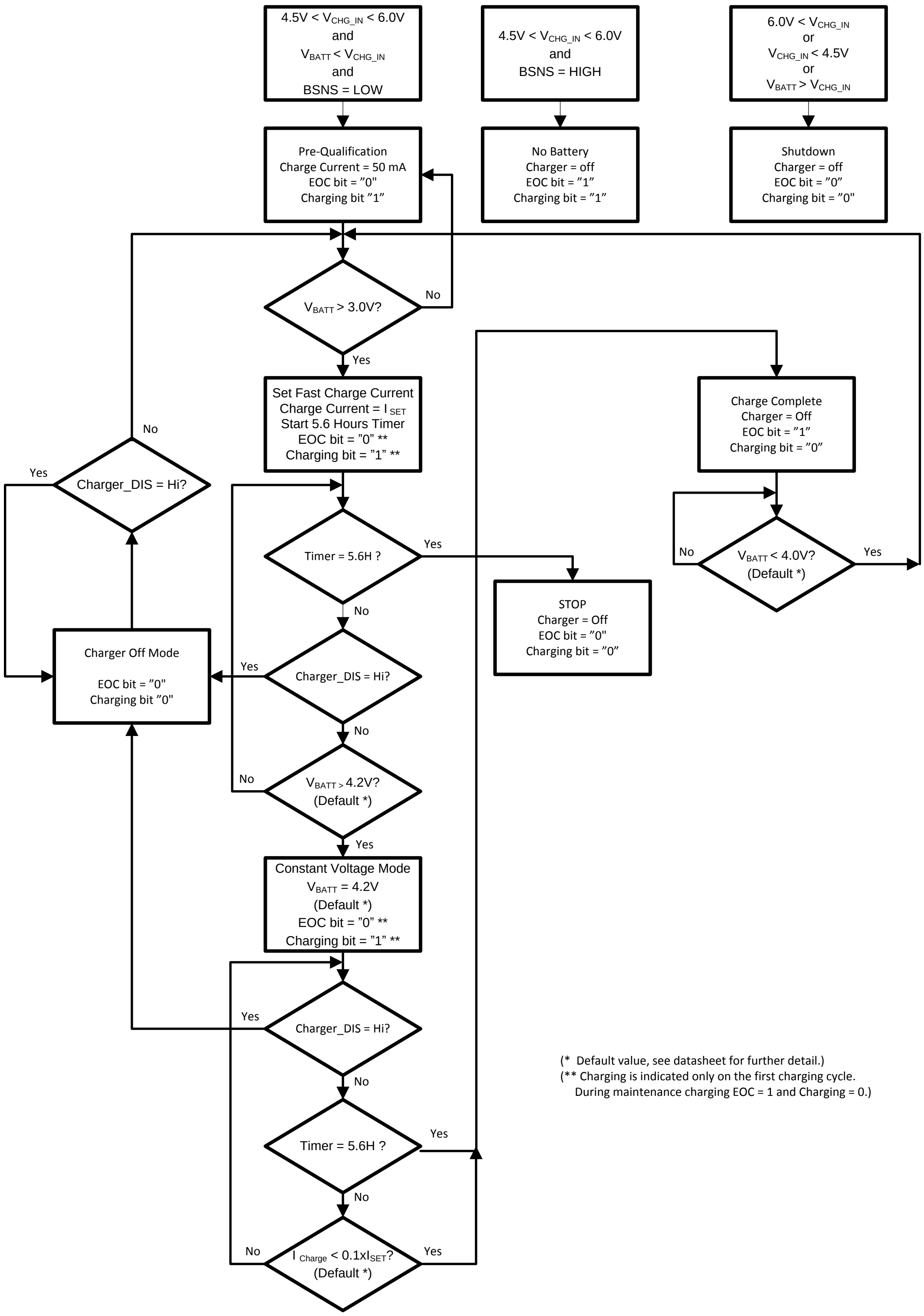
Li-Ion Battery Charger Operation



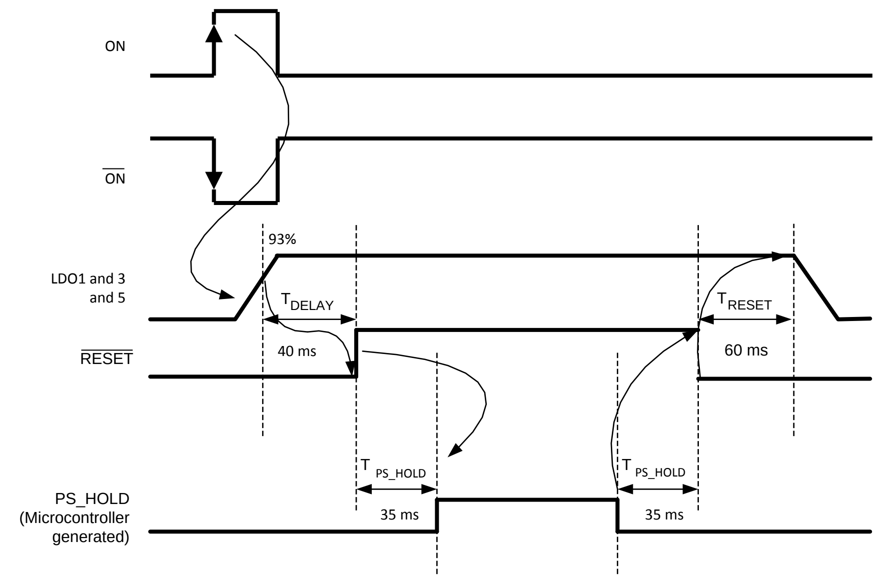
Charging Profile

(*) Battery charging termination voltage level, charging current and End-of-Charging current level are programmable. Battery charging termination voltage can be 4.1V or 4.2V (default). Maintenance charging start limit is 200 mV below the termination voltage level. End-of-Charging current level can be 20%, 15% or 10% (default) of maximum charging current. Picture shows typical situation with default programming. See LP3941A register map for programming details.

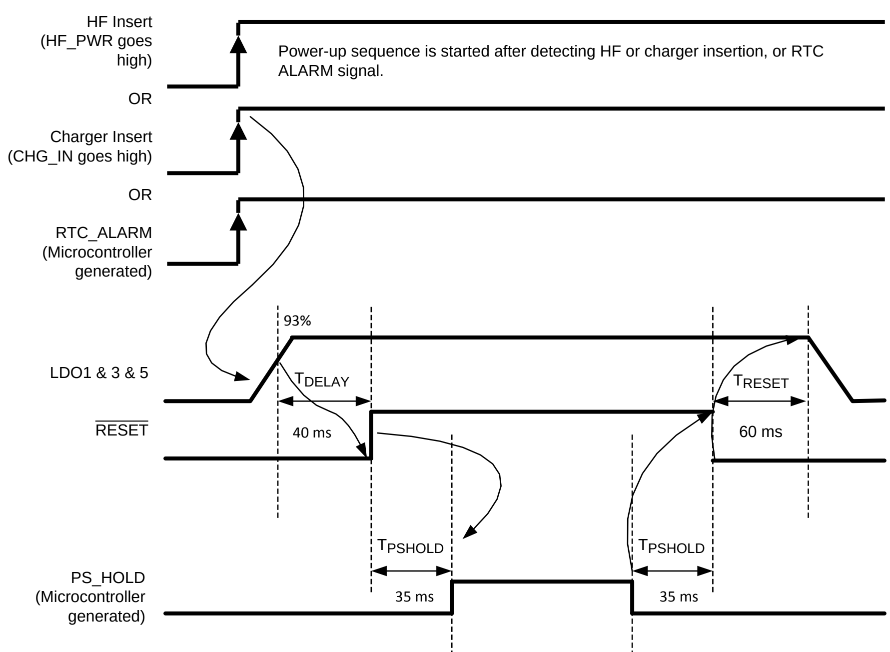
Li-Ion Battery Charger State Diagram



LP3941A Power-Up/Down Sequences



Power-up initiated by the ON-signal.



Power-up initiated by hands free signal, RTC Alarm or charger insertion.

If LDO1 does not reach 93% of nominal output level in 60 ms, LP3941A powers down.

If PS_HOLD does not go high in 35 ms from $\overline{\text{RESET}}$ high, LP3941A powers down.

If UVLO occurs before the rising edge of the PS_HOLD, LP3941A powers down.

If LDO1 output drops below 85% of nominal output level, LP3941A waits for 90 ms for it to recover to 93% (with $\overline{\text{RESET}}$ = ‘0’) before powering down. If LDO1 output reaches 93%, power-up sequence resumes with 40 ms $\overline{\text{RESET}}$ delay.

LP3941A powers down after PS_HOLD has been low for >35 ms continuously. ON-signal, HF_PWR, CHG_IN or RTC ALARM have no control over shutdown operation, but it has to be initiated using PS_HOLD.

Power-Up/Down Reason and Status Register Operation

Register h'0d stores the reason (the activating signal) for powering up the PMU. The possible inputs that can activate the LP3941 are the ON, HF_PWR, RTC ALARM and CHG_IN signals. The signal that activated the LP3941A will have its corresponding bit set to '1'. If multiple signals activate the PMU simultaneously then they are all marked with '1' in register h'0d.

Register h'2e maintains the current status of ON, HF_PWR and RTC_ALARM signals and indicates the presence of an external charger connected to the PMU. This register shows the current status of the inputs whereas h'0d indicates the reason for power-up and remains thereafter static until another power-up sequence occurs.

Register h'2e also indicates the status of the two comparator outputs and the status of the ADC as well.

Note that the bit indicating the presence of an external charger voltage in register h'2e differs provides different information than that in register h'0d. Register h'0d CHG_IN-bit is '1' if CHG_IN-pin was logic high at start-up. Register h'2e Charger Present-bit indicates whether the CHG_IN pin voltage is within acceptable limits (4.5V ≤ V_{CHG_IN} ≤ 6.0V) for charging. If the V_{CHG_IN} is valid for charging then this bit in register h'2e is set to '1'.

Flowchart Operation

The power-up/power-down state machine is reset when VBATT pin is less than 2.1V. The state machine is reset into the POWEROFF state. In this state the UVLO in enabled. All other functions except the RTC_LDO are off.

If an external charger or hands free power is connected, the state machine advances to the EXTERNAL STANDBY state and waits for the battery voltage to reach 3.0V. When the battery voltage reaches 3.0V the state machine advances to the TURNON LDOs state. In the EXTERNAL STANDBY state UVLO is enabled.

If the battery voltage reaches 3.0V before hands free power or a charger is connected the state machine advances to the STANDBY state. The back-up battery charger is enabled. If the ON-key is pressed, a charger is inserted, hands free power is connected or the RTC_ALARM goes high the state machine advances to the TURNON LDOs state.

Once in the TURNON LDOs state LDOs 1, 3 and 5 are enabled. The state machine remains in this state until LDO1 output reaches 93% of its nominal value or 60 ms have passed. If LDO1 reaches 93%, the state machine advances to the RESET OFF DELAY state. If 60 ms have passed before the 93% level is achieved, the state machine returns to the STANDBY state and waits for another wakeup source.

The RESET OFF DELAY state counts off 40 ms. If the battery voltage drops below the UVLO threshold of 2.5V, the state machine goes to the ENABLE RESET state and power down sequence. If LDO1 output drops below 85% of the nominal voltage the state machine returns to the TURNON LDOs state in an attempt to restart the LDO. If neither of these conditions occurs the state machine advances to the PS_HOLD DETECT state.

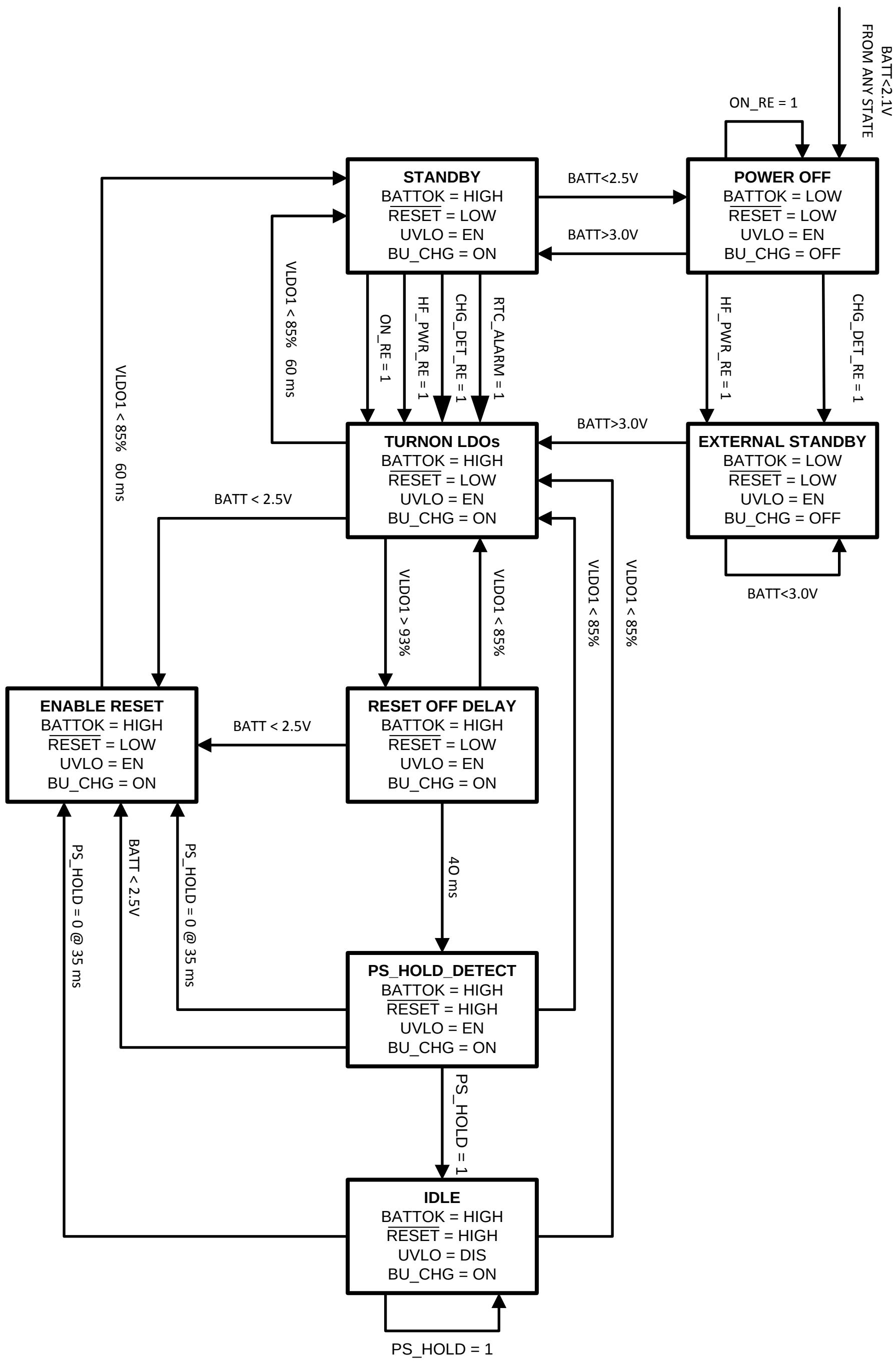
In the PS_HOLD DETECT, $\overline{\text{RESET}}$ is deasserted and the state machine waits 35 ms for the PS_HOLD signal to go high. If PS_HOLD goes high within 35 ms of $\overline{\text{RESET}}$ going low the state machine advances to the IDLE state. If PS_HOLD in still low after 35 ms the state machine goes to ENABLE RESET state and the power down sequence. If battery voltage pins drops below the UVLO threshold, the state machine advances to the ENABLE RESET state and the power down sequence. If LDO1 output drops below its 85% point the state machine returns to the TURNON LDOs state in an attempt to try restart the LDOs.

The state machine remains in the IDLE state until PS_HOLD goes low for 35 ms. If PS_HOLD is low for less than 35 ms the state machine remains in the IDLE state. If PS_HOLD stays low for more than 35 ms, the state machine advances to the ENABLE RESET state and the power down sequence. If LDO1 output falls below its 85% point the state machine returns to the TURNON LDOs state in an attempt to restart the LDOs. The UVLO is disabled in the IDLE state. The back-up battery charger is on.

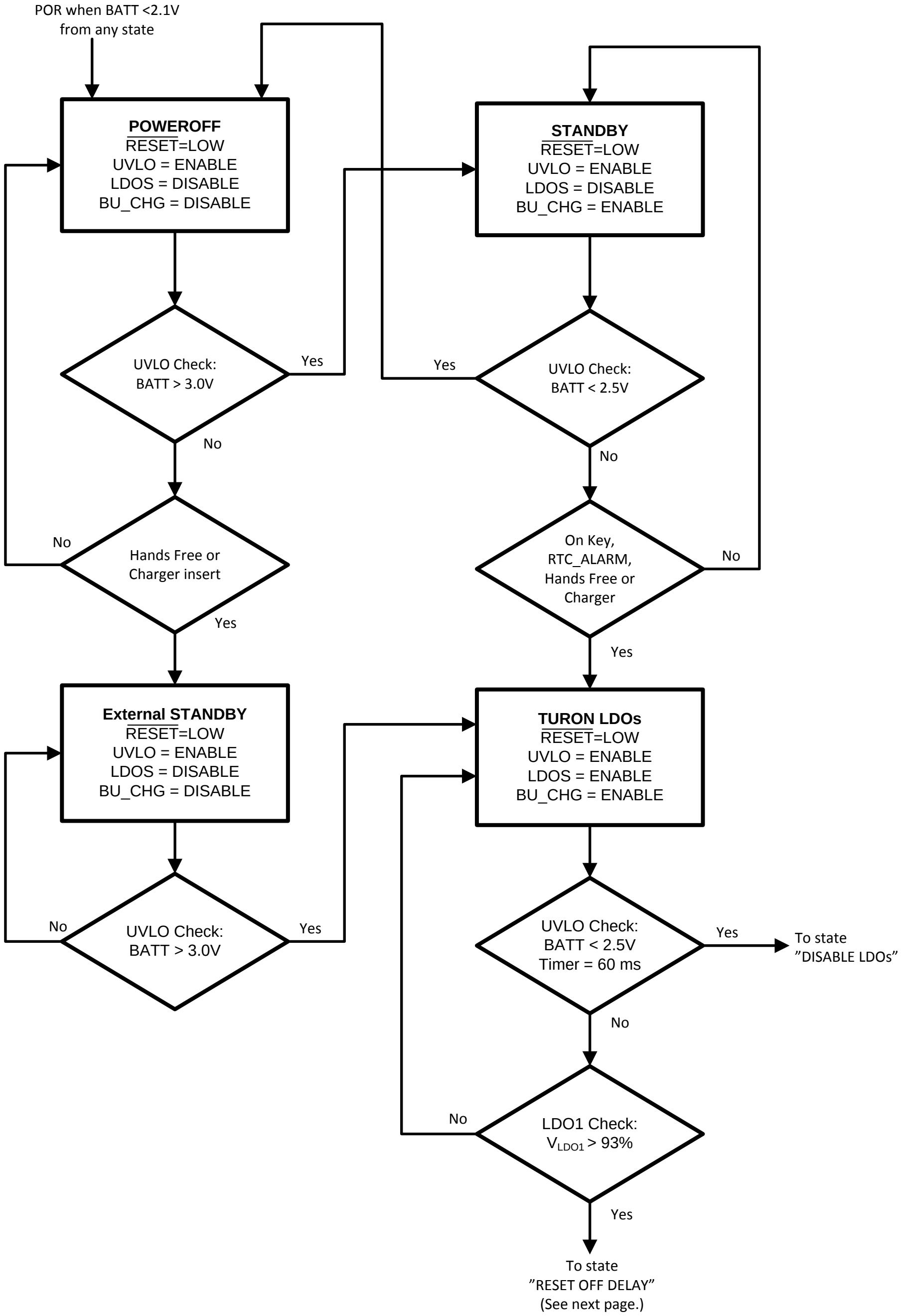
In the ENABLE RESET state $\overline{\text{RESET}}$ is asserted. After 60 ms all LDOs are turned off. UVLO as well as the back-up battery charger are on. Once LDO1 falls to its 85% point the state machine returns to the STANDBY state.

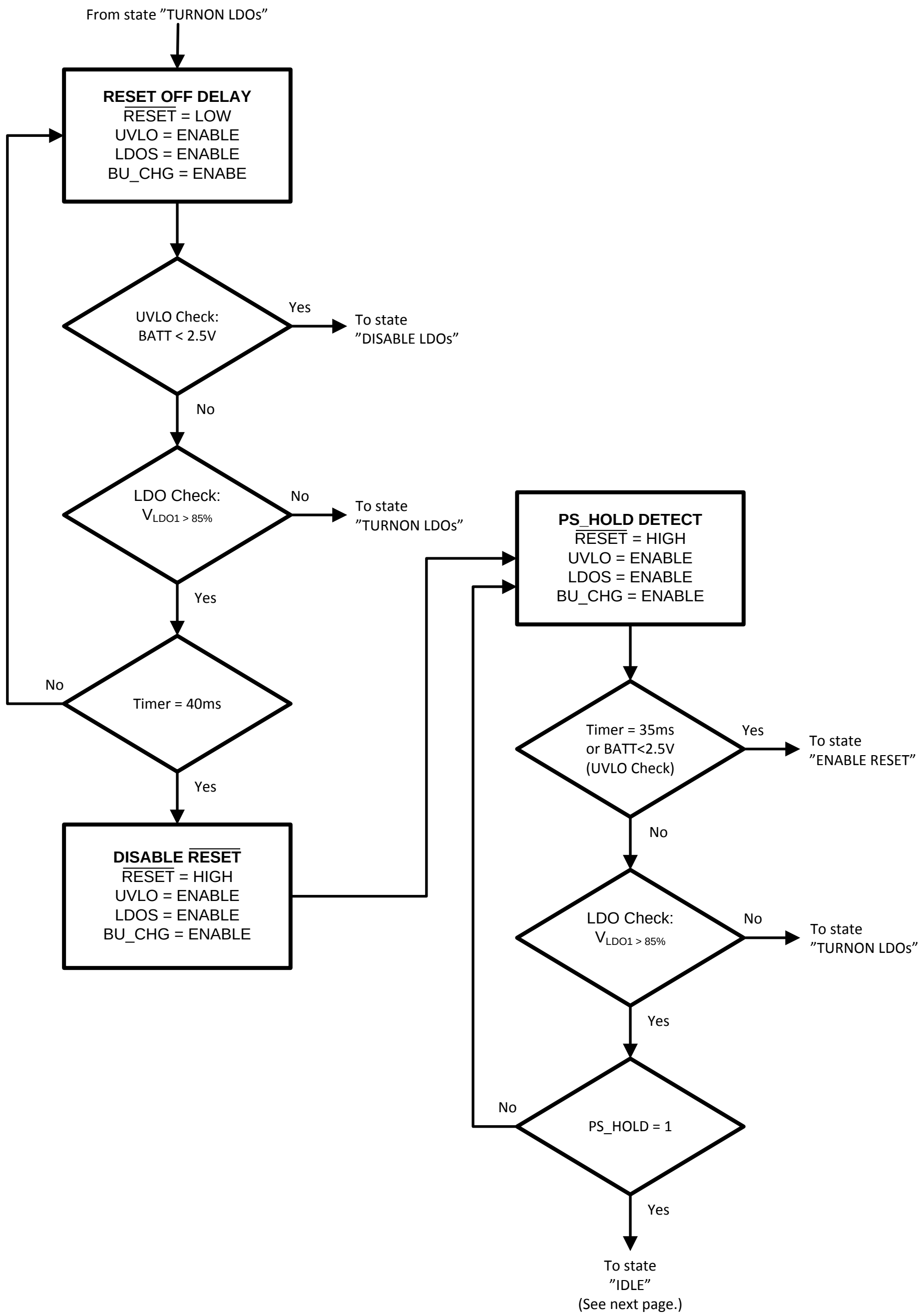
The RTC_LDO is powered by the back-up battery and is always on (unless specifically disabled via the I^2C interface).

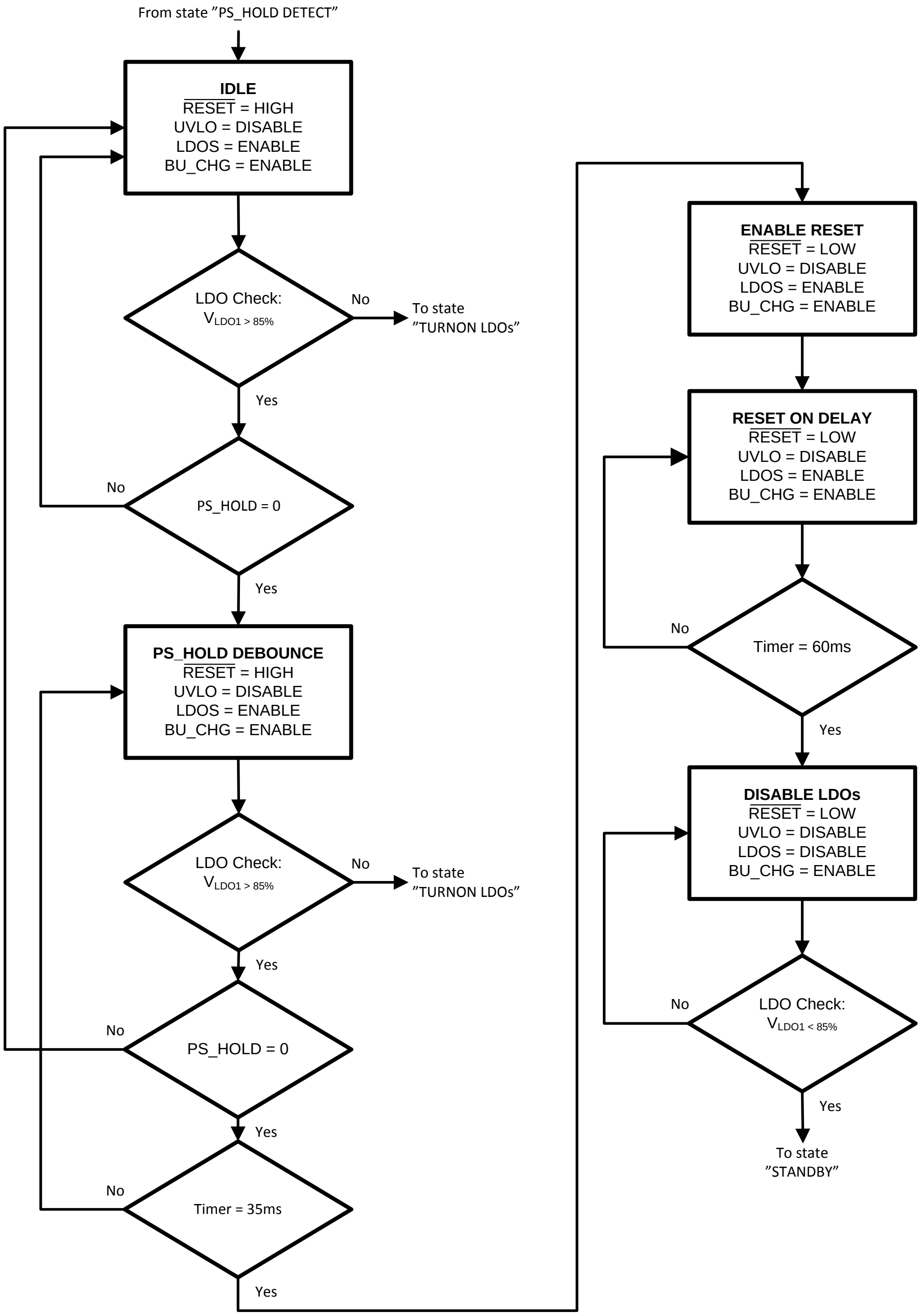
LP3941A Power-Up/Power-Down Flowchart



Detailed PU/PD Flowchart




From state "TURNON LDOs"
RESET OFF DELAY
RESET = LOW
UVLO = ENABLE
LDOS = ENABLE
BU_CHG = ENABE
UVLO Check:
BATT < 2.5V
Yes
To state
"DISABLE LDOs"
No
LDO Check:
VLDO1 > 85%
No
To state
"TURNON LDOs"
Yes
No
Timer = 40ms
Yes
DISABLE RESET
RESET = HIGH
UVLO = ENABLE
LDOS = ENABLE
BU_CHG = ENABLE
PS_HOLD DETECT
RESET = HIGH
UVLO = ENABLE
LDOS = ENABLE
BU_CHG = ENABLE
Timer = 35ms
or BATT<2.5V
(UVLO Check)
Yes
To state
"ENABLE RESET"
No
LDO Check:
VLDO1 > 85%
No
To state
"TURNON LDOs"
Yes
No
PS_HOLD = 1
Yes
To state
"IDLE"
(See next page.)


From state "PS_HOLD DETECT"
IDLE
RESET = HIGH
UVLO = DISABLE
LDOS = ENABLE
BU_CHG = ENABLE
LDO Check:
VLDO1 > 85%
No
To state "TURNON LDOs"
Yes
PS_HOLD = 0
No
Yes
PS_HOLD DEBOUNCE
RESET = HIGH
UVLO = DISABLE
LDOS = ENABLE
BU_CHG = ENABLE
LDO Check:
VLDO1 > 85%
No
To state "TURNON LDOs"
Yes
PS_HOLD = 0
No
Yes
Timer = 35ms
No
Yes
ENABLE RESET
RESET = LOW
UVLO = DISABLE
LDOS = ENABLE
BU_CHG = ENABLE
RESET ON DELAY
RESET = LOW
UVLO = DISABLE
LDOS = ENABLE
BU_CHG = ENABLE
Timer = 60ms
No
Yes
DISABLE LDOs
RESET = LOW
UVLO = DISABLE
LDOS = DISABLE
BU_CHG = ENABLE
LDO Check:
VLDO1 < 85%
No
Yes
To state "STANDBY"

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