# Low Power 2-Channel Central-Office xDSL Driver

Check for Samples: LMH6678

## FEATURES

- $AV_{CC1} = AV_{CC2}$ = +12V, $AV_{DD} = DV_{DD}$ = +3.3V, $T_A$ = 25°C, 2/3 Power Mode, Typical values unless specified.
- Low power consumption
  - Line power $P_{LINE}$ = 100 mW 580 mW/Ch
  - No signal 185 mW/Ch
  - Listen mode 100 mW/Ch
  - Shutdown mode 3 mW/Ch
- Power Supply
  - Analog ($AV_{CC1}$, $AV_{CC2}$) +12V
  - Digital ($DV_{DD}$, $AV_{DD}$) +3.3V
- Output voltage swing @ $R_L$ = 31Ω
  - Single ended 11.5 $V_{PP}$
  - Differential 23 $V_{PP}$
- Multi tone power ratio, f = 500 kHz 72 dB
- Output current 580 mA
- Thermal shutdown protection
- 5mm x 4mm LLP package
- Low thermal resistance 36°C/W ($\theta_{JA}$)
- Small PCB footprint

## APPLICATION

- Full rate ADSL, ADSL+, ADSL++ or G. Lite linecard
- Remote DSLAMs

## DESCRIPTION

The LMH6678 is a low power 2-channel differential output driver utilizing dual current feedback op amps with a fixed gain of $A_V$ = +5.4.

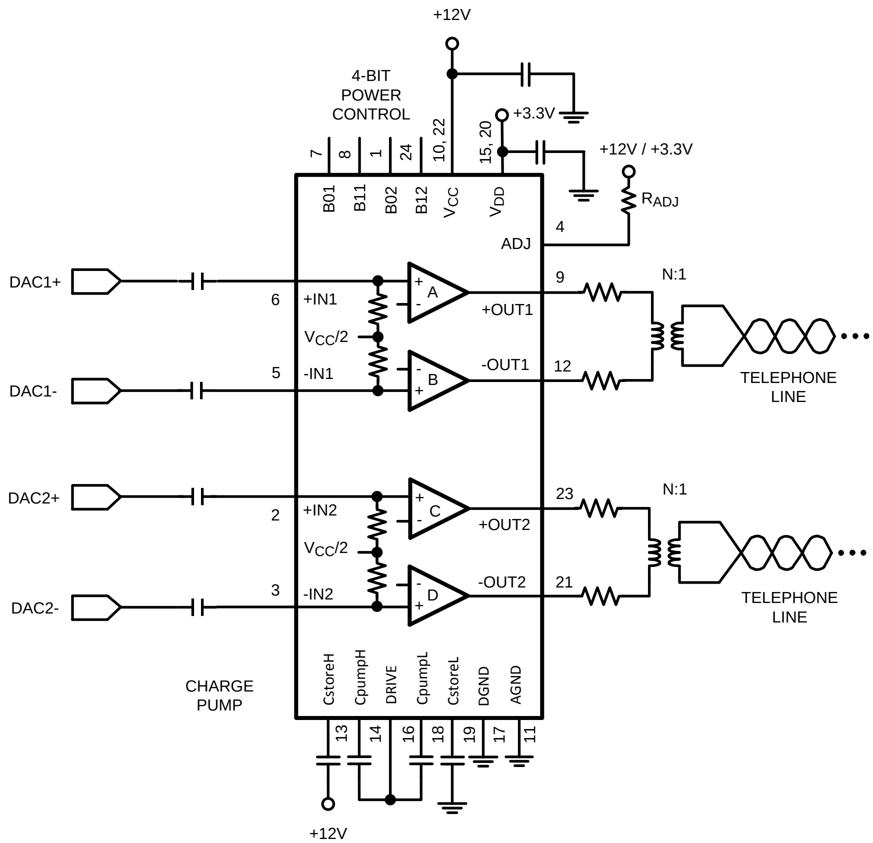
The LMH6678 utilizes high integration with low power consumption to provide 580 mW at 19.8 dBm line output. The LMH6678 can also be put into a listen mode to maintain the termination for receive signals with 100 mW/Ch power dissipation.

The LMH6678 has two separate 2-bit power control inputs compatible with 3.3V CMOS for each channel that enable independent control of line status. When the drivers for both channels are shut off, power consumption drops to only 6 mW.

Thermal Shutdown function protects the IC from a shorted line fault or system over temperature.

The LMH6678 is available in a 5mm x 4mm 24-lead LLP package.

## Block Diagram




These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## Absolute Maximum Ratings [1]

| | |
|---|---|
| ESD Tolerance | |
| Human Body Model | 2KV [2] |
| Machine Model | 200V [3] |
| $V_{IN}$ Differential | ±3V |
| Supply Voltages | |
| $AV_{CC1}$ – AGND or $AV_{CC2}$ – AGND | +13.2V |
| $DV_{DD}$ – DGND | +3.6V |
| $AV_{DD}$ – AGND | +3.6V |
| DGND − AGND | ±0.2V |
| $AV_{CC1}$ – $AV_{CC2}$ | ±0.2V |
| $AV_{DD}$ – $DV_{DD}$ | ±0.2V |
| Voltage at Input Pin | |
| Analog Input | $AV_{CC1}$ ($AV_{CC2}$) +0.8V, AGND −0.8V |
| Digital Control Input | $DV_{DD}$ +0.8V, DGND −0.8V |
| Soldering Information | |
| Infrared or Convection (20 sec.) | 235°C |
| Storage Temperature Range | −65°C to +150°C |
| Junction Temperature [4] | +150°C |

(1) Absolute maximum ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.
(2) Human body model, 1.5kΩ in series with 100pF.
(3) Machine Model, 0Ω in series with 200 pF.
(4) The maximum power dissipation is a function of $T_{J(MAX)}$, $\theta_{JA}$, and $T_A$. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly onto a PC board. Die attach pad is electrically connected to AGND.

## Operating Ratings [1]

| | |
|---|---|
| Supply Voltage | |
| $AV_{CC1}$ to AGND | +12V ±10% |
| $AV_{CC2}$ to AGND | +12V ±10% |
| $DV_{DD}$ to DGND | +3.3V ±10% |
| $AV_{DD}$ to AGND | +3.3V ±10% |
| Operating Temperature Range [2], [3] | −40°C to +85°C |
| Package Thermal Resistance ($\theta_{JA}$) [3] | 36°C/W |

(1) Absolute maximum ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.
(2) Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150° C.
(3) The maximum power dissipation is a function of $T_{J(MAX)}$, $\theta_{JA}$, and $T_A$. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly onto a PC board. Die attach pad is electrically connected to AGND.

## Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J$ = 25°C, $AV_{CC1}$ = $AV_{CC2}$ = +12V, $DV_{DD}$ = $AV_{DD}$ = +3.3V. DGND = AGND = 0V, 2/3 Power Mode. See (1).

| Symbol | Parameter | Conditions | | | | Min (2) | Typ (3) | Max (2) | Units |
|---|---|---|---|---|---|---|---|---|---|
| **Dynamic Performance** | | | | | | | | | |
| $f_{CL}$ | −3 dB BW | $R_L$ = 100Ω | | | | | 50 | | MHZ |
| SR | Slew Rate (4) | $V_{IN\_DIFF}$ = ±2.4V, $R_L$ = 100Ω | | | | | 700 | | V/μs |
| **Distortion and Noise Response** | | | | | | | | | |
| HD2 | 2nd Harmonic Distortion | fc = 1 MHz, $V_O$ = 2 $V_{PP}$, $R_L$ = 31Ω | | | | | −91 | | dBc |
| | | fc = 200 kHz, $V_O$ = 2 $V_{PP}$, $R_L$ = 31Ω | | | | | −98 | | |
| HD3 | 3rd Harmonic Distortion | fc = 1 MHz, $V_O$ = 2 $V_{PP}$, $R_L$ = 31Ω | | | | | −57 | | dBc |
| | | fc = 200 kHz, $V_O$ = 2 $V_{PP}$, $R_L$ = 31Ω | | | | | −71 | | |
| MTPR | Multi-Tone Power Ratio | f = 500 kHz | | | | | 72 | | dBc |
| $V_{IN}$ | Differential Output Noise | 100 kHz to 10 MHz | | | | | 57 | | $nV/\sqrt{Hz}$ |
| **Input Characteristics** | | | | | | | | | |
| $V_{IN}$ | Input DC Voltage | Common Mode | | | | 6.04 | 6.1 | 6.16 | V |
| $R_{IN}$ | Input Resistance | Differential<br>$I_{DIFF}$ = 10 μA from +IN to −IN | | | | 14.4 | 20 | 28.4 | kΩ |
| **Transfer Characteristics** | | | | | | | | | |
| $A_V$ | Voltage Gain | $V_{IN\_DIFF}$ = −1 to 1V, No Load | | | | +5.37 | +5.40 | +5.48 | V/V |
| PSRR | Power Supply Rejection Ratio | | | | | | −108 | | dB |
| Xt | Cross Talk | f = 1 MHz, $R_L$ = 100Ω | | | | | −95 | | |
| $V_O$ | Output Voltage Swing High | $V_{IN\_DIFF}$ = ±2.4V, No Load | | | | | 11.85 | | V |
| | | $V_{IN\_DIFF}$ = ±2.4V, $R_L$ = 31Ω | | | | 11.68 | 11.75 | | |
| | | $V_{IN\_DIFF}$ = ±2.4V, $I_{OUT}$ = 580 mA | | | | 11.64 | 11.74 | | |
| | Output Voltage Swing Low | $V_{IN\_DIFF}$ = ±2.4V, No Load | | | | | 0.15 | | V |
| | | $V_{IN\_DIFF}$ = ±2.4V, $R_L$ = 31Ω | | | | | 0.25 | 0.36 | |
| | | $V_{IN\_DIFF}$ = ±2.4V, $I_{OUT}$ = 580 mA | | | | | 0.31 | 0.39 | |
| $I_{SC}$ | Output Short Circuit Current | Sourcing to Ground | | | | | +800 | | mA |
| | | Sinking to Ground | | | | | −800 | | |
| $I_{OUT}$ | Output Current | $V_{IN\_DIFF}$ = ±2.4V<br>Sourcing, $R_L$ = 20Ω<br>Sinking, $R_L$ = 20Ω | | | | | ±580 | | mA |
| $V_{OC}$ | Output Common Mode Voltage | | | | | 5.89 | 6 | 6.05 | V |
| $V_{OS}$ | Output Offset Voltage | | | | | −40 | 0 | +40 | mV |
| **Power Supply (5), (6)** | | | | | | | | | |
| $I_{CC}$ | $AV_{CC}$ Quiescent Supply Current | B01 | B11 | B02 | B12 | | | | |
| | Full Power | L | L | L | L | 28.6 | 33 | 36.9 | mA |
| | 2/3 Power | H | L | H | L | 18.6 | 22 | 25.4 | |
| | 1/3 Power | L | H | L | H | 9.2 | 12 | 14.3 | |
| | Shutdown | H | H | H | H | | 0.2 | .95 | |

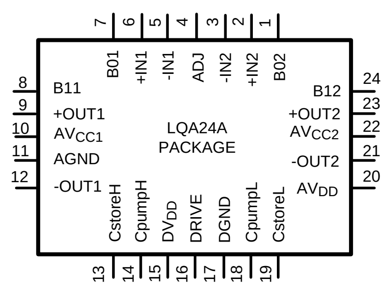
(1) Electrical table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J$ = $T_A$. No guarantee of parametric performance is indicated in the electrical tables under conditions of internal self heating where $T_J$ > $T_A$. Absolute maximum ratings indicate junction temperature limits beyond which the device may be permanently degraded, either mechanically or electrically.
(2) All limits are guaranteed by testing or statistical analysis.
(3) Typical Values represent the most likely parametric norm.
(4) Slew rate is the slowest of the rising and falling slew rates.
(5) Quiescent supply current specification apply for the condition of no input signal. See application section for information on power consumption as a function of output power, power control bit settings and external resistor $R_{ADJ}$.
(6) “L” is $V_{IL}$ and “H” is $V_{IH}$.

## Electrical Characteristics (continued)

Unless otherwise specified, all limits guaranteed for $T_J$ = 25°C, $AV_{CC1}$ = $AV_{CC2}$ = +12V, $DV_{DD}$ = $AV_{DD}$ = +3.3V. DGND = AGND = 0V, 2/3 Power Mode. See [1].

| Symbol | Parameter | Conditions | | | | Min [2] | Typ [3] | Max [2] | Units |
|---|---|---|---|---|---|---|---|---|---|
| $I_{DV}$ | $DV_{DD}$ Quiescent Supply Current | B01 | B11 | B02 | B12 | | | | mA |
| | Full Power | L | L | L | L | 11 | 16 | 19 | |
| | 2/3 Power | H | L | H | L | 7 | 12 | 15 | |
| | 1/3 Power | L | H | L | H | 3 | 7 | 10.3 | |
| | Shutdown | H | H | H | H | | 0.05 | .14 | |
| $I_{AV}$ | $AV_{DD}$ Quiescent Supply Current | All Power Modes | | | | .8 | 1.1 | 1.4 | mA |
| **Logic Inputs** | | | | | | | | | |
| $V_{IH}$ | Input High Voltage | | | | | 2.7 | 3.3 | | V |
| $V_{IL}$ | Input Low Voltage | | | | | | 0 | 0.5 | V |
| $I_{IH}$ | Input High Current | @ $V_{IH}$ = 3.3V | | | | −0.5 | 0.02 | +0.5 | μA |
| $I_{IL}$ | Input Low Current | @ $V_{IH}$ = 0V | | | | −0.5 | 0.02 | +0.5 | μA |
| **Charge Pump** | | | | | | | | | |
| $f_{CP}$ | Charge Pump Frequency | Measure at DRIVE at Full Power | | | | 2.43 | 2.75 | | MHz |
| $V_{HIGH}$ | Charge Pump High Average Voltage | Measure at CstoreH at Full Power | | | | | +14.6 | | V |
| $V_{LOW}$ | Charge Pump Low Average Voltage | Measure at CstoreL at Full Power | | | | | −2.7V | | V |

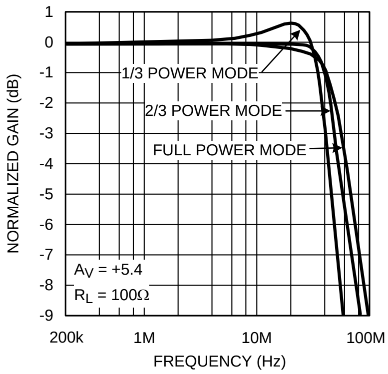
## Connection Diagram



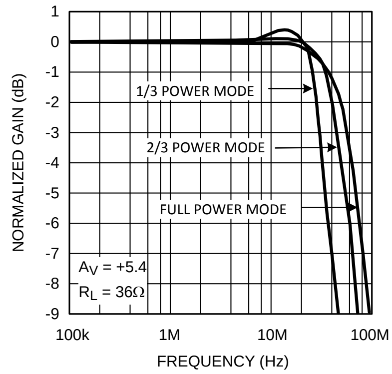

Note: Die attach pad is electrically connected to AGND

## Typical Performance Characteristics

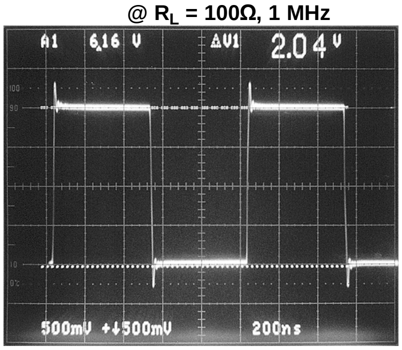
**Single-Ended Small Signal Frequency Response @ $R_L$ = 100Ω**



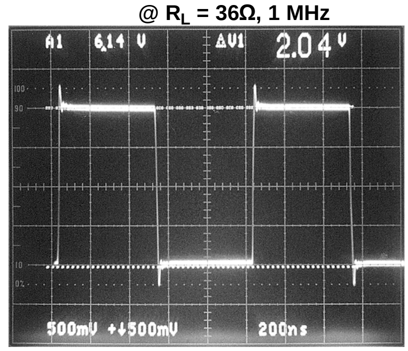

**Single-Ended Small Signal Frequency Response @ $R_L$ = 36Ω**



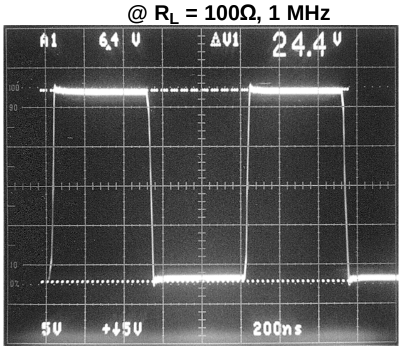

**Medium Signal Pulse Response @ $R_L$ = 100Ω, 1 MHz**



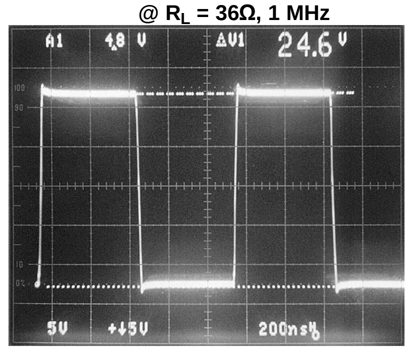

**Medium Signal Pulse Response @ $R_L$ = 36Ω, 1 MHz**



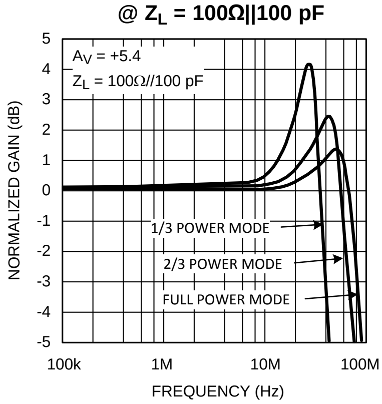

**Large Signal Pulse Response @ $R_L$ = 100Ω, 1 MHz**



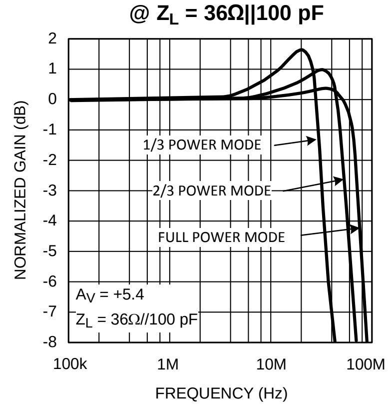

**Large Signal Pulse Response @ $R_L$ = 36Ω, 1 MHz**




**Single-Ended Small Signal Frequency Response @ $Z_L$ = 100Ω||100 pF**



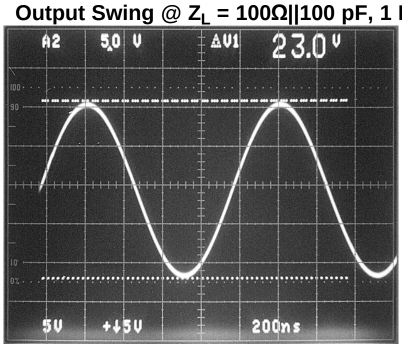

**Single-Ended Small Signal Frequency Response @ $Z_L$ = 36Ω||100 pF**



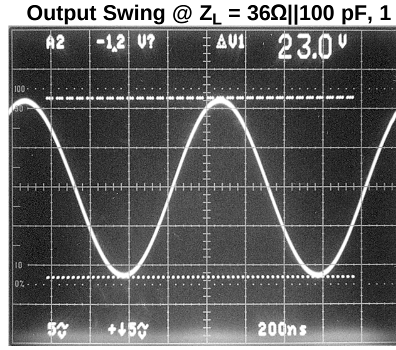

 

## Typical Performance Characteristics (continued)

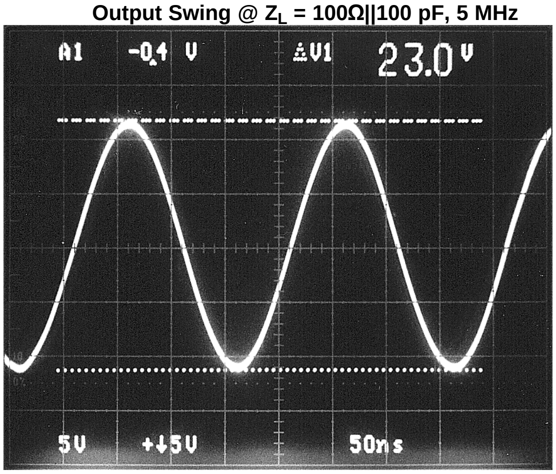
**Output Swing @ $Z_L$ = 100Ω||100 pF, 1 MHz**



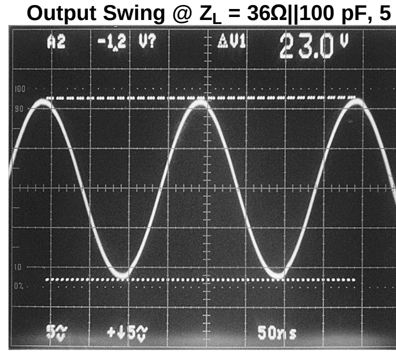

**Output Swing @ $Z_L$ = 36Ω||100 pF, 1 MHz**



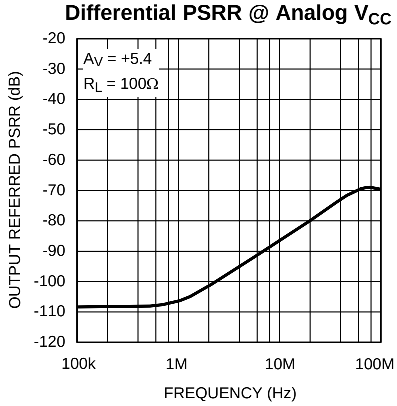

**Output Swing @ $Z_L$ = 100Ω||100 pF, 5 MHz**



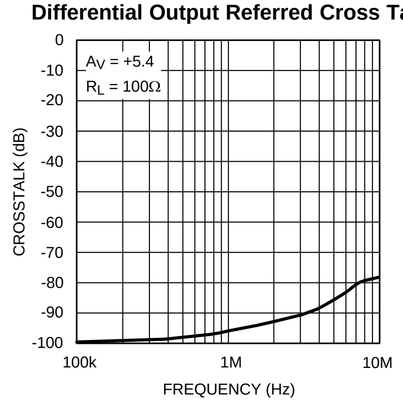

**Output Swing @ $Z_L$ = 36Ω||100 pF, 5 MHz**



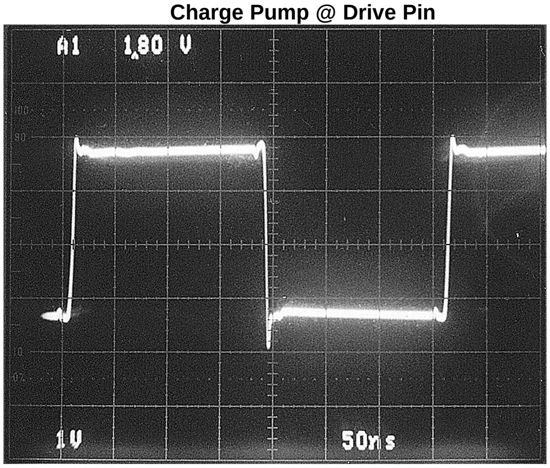

**Differential PSRR @ Analog $V_{CC}$**



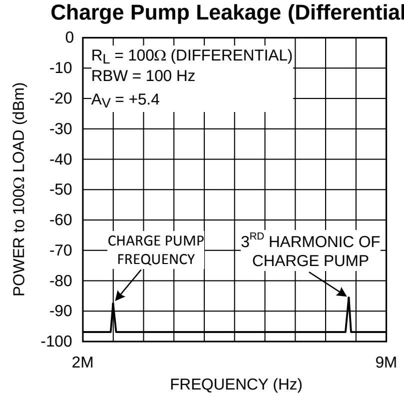

**Differential Output Referred Cross Talk**




**Charge Pump @ Drive Pin**

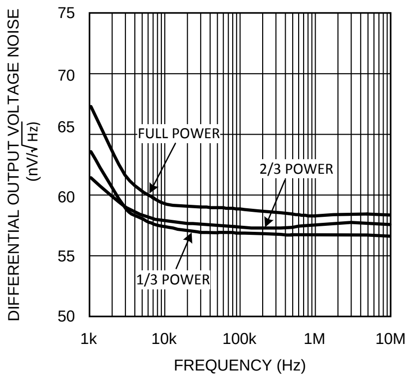



**Charge Pump Leakage (Differential)**

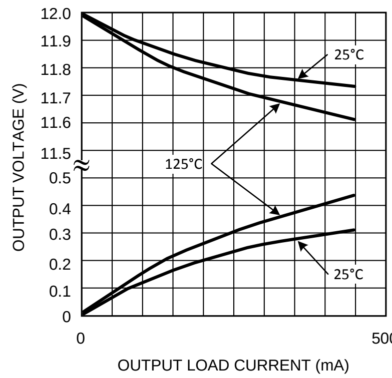


## Typical Performance Characteristics (continued)

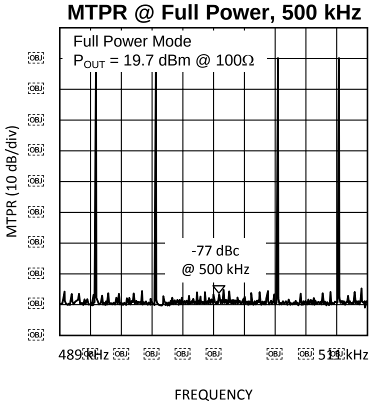
**Output Voltage Noise @ $R_S$ = 50Ω**



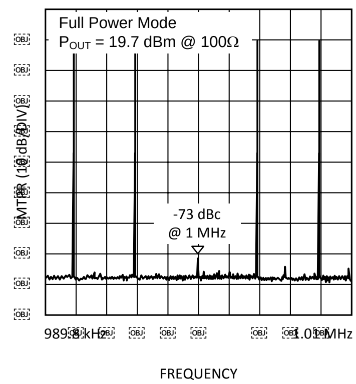

**Output Voltage Swing**



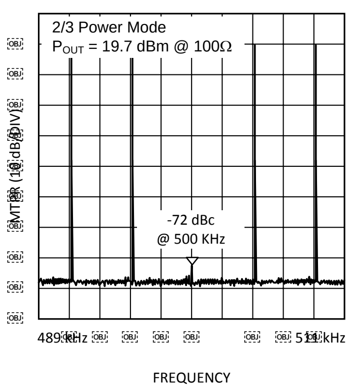

**MTPR @ Full Power, 500 kHz**



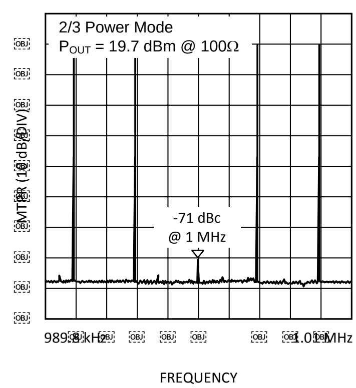

**MTPR @ Full Power, 1 MHz**



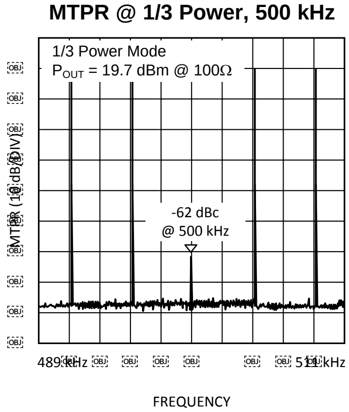

**MTPR @ 2/3 Power, 500 kHz**



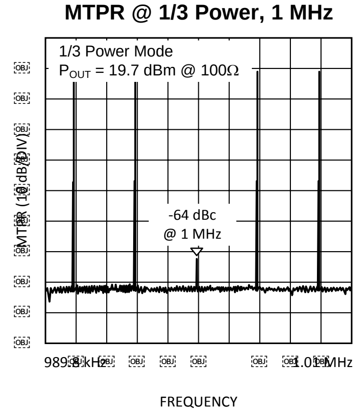

**MTPR @ 2/3 Power, 1 MHz**




**MTPR @ 1/3 Power, 500 kHz**

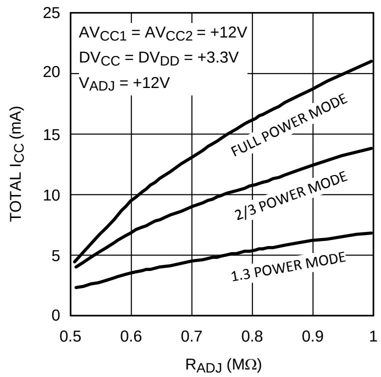



**MTPR @ 1/3 Power, 1 MHz**

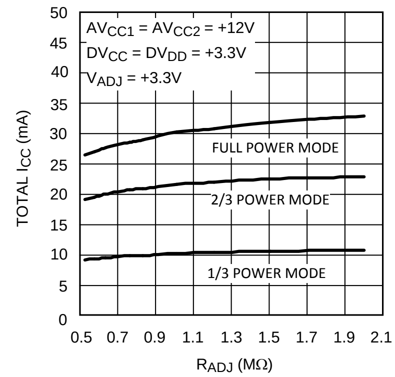


## Typical Performance Characteristics (continued)

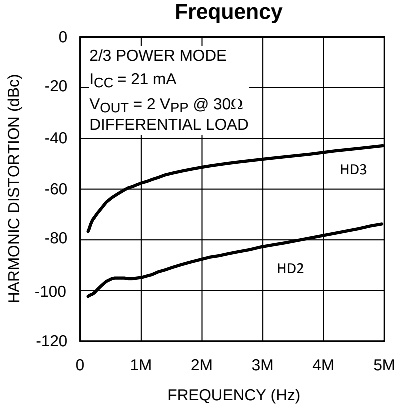
**Detail View of Total $I_{CC}$ vs. $R_{ADJ}$ @ $V_{ADJ}$ = +12V**



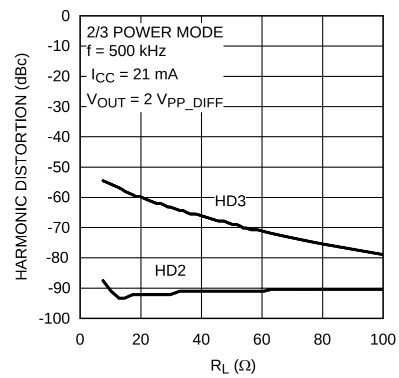

**Detail View of Total $I_{CC}$ vs. $R_{ADJ}$ @ $V_{ADJ}$ = +3.3V**



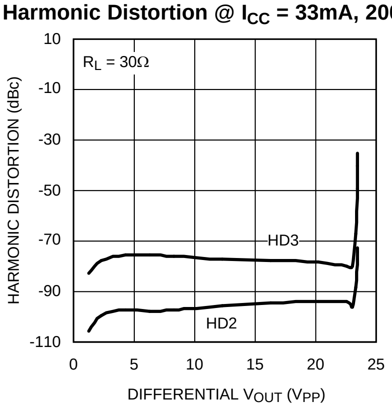

**Harmonic Distortion vs. Frequency**



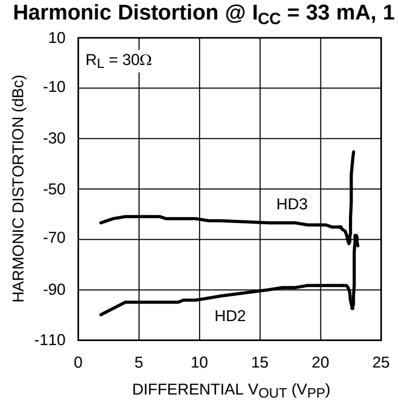

**Harmonic Distortion vs. Load**




**Harmonic Distortion @ $I_{CC}$ = 33mA, 200 kHz**

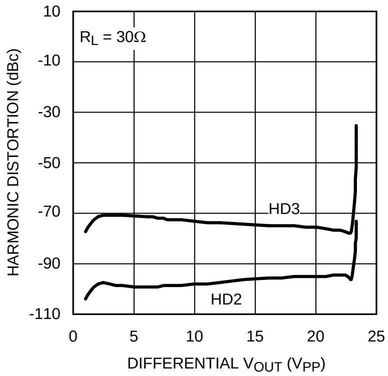



**Harmonic Distortion @ $I_{CC}$ = 33 mA, 1 MHz**

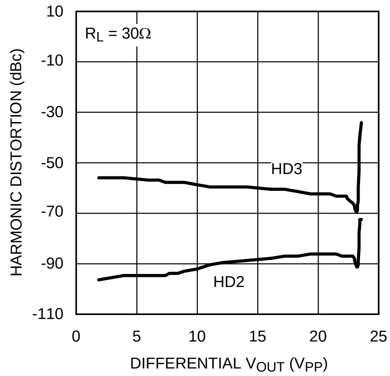


## Typical Performance Characteristics (continued)

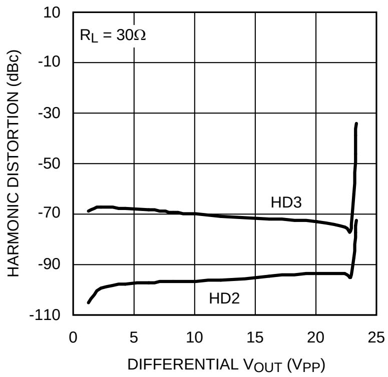
**Harmonic Distortion @ $I_{CC}$ = 21 mA, 200 kHz**



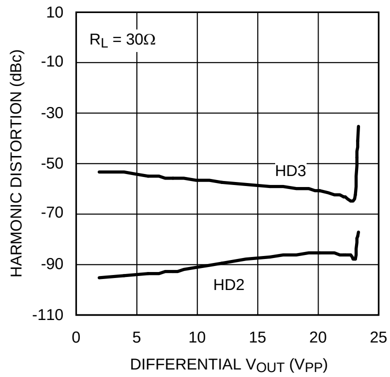

**Harmonic Distortion @ $I_{CC}$ = 21 mA, 1 MHz**



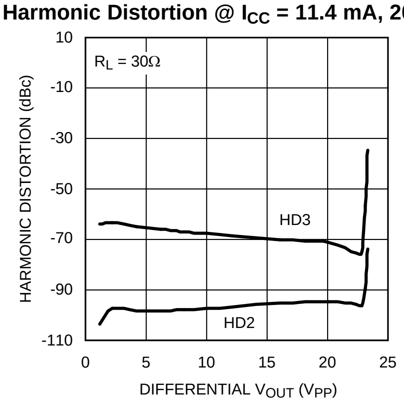

**Harmonic Distortion @ $I_{CC}$ = 16 mA, 200 kHz**



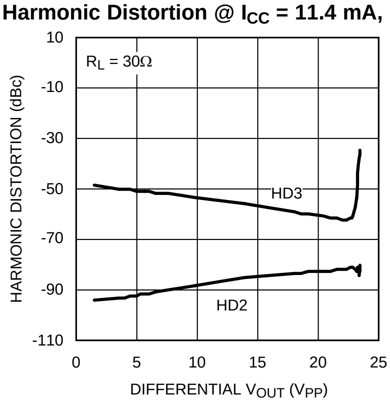

**Harmonic Distortion @ $I_{CC}$ = 16 mA, 1 MHz**




**Harmonic Distortion @ $I_{CC}$ = 11.4 mA, 200 kHz**




**Harmonic Distortion @ $I_{CC}$ = 11.4 mA, 1 MHz**




## Application Notes

### FUNCTIONAL DESCRIPTION

The LMH6678 contains two pairs of high speed/high output current operational amplifiers configured as two amplifiers differential inputs and outputs, as shown in Figure 1. Quiescent current can be set independently for each channel via two control bits as depicted in Table 1. Also, quiescent current can be continuously varied by selection of an external resistor between the ADJ pin and a supply voltage of either +12V or +3.3V.

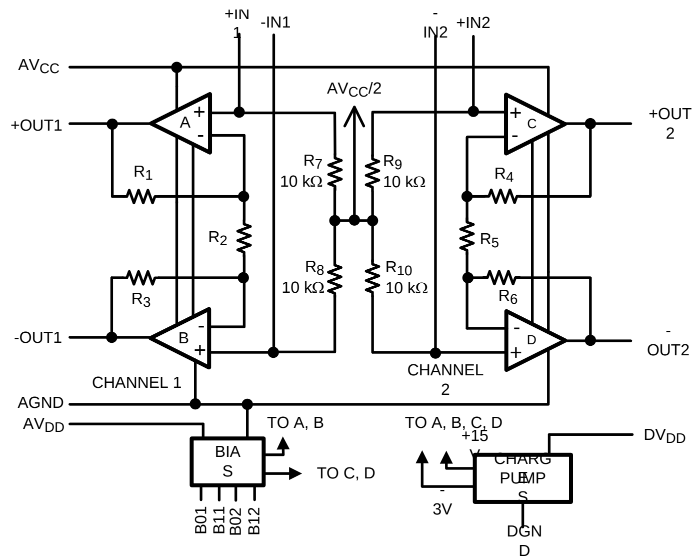



**Figure 1. Functional Block Diagram**

**Table 1. Power Mode Logic Control**

| | Channel A (B) | |
|---|---|---|
| **Power Mode** | **B01 (B02)** | **B11 (B12)** |
| **Full Power** | L | L |
| **2/3 Power** | H | L |
| **1/3 Power** | L | H |
| **Shutdown** | H | H |

Two supply voltages are required, +12V ±10% and +3.3V ±10%. Current for the driver amplifiers, including their output current, flows from the 12V analog $V_{CC}$ ($AV_{CC}$) supply and Analog Ground (AGND.) For proper output swing and distortion performance, both $AV_{CC}$ pins must be connected to +12V and the exposed metal pad must be soldered to ground potential as described in the layout section. Both $AV_{DD}$ and $DV_{DD}$ pins must be connected to +3.3V. The internal bias circuitry is powered from $AV_{DD}$ and AGND while the digital circuitry and charge pump are powered from $DV_{DD}$ and DGND. This allows separate bypassing and decoupling for $AV_{DD}$ and $DV_{DD}$.

All supply voltage pins need a 0.1 µF ceramic capacitor in parallel with a 4.7 µF capacitor as bypass capacitors. The 0.1 µF capacitor should be as close as possible to the supply voltage pin and the larger capacitor placed next to it.

The LMH6678 delivers very low power consumption at a single +12V analog supply voltage by a combination of its circuit architecture and the on-chip dual charge pump. The output stage is an emitter-follower type, which can provide low distortion, low quiescent current and high peak output currents.

The charge pumps generate two internal dc voltages, $V_{HIGH}$ = +15V and $V_{LOW}$ = −3V. As shown in Figure 2, $V_{HIGH}$ and $V_{LOW}$ supply base currents for the output stages. This enables the drivers to swing within a $V_{CE}$(sat) of $V_{CC}$ and ground, giving the LMH6678 its high swing of +11.5 $V_{PP}$ into a 31Ω load.

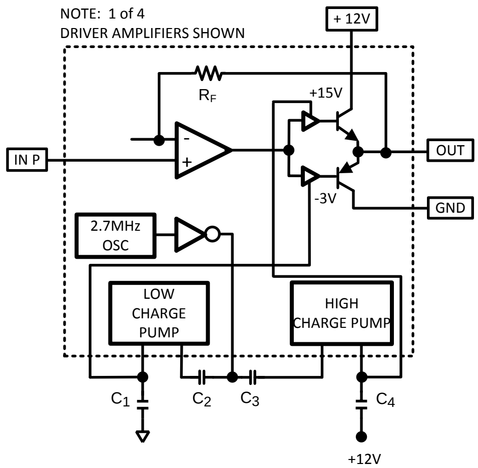



**Figure 2. Internal Connections of Integrated Charge Pumps**

## CHARGE PUMPS

Figure 3 is a simplified schematic of the internal charge pumps. Each pump consists of a transfer capacitor and a reservoir capacitor and switches. The states of switches are driven by an internal 2.75 MHz clock oscillator. The transfer capacitor of the high charge pump, C1, is connected across $DV_{DD}$ and DGND during one phase of the clock and between $V_{HIGH}$ and $AV_{CC}$ during the opposite phase. This causes its reservoir capacitor, $C_2$, to charge up to $DV_{DD}$ (3.3Volts) potential less a small drop due to finite switch resistance. $V_{HIGH}$ therefore is pumped to nearly $V_{CC}$ + $V_{DD}$ potential or approximately +15V.

Similarly, the transfer capacitor of the low charge pump, $C_3$, is connected across $DV_{DD}$ and DGND during one phase of the clock and between AGND and $V_{LOW}$ during the opposite phase. This causes its reservoir capacitor, $C_4$, to charge up to $V_{DD}$ potential less a small drop due to finite switch resistance. $V_{LOW}$ therefore is pumped to nearly $-V_{DD}$ potential or approximately −3V.

The charge pumps outputs provide both dc bias currents and the base current of the output transistors. These base currents are small compared to the dc bias currents. Typical and maximum quiescent $V_{DD}$ supply currents are given in the electrical characteristics. Thus, for the charge pump capacitors $C_1$-$C_4$, the suggested values are 0.022 µF 20% X7R type. With theses values, the ripple on $V_{HIGH}$ and $V_{LOW}$ will be approximately 40 $mV_{PP}$. This results in a small spurious output on the line of typically −120 dBm/Hz at 2.75 MHz. Spurs produced at harmonics of the clock frequency are at least 20 dB lower and further attenuated by the transformer. This is shown in the typical performance characteristics section. Ripple and spurious outputs can be further attenuated by increasing the size of the reservoir capacitors $C_2$ and $C_4$.

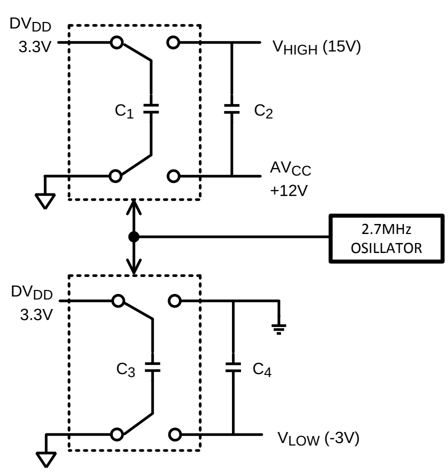



**Figure 3. Charge Pump Functional Schematic**

## MULTI-TONE POWER RATIO AND NOISE

The Multi-Tone Power Ratio of the LMH6678 is shown in the typical performance characteristics section. MTPR is the best representation of non-linearity for ADSL modems. The measurement is accomplished with all ADSL bins transmitting full power except one. The delta between the peak amplitude of the transmitting carriers and energy left in the single bin defines the maximum available SNR for that bin. The test circuit is described in Figure 4. Here $R_2$, $C_3$, $R_4$ and $C_4$ were added for increase gain.

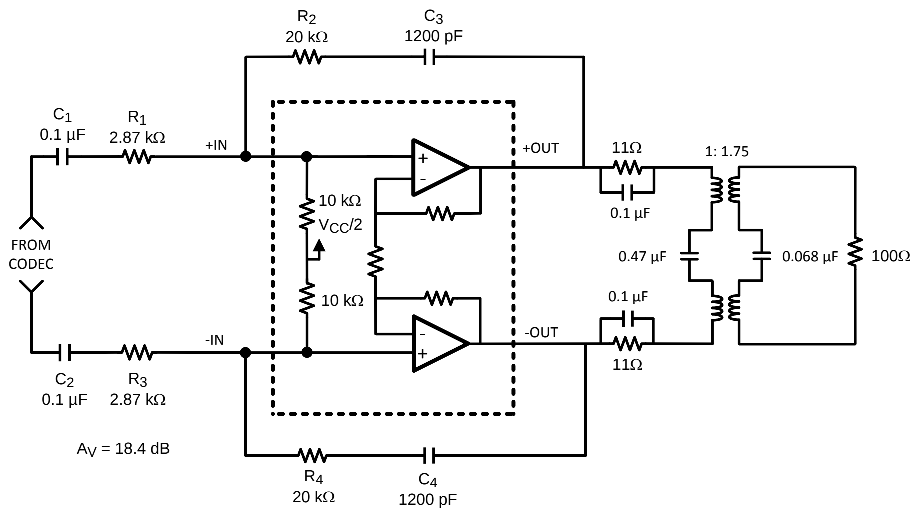



**Figure 4. MTPR Measurement Test Circuit**

## R-C TERMINATION CIRCUIT AND TRANSFORMER TURNS RATIO

The LMH6678 was designed to operate in the circuit of Figure 5. In this circuit, resistor $R_1$ and $R_2$ provide a line termination in the upstream band. At higher frequencies in the downstream band, capacitors $C_1$ and $C_2$ bypass $R_1$ and $R_2$ for higher efficiency.

To calculate the transformer turns ratio required, we assume a peak-to-rms ratio of 5.8 must be supported and the $V_{CC}$ supply tolerance is 5%. At a 30Ω load, the driver outputs can swing to 350 mV of each rail with low distortion. This gives a peak swing of 12(.95) −0.7 = 10.7V. A typical selection for $C_1$, $C_2$, $R_1$ and $R_2$ results in approximately 0.1 dB loss and the transformer loss is typically 0.25 dB, so total voltage loss is about 0.35 dB.

For 19.8 dBm output, line rms voltage is 3.09 and peak voltage is 17.9. The optimum turns ratio is calculated at 1.035 x 17.9/10.7 = 1.73. This gives a reflected line impedance of $100\Omega/(1.73)^2$ = 33.4 at the primary side. $R_1$ and $R_2$ are usually chosen to be 33.4/2 = 16.7 to terminate the line at lower frequencies.

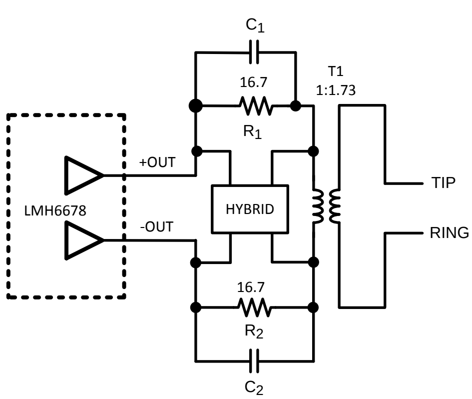



**Figure 5. Typical R-C Termination**

## INPUT POWER LEVEL AND GAIN

With losses included, output power from the LMH6678 should be 19.8 dBm + 0.35 dB = 20.15 dBm or 103.5 mW. At 33.4Ω, the rms differential output voltage is √(PxR) = 1.86 Vrms. The driver amplifiers have a voltage gain of 5.4V/V, so the input level should be 1.86/5.4 = 344 $mV_{RMS}$ to deliver 19.8 dBm to the line.

The driver input equivalent circuit is shown in Figure 1. The inputs should be capacitively coupled to maintain the input and output common-mode voltage at $V_{CC}/2$.

If additional gain is required, the gain can be increased with positive feedback using the circuit of Figure 6. In this case the voltage gain $A_V$ will be

$$A_V = 5.4*(1-K)/(1-5.4*K) \quad (1)$$

Where

$$K = (R_1||10K)/(R_1||10K + R_2) = 10K*R_1(10K*R_1 + R_1R_2 + 10K*R_2) \text{ and } R_1 = R_3, R_2 = R_4 \quad (2)$$

It is suggested to choose $R_1$ < 3K so that the 15% tolerance of the input resistance will not greatly affect the gain. Furthermore, this circuit will have a differential input resistance of

$$R_{IN\_DIFF} = 2*R_1 - 2*R_2/(4.4) \quad (3)$$

which may be negative in band. Usually no stability problems are seen if this $|R_{IN}|$ is chosen larger than 500Ω. To minimize distortion caused by loading on the Codec outputs, $|R_{IN}|$ is usually chosen to be 1kΩ or more. Additional blocking capacitors $C_3$ and $C_4$ must be inserted in series with $R_2$ and $R_4$ to prevent the circuit from latching. $C_3$ and $C_4$ should be chosen to be less than 1/5 of $C_1$ to avoid large signal oscillation.

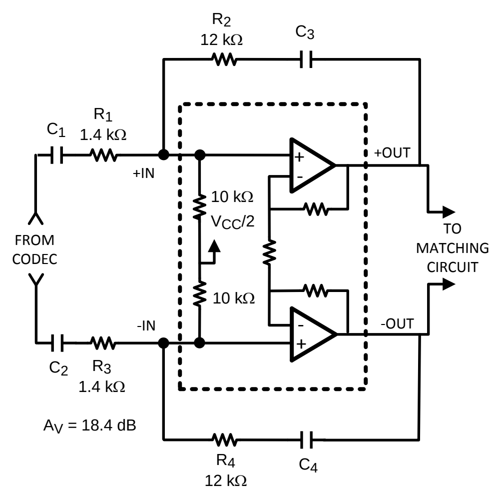



**Figure 6. Increasing Gain**

## ACTIVE TERMINATION CIRCUIT

The LMH6678 can be used to synthesize the output impedance by using positive feedback to increase the output resistance. In ADSL this technique is often used to lower the total power consumption of the line driver by reducing the voltage across the series termination resistors. This approach gives slightly higher power consumption but better return loss in the downstream band compared to the R-C termination of Figure 5. The equations that follow and Figure 7 describe how to implement this technique with the LMH6678.

1. Pick positive feedback factor (also called the resistance gain), $A_Z$.
2. Pick desired output resistance, $R_{OUT}$, seen by the line.
3. Calculate transformer turns ratio based on $A_Z$, line driver voltage swing, and transformer insertion loss (TIL). $R_L$ is the line impedance, 100Ω for ADSL. $N = [(V_{LINEPP}/(2 * 11.2)]* [(1 + R_{OUT}/(R_L * A_Z)] * 10^{(TIL/20)}$
4. Calculate $R_4$ from $R_{OUT}$, $A_Z$, and $NR_4 = R_{OUT} / (2 * A_Z * N^2)$
5. Calculate the resistance looking into the transformer secondary (chip side).$R_{SEC} = R_L / N^2$
6. Calculate $K_1$. $K_1 = (A_Z - 1)/(5.4 * A_Z)$
7. Calculate $K_2$.$K_2 = R_{SEC}/(R_{SEC} + 2 * R_4)$

8. Pick a value for $R_2$. Typically 3kΩ is a good value.
9. Calculate $R_{EQ}$.$R_{EQ} = R_2/(1\text{-}5.4^* K_2)$ (Note $R_{EQ}$ is usually negative.)
10. Calculate $R_{IN}$ $R_{IN} = [(K_1{*}R_2)/(1\text{-}K_1){*}10k]/[10k\text{-}(K_1{*}R_2)/(1\text{-}K_1)]$
11. Calculate the gain without the input voltage divider.$A_{V1} = N{*}5.4{*}K_2 * [(R_{EQ}//10k)/(R_{IN} + R_{EQ}//10k)] /(10^{TIL/20})$
12. . Calculate $A_{VTOTAL}$ the final required gain from input to the line.$A_{VTOTAL} = V_{LINERMS}/V_{INRMS}$
13. . Calculate the voltage divider network of R1 and R3 using $A_{V1}$, transformer insertion loss (TIL),$R_1 = R_{IN} * [A_{V1}/(A_{VTOTAL}{*}10^{TIL/20})]R_3 = (2 * R_{IN})/[1 - (A_{VTOTAL}{*}10^{TIL/20})/ A_{V1}]$

The example shown in Figure 7 is designed to the following parameters:

$V_{LINERMS}$ = 3.13V (19.8 dBm output power)

$A_Z$ = 4.5

$R_{OUT}$ = 65Ω (13.5dB return loss)

Crest Factor = 5.8 @ nominal 12V supply

Transformer Insertion Loss = 0.4dB

$V_{INRMS}$ = 350mV (AFE output level)

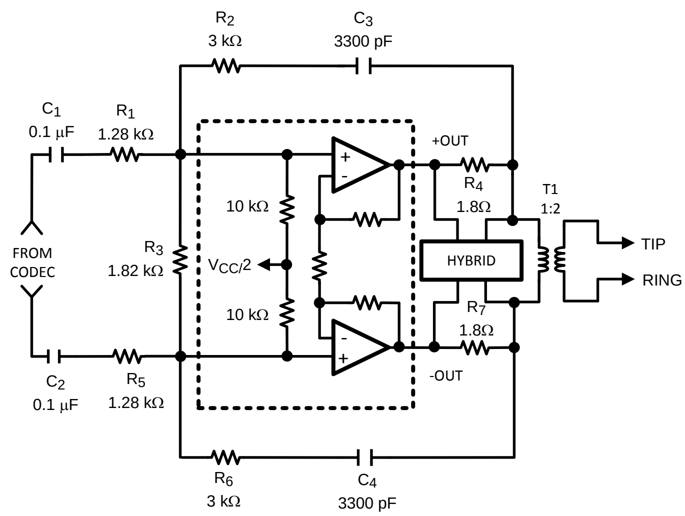



**Figure 7. Active Termination Application**

## POWER CONSUMPTION

Power consumption is a function of line power and dynamic bias current of the line driver. After the transformer turns ratio has been selected as described above, power consumption per channel for the typical R-C termination application can be estimated as follows:

$$I_{CC} = IdB + I_{LOAD} \quad (4)$$

$$IdB = 0.25 * Iq \quad (5)$$

This is because 25% of the total dc current flows in the output transistors. This term effectively vanishes when the class AB stage is drives a heavy load.

**Where** $I_{LOAD}$ = average load current driven by output transistors
IdB = dynamic $V_{CC}$ bias current while driving full load power
$I_{CC}$ = average $V_{CC}$ current

When losses included, 103.5 mW is delivered by the driver, therefore

$$I_{RMS} = TR^* \sqrt{(.1035/100)} = 32.2\text{ mA} \quad (6)$$

Since the ADSL signal is DMT and is effectively guassian, the average value of the supply current due to driving the load is given by

$I_{LOAD}$ = average|$I_{RMS}$| = √(2/π)*$I_{RMS}$ = 0.8 * $I_{RMS}$ = 44.6 mA for TR = 1.73 (7)

Assuming 2/3 power mode, Ifixed = 0.25 * 11 mA = 2.75 mA

$I_{CC}$ = 2.75 mA + 44.6 mA = 47.4 mA (8)

$P_{CC}$ = $I_{CC}$ x $V_{CC}$ = 569 mW (9)

To get the $I_{DD}$ full current, simply add 0.75 mA to the quiescent current per channel:

$I_{DD}$ = 0.75 + 5.5 + 0.6 = 6.8 mA (10)

$P_{DD}$ = $V_{DD}$ * $I_{DD}$ = 23 mW (11)

For the total power consumption per channel,

$P_{CON}$ = $P_{DD}$ + $P_{CC}$ = 592 mW (12)

For power dissipation of the LMH6678, subtract the power into the load plus external losses:

$P_{DISS}$ = 592-103 = 489 mW per channel (13)

$P_{DISS}$ total = 2 x 489 = 978 mW for both channels (14)

Proper selection of the external resistor between the ADJ pin can optimize the trade-off between power consumption and distortion. This external resistor will reduce the supply current for the 1/3, 2/3 and full bias settings for both channels. The approximately equation is

$I_S$ = $I_S$ * (1- ($V_{CC}$-0.8)/(30μA*$R_{ADJ}$)) (15)

Curves of $V_{CC}$ and $V_{DD}$ supply currents per channel vs. $R_{ADJ}$ for the various power settings are shown in typical performance characteristics section.

## PACKAGE AND LAYOUT CONSIDERATION

The LMH6678 uses the 24-pin Leadless Leadframe Package, a thermally enhanced, standard size IC package designed to eliminate the use of bulky heatsinks traditionally used in thermal packages. This package can be easily mounted using standard PCB surface mount assembly techniques.

The LLP is designed so that the thermal pad is exposed on the bottom of the IC, as shown in the package drawing. This provides an extremely low thermal resistance ($\theta_{JC}$) path between the die and the exterior of the package. The thermal pad on the bottom of the IC can then be soldered directly to the PCB, using the PCB as a heatsink. In addition, plated-through holes (vias) on the PCB provide a low thermal resistance heat flow path to the backside of the circuit board.

## LAND PATTERN AND ASSEMBLY GUIDELINE FOR LMH6678

1. The thermal pad must be connected to analog ground AGND in LMH6678.
2. Prepare the PCB with a top-side land pattern, as shown in Figure 8.
3. Place the recommended number of plated-through holes in the area of the thermal pad. These holes should be 8 mils max. in diameter. They are kept small so that solder wicking through the holes is not a problem during reflow. The minimum recommended number of holes for the 24-pin LLP is six, as shown in Figure 8.
4. Connect all holes to the internal and bottom analog ground plane.
5. When laying out these holes to the ground plane, do not use the typical web or spoke via connection methodology, as shown in Figure 9. Web connections have a high thermal resistance connection that is useful for slowing the heat transfer during soldering operations. This makes soldering the vias that have ground plane connections easier. However, in this application, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the thermal pad should make their connection to the internal ground plane with a complete connection around the entire circumference of the plated-through hole. Use plated via with solid connection to plane as shown in Figure 10.
6. The top-side solder mask should leave the terminals of the pad connections and the thermal pad area exposed. The thermal pad area should leave the 8 mils holes exposed.
7. Apply solder paste to the exposed thermal pad area and all of the package terminals.
8. With these preparatory steps in place, the LLP is simply placed in position and run through the solder reflow operation as any standard surface-mount component. This results in a part that is properly installed.

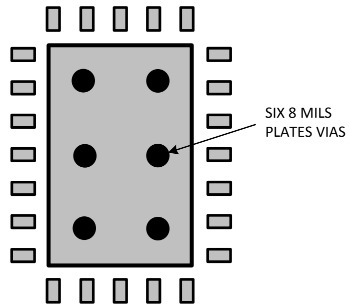



**Figure 8. Recommended Land Pattern**

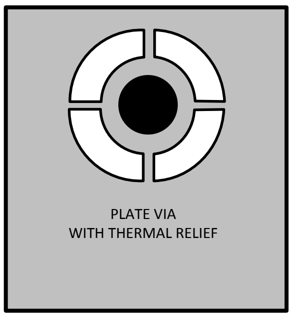



**Figure 9. Via Connection Not Recommended Under the Thermal Pad**

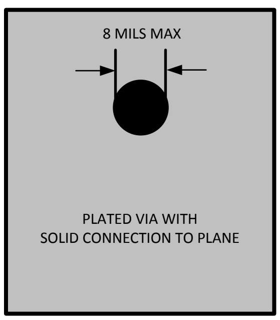



**Figure 10. Via Connection Recommended For Use in Thermal Pad**

## HIGH SPEED DRIVER LAYOUT GUIDELINES

The LMH6678 is a high performance differential line amplifier that requires proper layout for best performance.

- Keep power-supply leads as short as possible. This will keep inductance low and resistive losses at a minimum.
- Proper power-supply bypassing with low ESR capacitors is essential to achieve good performance. A parallel combination of small (around 0.1 μF) ceramic and bigger (6.8 μF) tantalum bypass capacitors will provide low and impedance over a wide frequency rage.
- Bypass capacitor should be placed as close as possible, limited by pick and place machine requirement, to the power-supply pins of the LMH6678 (ceramic cap first and then tantalum cap).
- PCB traces conducting high currents, such as from output to load or from power-supply connector to the power-supply pins of the LMH6678 should be kept as wide and short as possible to minimize inductance and resistive loss.
- The six holes in the landing pattern for the LMH6678 are for the thermal vias that connect the thermal pad of LLP package to the internal/external ground plane on the PCB.

For detail information on the LLP package including thermal modeling considerations and prepared procedures, please see National Semiconductor.

"Applications Note 1187: Leadless Leadframe Package (LLP)" located at www.national.com.

## IMPORTANT NOTICE



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