LME49726 High Current, Low Distortion, Rail-to-Rail Output Audio Operational Amplifier

Check for Samples: LME49726

FEATURES

- **Rail-to-rail output**
- **Easily drives 2kΩ loads to within 4mV of each power supply voltage rail**
- **Optimized for superior audio signal fidelity**
- **Output short circuit protection**
- **High output drive (>300mA)**
- **Available in mini-SOIC exposed-DAP package**

APPLICATIONS

- **Portable audio amplification**
- **Preamplifiers and multimedia**
- **Equalization and crossover networks**
- **Line drivers and receivers**
- **Active filters**
- **DAC I–V converter gain stage**
- **ADC front-end signal conditioning**

DESCRIPTION

The LME49726 is a low distortion, low noise rail-to-rail output audio operational amplifier optimized and fully specified for high performance, high fidelity applications. The LME49726 delivers superior audio signal amplification for outstanding audio performance. The LME49726 has a very low THD+N to easily satisfy demanding audio applications. To ensure that the most challenging loads are driven without compromise, the LME49726 provides output current greater than 300mA at 5V. Further, dynamic range is maximized by an output stage that drives 2kΩ loads to within 4mV of either power supply voltage.

The LME49726 has a supply range of 2.5V to 5.5V. Over this supply range the LME49726's input circuitry maintains excellent common-mode and power supply rejection, as well as maintaining its low input bias current. The LME49726 is unity gain stable.

Table 1. Key Specifications

	VALUE	UNIT
■ Power Supply Voltage Range	2.5 to 5.5	V
■ Quiescent Current per Amplifier at 5V	0.7	mA (typ)
■ THD+N, $A_V = 1$, $f_{IN} = 1kHz$, $R_L = 10k\Omega$ ($V_{OUT} = 3.5V_{P-P}$, $V_{DD} = 5.0V$) ($V_{OUT} = 1.5V_{P-P}$, $V_{DD} = 2.5V$)	0.00008 0.00002	% (typ) % (typ)
■ Equivalent Input Noise (f = 10k)	8.3	nV/√Hz (typ)
■ Slew Rate	±3.7	V/µs (typ)
■ Gain Bandwidth Product	6.25	MHz (typ)
■ Open Loop Gain ($R_L = 10k\Omega$)	120	dB (typ)
■ Input Bias Current	0.2	pA (typ)
■ Input Offset Voltage	0.5	mV (typ)
■ PSRR (DC)	104	dB (typ)

Figure 1. Input Voltage Noise vs Frequency V_{DD} = 3V

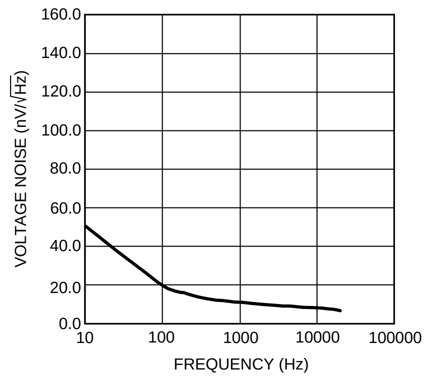
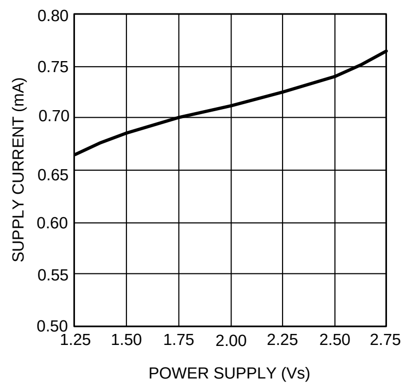


Figure 2. Supply Current vs Supply Voltage per Amplifier, R_L = No Load, A_V = –1



Typical Connections

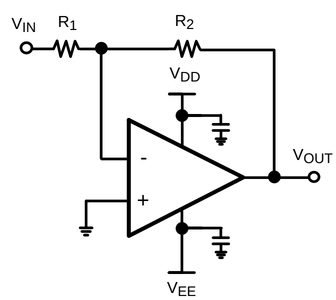


Figure 3. Inverting Configuration Split Supplies

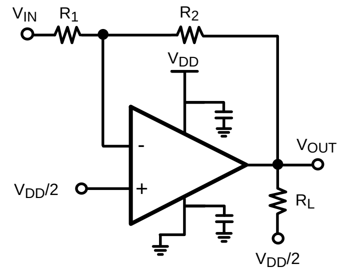


Figure 4. Inverting Configuration Single Supplies

Connection Diagram

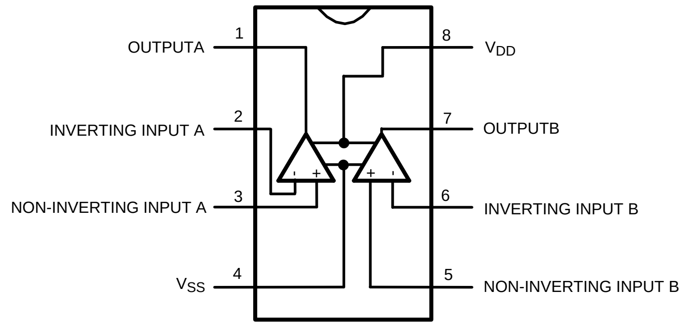


Figure 5. Connection Diagram

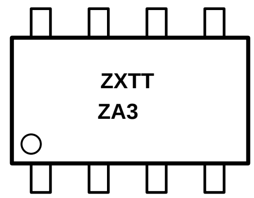


Figure 6. Package Marking

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings [1] [2]

Power Supply Voltage $V_S = V_{SS}$-V_{DD}	6V
Storage Temperature	−65°C to 150°C
Input Voltage	(V_{SS}) – 0.7V to (V_{DD}) + 0.7V
Output Short Circuit (Note 3)	Continuous
Power Dissipation	Internally Limited
ESD Rating (Note 4)	2000V
ESD Rating (Note 5)	200V
Junction Temperature	150°C
Thermal Resistance	
θ_{JA} (MUY-08)	72°C/W

(1) *Absolute Maximum Ratings*" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the *Absolute Maximum Ratings* or other conditions beyond those indicated in the *Recommended Operating Conditions* is not implied. The *Recommended Operating Conditions* indicate conditions at which the device is functional and the device should not be operated beyond such conditions. All voltages are measured with respect to the ground pin, unless otherwise specified.

(2) The *Electrical Characteristics* tables list guaranteed specifications under the listed *Recommended Operating Conditions* except as otherwise modified or specified by the *Electrical Characteristics Conditions* and/or Notes. Typical specifications are estimations only and are not guaranteed.

Operating Ratings [1]

Temperature Range	
$T_{MIN} \leq T_A \leq T_{MAX}$	$-40°C \leq T_A \leq 125°C$
Supply Voltage Range	$2.5V \leq V_S \leq 5.5V$

(1) *Absolute Maximum Ratings*" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the *Absolute Maximum Ratings* or other conditions beyond those indicated in the *Recommended Operating Conditions* is not implied. The *Recommended Operating Conditions* indicate conditions at which the device is functional and the device should not be operated beyond such conditions. All voltages are measured with respect to the ground pin, unless otherwise specified.

Electrical Characteristics (V_{DD} = 5.0V and V_{DD} = 2.5V)

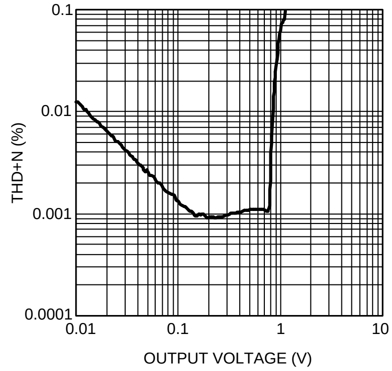
The following specifications apply for the circuit shown in Figure 1. V_{DD} = 5.0V and V_{DD} = 2.5V, V_{SS} = 0.0V, V_{CM} = $V_{DD/2}$, R_L = 10kΩ, C_{LOAD} = 20pF, f_{IN} = 1kHz, BW = 20–20kHz, and T_A = 25°C, unless otherwise specified.

Symbol	Parameter	Conditions	LME49726 Typical (1)	LME49726 Limit (2)	Units (Limits)
THD+N	Total Harmonic Distortion + Noise	A_V = –1, V_{OUT} = 3.5V_{p-p}, V_{DD} = 5V R_L = 600Ω R_L = 2kΩ R_L = 10kΩ	 0.0008 0.0002 0.00008		 % % %
		A_V = –1, V_{OUT} = 1.5V_{p-p}, V_{DD} = 2.5V R_L = 600Ω R_L = 2kΩ R_L = 10kΩ	 0.001 0.0008 0.0002		 % % %
GBWP	Gain Bandwidth Product		6.25	5.0	MHz (min)
SR	Slew Rate	A_V = +1, R_L = 10kΩ	3.7	2.5	V/μs (min)
t_s	Settling time	A_V = 1V step 0.1% error range 0.001% error range	 800 1.2		 ns μs
e_N	Equivalent Input Noise Voltage	f_{BW} = 20Hz to 20kHz (A-weighted)	0.7	1.25	$μV_{RMS}$ (max)
e_N	Equivalent Input Noise Density	f = 10kHz	8.3		nV/√Hz
		f = 1kHz	10		nV/√Hz
		f = 100Hz	24		nV/√Hz
I_N	Current Noise Density	f = 1kHz	0.75		pA/√Hz
V_{OS}	Input Offset Voltage	V_{IN} = $V_{DD/2}$, V_O = $V_{DD/2}$, A_V = 1	0.5	2.25	mV (max)
$ΔV_{OS}$/ΔTemp	Average Input Offset Voltage Drift vs Temperature	40°C ≤ T_A ≤ 85°C	1.2		μV/°C
PSRR	Power Supply Rejection Ratio	2.5 to 5.5V, V_{CM} = 0, V_{DD}/2	104	85	dB (min)
ISO_{CH-CH}	Channel-to-Channel Isolation	f_{IN} = 1kHz	94		dB
I_B	Input Bias Current	V_{CM} = V_{DD}/2	±0.2		pA
$ΔI_{OS}$/ΔTemp	Input Bias Current Drift vs Temperature	–40°C ≤ T_A ≤ 85°C	35		nA/°C
I_{OS}	Input Offset Current	V_{CM} = V_{DD}/2	±0.2		pA
V_{IN-CM}	Common-Mode Input Voltage Range			V_{DD}–1.6 V_{SS}+0.1	V (min)
CMRR	Common Mode Rejection Ratio	0.1V < V_{DD} – 1.6V	95	80	dB (min)
1/f	1/f Corner Frequency		2		kHz
A_{VOL}	Open-Loop Voltage Gain	V_{OUT} = V_{DD}/2	120	100	dB (min)
$V_{OUTSWING}$	Maximum Output Voltage Swing	R_L = 2kΩ to V_{DD}/2	V_{DD}–0.004 V_{SS} +0.004		V (min) V (max)
		R_L = 16Ω to V_{DD}/2	V_{DD} –0.33 V_{SS}+0.33		V (min) V (max)
I_{OUT}	Output Current	V_{OUT} = 5V, V_{DD} = 5V	350		mA
		V_{OUT} = 2.5V, V_{DD} = 2.5V	160		mA
I_S	Quiescent Current per Amplifier	I_{OUT} = 0mA, V_{DD} = 5V	0.7	1.1	mA (max)
		I_{OUT} = 0mA, V_{DD} = 2.5V	0.64	1.0	mA (max)

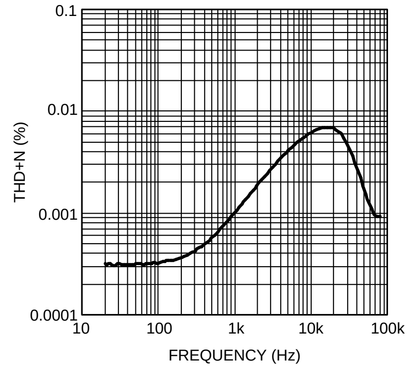
(1) Typical values represent most likely parametric norms at T_A = +25ºC, and at the *Recommended Operation Conditions* at the time of product characterization and are not guaranteed.
(2) Datasheet min/max specification limits are guaranteed by test or statistical analysis.

Typical Performance Characteristics

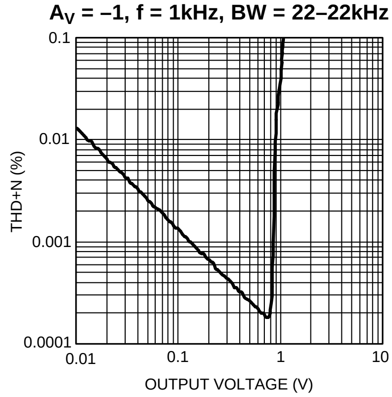
THD+N vs Output Voltage
V_{DD} = 1.25V, V_{SS} = –1.25V, R_L = 600Ω
A_V = –1, f = 1kHz, BW = 22–22kHz



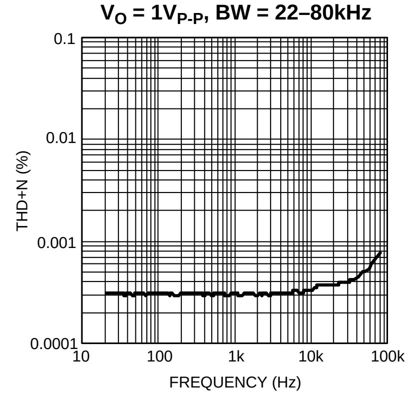
THD+N vs Frequency
V_{DD} = 1.25V, V_{SS} = –1.25V, R_L = 600Ω
V_O = 1.5V_{P-P}, BW = 22–80kHz



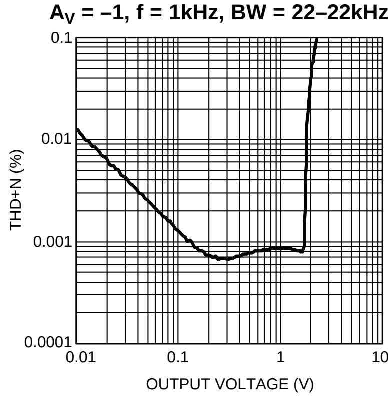
THD+N vs Output Voltage
V_{DD} = 1.25V, V_{SS} = –1.25V, R_L = 10kΩ
A_V = –1, f = 1kHz, BW = 22–22kHz



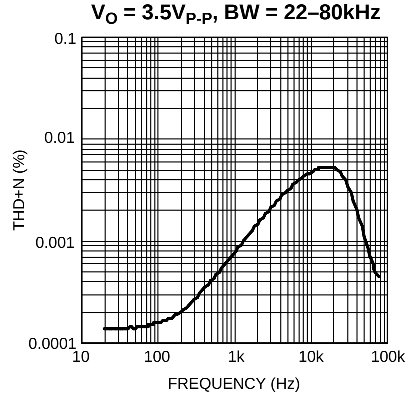
THD+N vs Frequency
V_{DD} = 1.25V, V_{SS} = –1.25V, R_L = 10kΩ
V_O = 1V_{P-P}, BW = 22–80kHz



THD+N vs Output Voltage
V_{DD} = 2.50V, V_{SS} = –2.50V, R_L = 600Ω
A_V = –1, f = 1kHz, BW = 22–22kHz

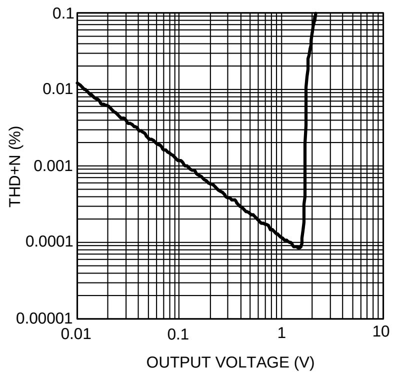


THD+N vs Frequency
V_{DD} = 2.50V, V_{SS} = –2.50V, R_L = 600Ω
V_O = 3.5V_{P-P}, BW = 22–80kHz

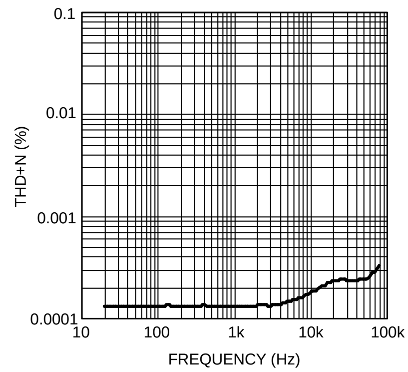


Typical Performance Characteristics (continued)

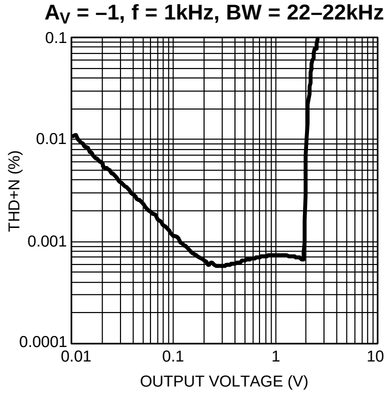
THD+N vs Output Voltage
V_{DD} = 2.50V, V_{SS} = –2.50V, R_L = 10kΩ
A_V = –1, f = 1kHz, BW = 22–22kHz



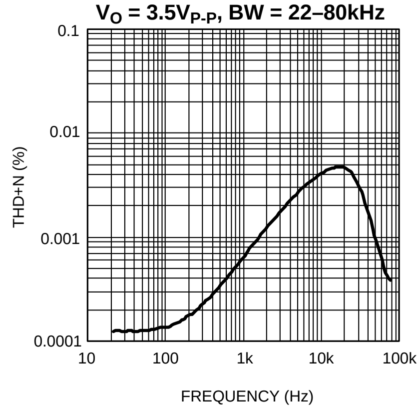
THD+N vs Frequency
V_{DD} = 2.50V, V_{SS} = –2.50V, R_L = 10kΩ
V_O = 1V_{P-P}, BW = 22–80kHz



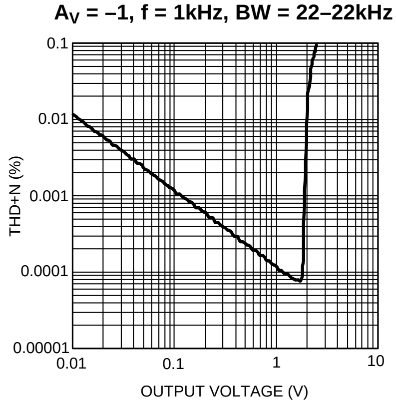
THD+N vs Output Voltage
V_{DD} = 2.75V, V_{SS} = –2.75V, R_L = 600Ω
A_V = –1, f = 1kHz, BW = 22–22kHz



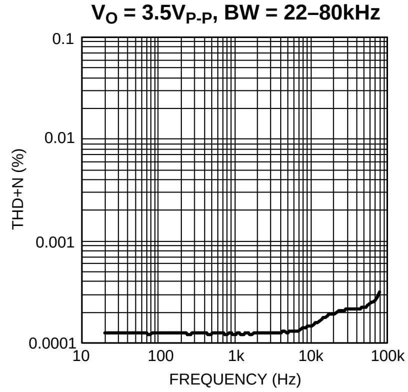
THD+N vs Frequency
V_{DD} = 2.75V, V_{SS} = –2.75V, R_L = 600Ω
V_O = 3.5V_{P-P}, BW = 22–80kHz



THD+N vs Output Voltage
V_{DD} = 2.75V, V_{SS} = –2.75V, R_L = 10kΩ
A_V = –1, f = 1kHz, BW = 22–22kHz

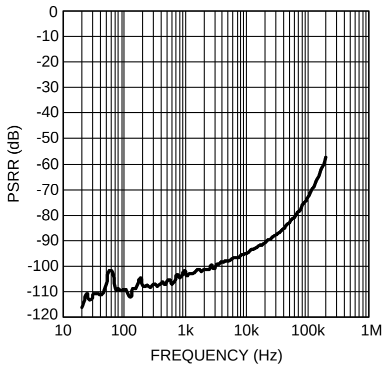


THD+N vs Frequency
V_{DD} = 2.75V, V_{SS} = –2.75V, R_L = 10kΩ
V_O = 3.5V_{P-P}, BW = 22–80kHz

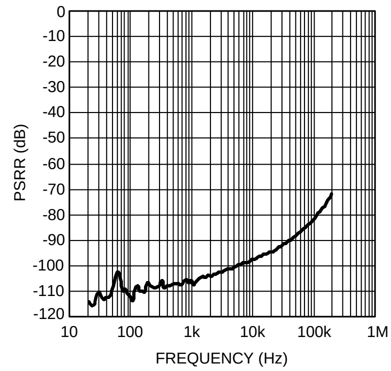


Typical Performance Characteristics (continued)

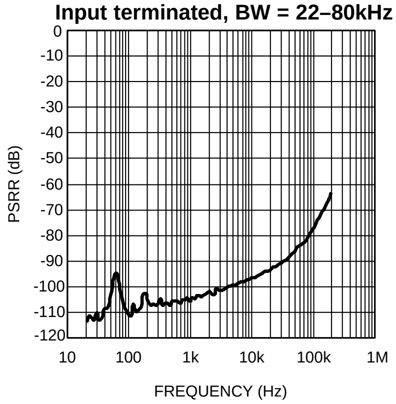
PSRR+ vs Frequency
V_{DD} = 1.25V, V_{SS} = –1.25V, V_{RIPPLE} = 200mV_{P-P}
Input terminated, BW = 22–80kHz



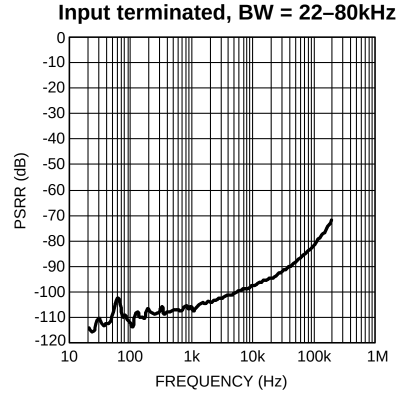
PSRR– vs Frequency
V_{DD} = 1.25V, V_{SS} = –1.25V, V_{RIPPLE} = 200mV_{P-P}
Input terminated, BW = 22–80kHz



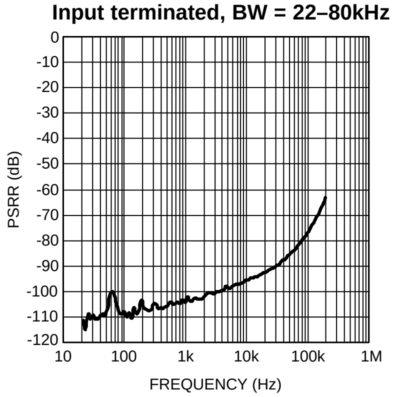
PSRR+ vs Frequency
V_{DD} = 2.50V, V_{EE} = –2.50V, V_{RIPPLE} = 200mV_{P-P}
Input terminated, BW = 22–80kHz



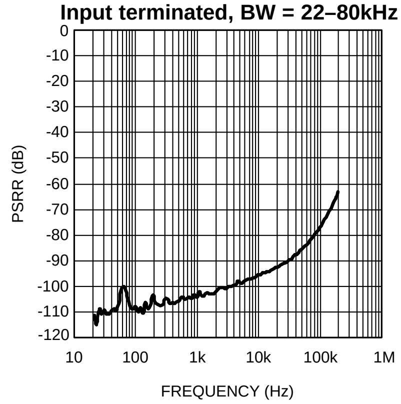
PSRR– vs Frequency
V_{DD} = 2.50V, V_{SS} = –2.50V, V_{RIPPLE} = 200mV_{P-P}
Input terminated, BW = 22–80kHz



PSRR+ vs Frequency
V_{DD} = 2.75V, V_{SS} = –2.75V, V_{RIPPLE} = 200mV_{P-P}
Input terminated, BW = 22–80kHz

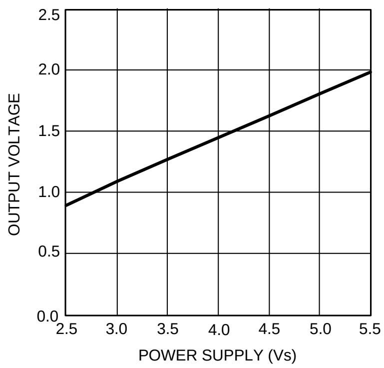


PSRR– vs Frequency
V_{DD} = 2.75V, V_{SS} = –2.75V, V_{RIPPLE} = 200mV_{P-P}
Input terminated, BW = 22–80kHz

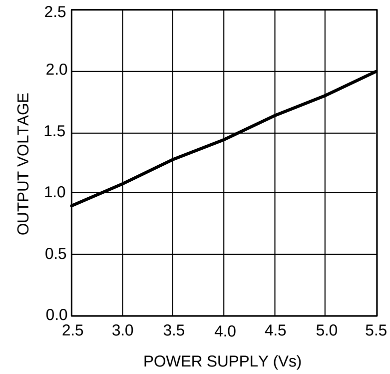


Typical Performance Characteristics (continued)

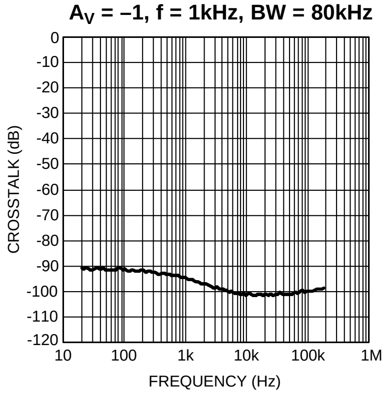
Output Voltage vs Supply Voltage
R_L = 600Ω, A_V = –1
f = 1kHz, THD+N = 1%, BW = 22–80kHz



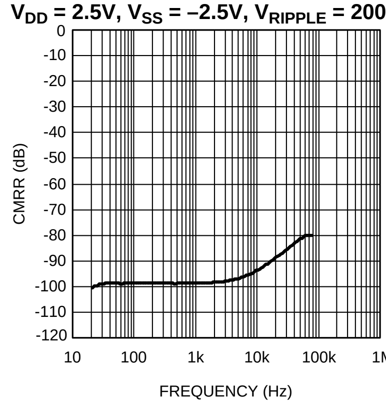
Output Voltage vs Supply Voltage
R_L = 10kΩ, A_V = –1
f = 1kHz, THD+N = 1%, BW = 22–80kHz



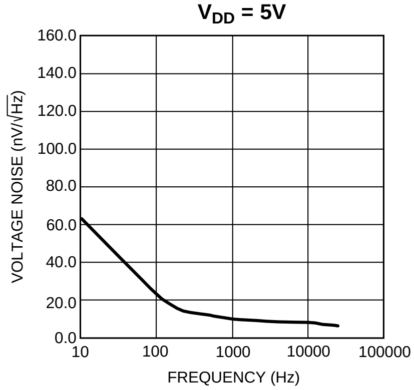
Crosstalk vs Frequency
V_{DD} = 2.50V, V_{SS} = –2.50V, R_L = 10kΩ
A_V = –1, f = 1kHz, BW = 80kHz



CMRR vs Frequency
V_{DD} = 2.5V, V_{SS} = –2.5V, V_{RIPPLE} = 200mV_{P-P}



Input Voltage Noise vs Frequency
V_{DD} = 5V



Application Information

DISTORTION MEASUREMENTS

The vanishingly low residual distortion produced by LME49726 is below the capabilities of all commercially available equipment. This makes distortion measurements just slightly more difficult than simply connecting a distortion meter to the amplifier's inputs and outputs. The solution. however, is quite simple: an additional resistor. Adding this resistor extends the resolution of the distortion measurement equipment.

The LME49726's low residual is an input referred internal error. As shown in Figure 7, adding the 10Ω resistor connected between athe amplifier's inverting and non-inverting inputs changes the amplifier's noise gain. The result is that the error signal (distortion) is amplified by a factor of 101. Although the amplifier's closed-loop gain is unaltered, the feedback available to correct distortion errors is reduced by 101. To ensure minimum effects on distortion measurements, keep the value of R1 low as shown in Figure 7.

This technique is verified by duplicating the measurements with high closed loop gain and/or making the measurements at high frequencies. Doing so, produces distortion components that are within measurement equipment capabilities. This datasheet's THD+N and IMD values were generated using the above described circuit connected to an Audio Precision System Two Cascade.

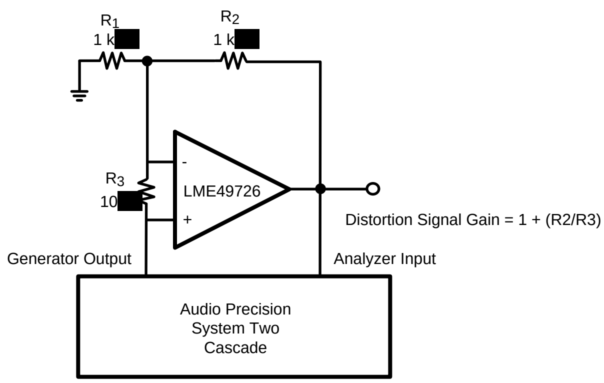


Figure 7. THD+N and IMD Distortion Test Circuit

OPERATING RATINGS AND BASIC DESIGN GUIDELINES

The LME49726 has a supply voltage range from +2.5V to +5.5V single supply or ±1.25 to ±2.75V dual supply.

Bypassed capacitors for the supplies should be placed as close to the amplifier as possible. This will help minimize any inductance between the power supply and the supply pins. In addition to a 10μF capacitor, a 0.1μF capacitor is also recommended in CMOS amplifiers.

The amplifier's inputs lead lengths should also be as short as possible. If the op amp does not have a bypass capacitor, it may oscillate.

BASIC AMPLIFIER CONFIGURATIONS

The LME49726 may be operated with either a single supply or dual supplies. Figure 2 shows the typical connection for a single supply inverting amplifier. The output voltage for a single supply amplifier will be centered around the common-mode voltage, V_{CM}. Note, the voltage applied to the V_{CM} insures the output stays above ground. Typically, the V_{CM} should be equal to $V_{DD}/2$. This is done by putting a resistor divider circuit at this node, see Figure 8.

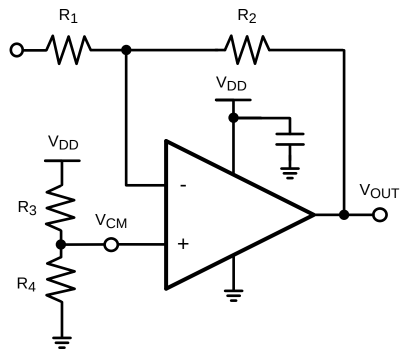


Figure 8. Single Supply Inverting Op Amp

Figure 9 shows the typical connection for a dual supply inverting amplifier. The output voltage is centered on zero.

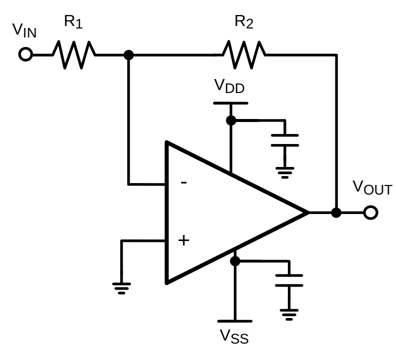


Figure 9. Dual Supply Inverting Configuration

Figure 10 shows the typical connection for the Buffer Amplifier or also called a Voltage Follower. The Buffer is a unity gain stable amplifier.

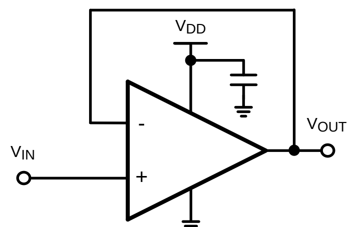
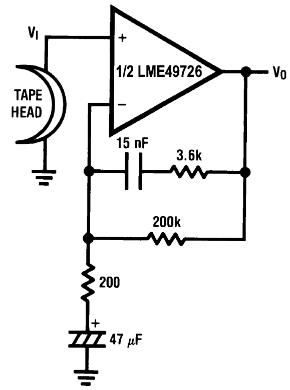


Figure 10. Unity-Gain Buffer Configuration

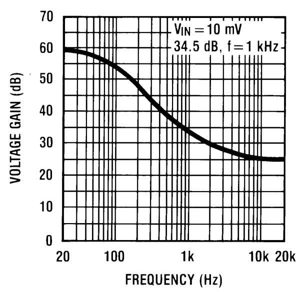
Typical Applications

Figure 11. NAB Preamp



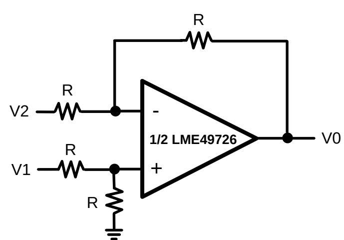
A_V = 34.5
F = 1 kHz
E_n = 0.38 μV
A Weighted

Figure 12. NAB Preamp Voltage Gain vs Frequency



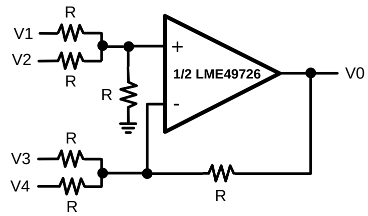
A_V = 34.5
F = 1 kHz
E_n = 0.38 μV
A Weighted

Figure 13. Balanced to Single Ended Converter



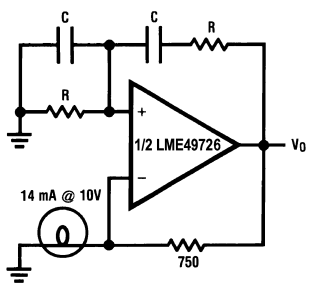
V_O = V1–V2

Figure 14. Adder/Subtracter



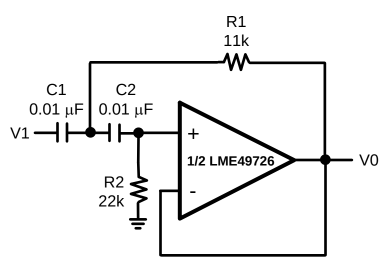
$V_O = V1 + V2 - V3 - V4$

Figure 15. Sine Wave Oscillator



$$f_o = \frac{1}{2\pi RC}$$

Figure 16. Second Order High Pass Filter (Butterworth)



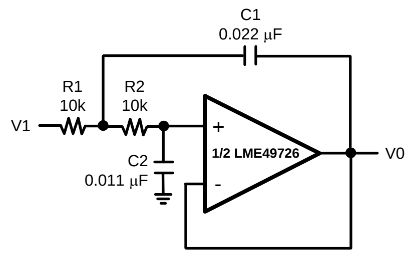
if $C1 = C2 = C$

$$R1 = \frac{\sqrt{2}}{2\omega_o C}$$

$R2 = 2 \bullet R1$

Illustration is $f_0 = 1$ kHz

Figure 17. Second Order Low Pass Filter (Butterworth)



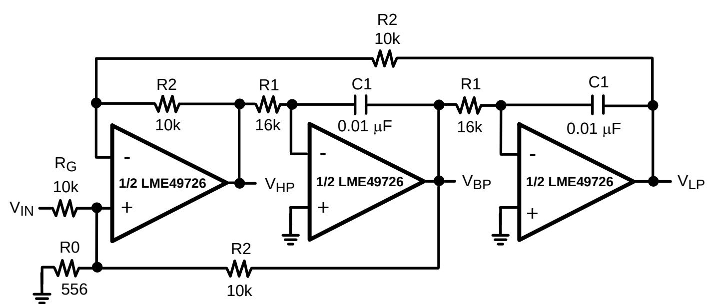
$\text{if } R1 = R2 = R$

$C1 = \frac{\sqrt{2}}{\omega_o R}$

$C2 = \frac{C1}{2}$

Illustration is f_0 = 1 kHz

Figure 18. State Variable Filter



$f_0 = \frac{1}{2\pi C1R1}, Q = \frac{1}{2}\left(1 + \frac{R2}{R0} + \frac{R2}{RG}\right), A_{BP} = QA_{LP} = QA_{LH} = \frac{R2}{RG}$

Illustration is f_0 = 1 kHz, Q = 10, A_{BP} = 1

Figure 19. AC/DC Converter

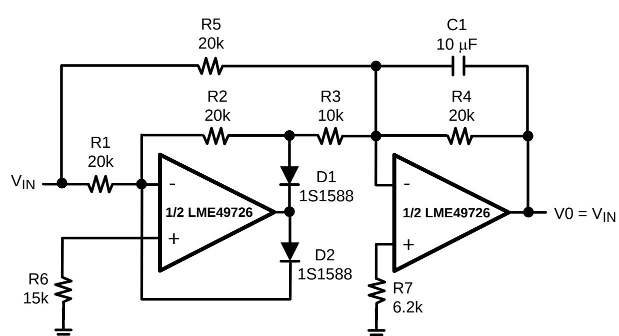


Figure 20. 2 Channel Panning Circuit (Pan Pot)

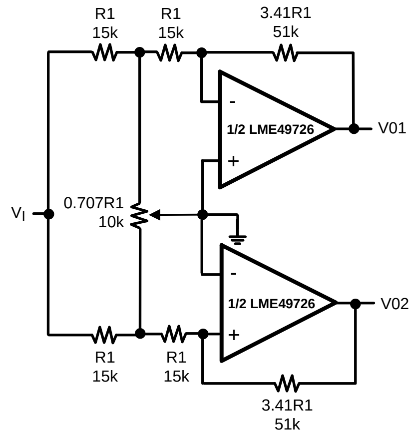


Figure 21. Line Driver

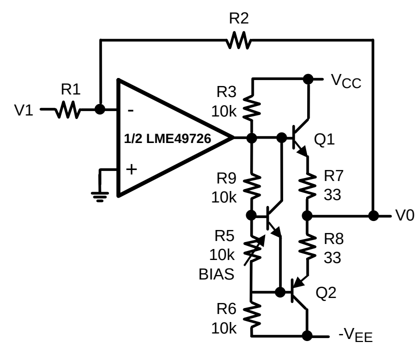
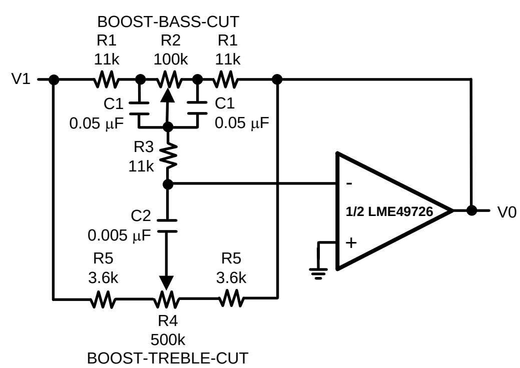


Figure 22. Tone Control



$f_L = \frac{1}{2\pi R2C1}, f_{LB} = \frac{1}{2\pi R1C1}$

$f_H = \frac{1}{2\pi R5C2}, f_{HB} = \frac{1}{2\pi (R1 + R5 + 2R3)C2}$

Illustration is:

f_L = 32 Hz, f_{LB} = 320 Hz

f_H =11 kHz, f_{HB} = 1.1 kHz

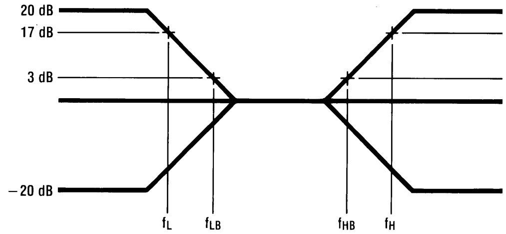
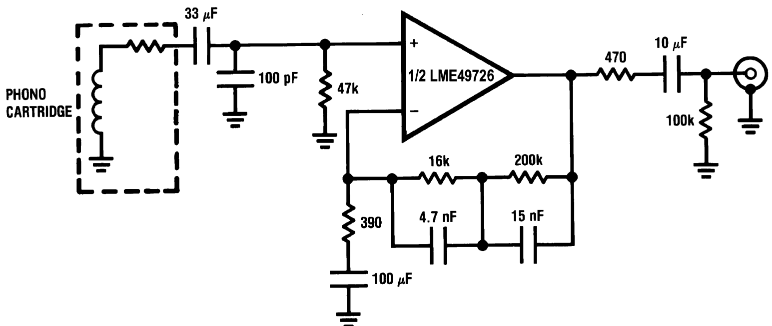
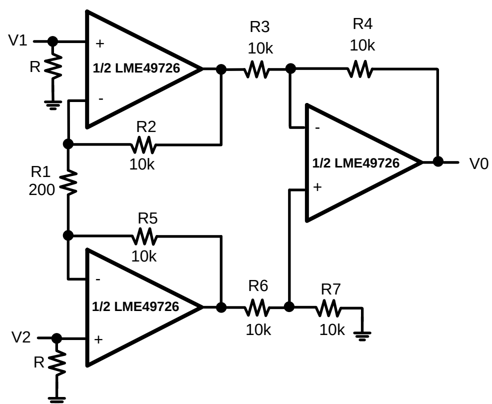


Figure 23. RIAA Preamp



A_v = 35 dB
E_n = 0.33 μV
S/N = 90 dB
f = 1 kHz
A Weighted
A Weighted, V_{IN} = 10 mV
@f = 1 kHz

Figure 24. Balanced Input Mic Amp

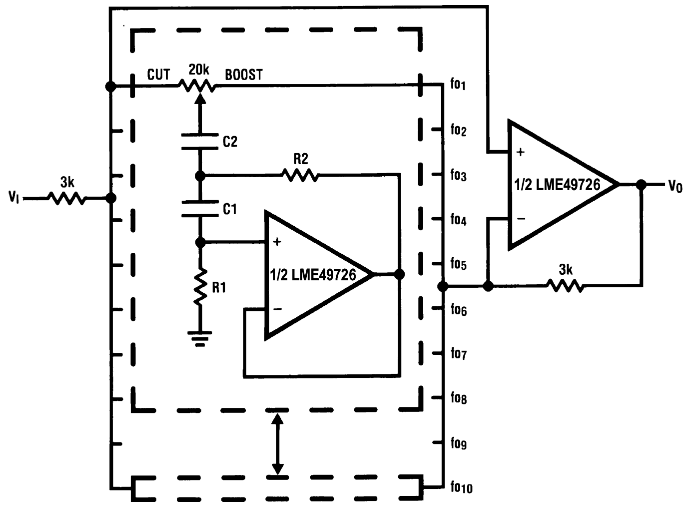


If R2 = R5, R3 = R6, R4 = R7

$$V0 = \left(1 + \frac{2R2}{R1}\right)\frac{R4}{R3}(V2 - V1)$$

Illustration is:
V0 = 101(V2 − V1)

Figure 25. 10 Band Graphic Equalizer

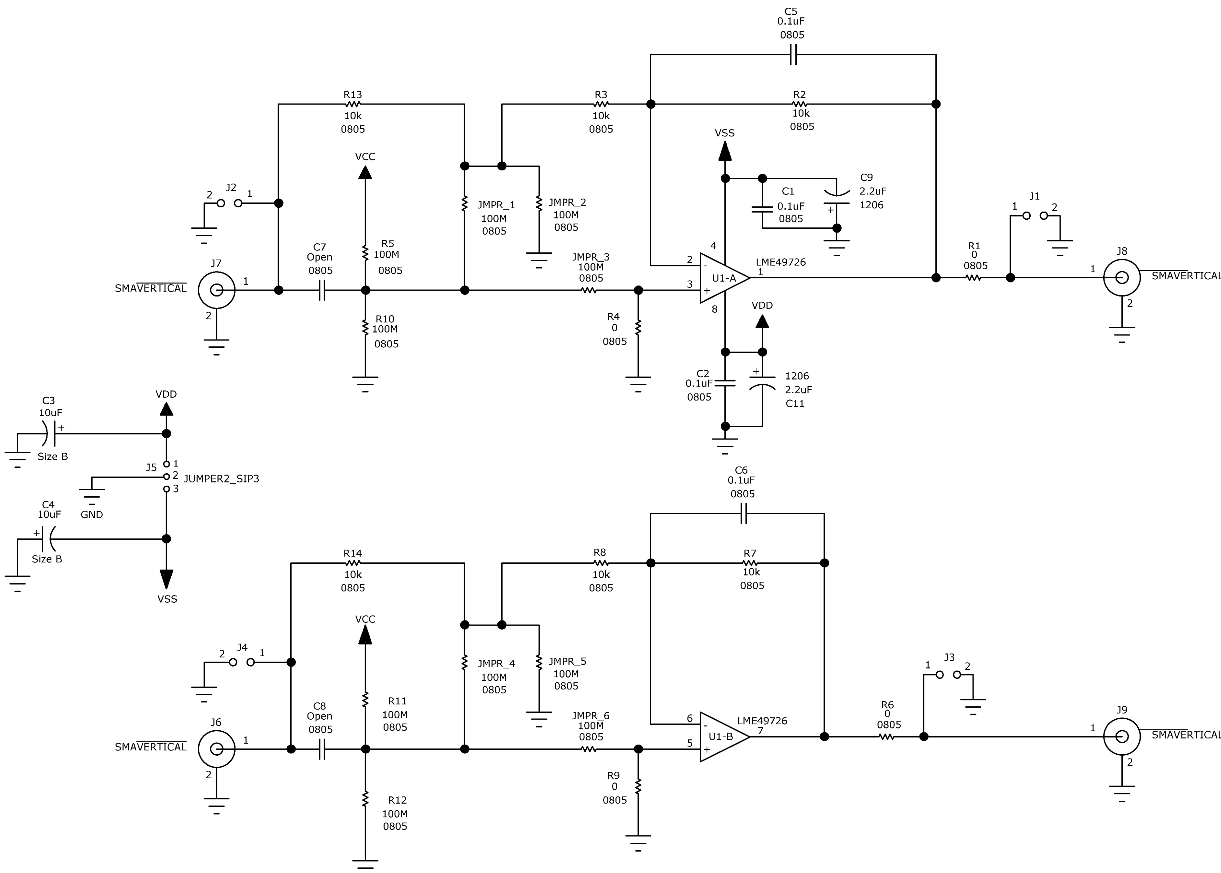


fo (Hz)	C_1	C_2	R_1	R_2
32	0.12µF	4.7µF	75kΩ	500Ω
64	0.056µF	3.3µF	68kΩ	510Ω
125	0.033µF	1.5µF	62kΩ	510Ω
250	0.015µF	0.82µF	68kΩ	470Ω
500	8200pF	0.39µF	62kΩ	470Ω
1k	3900pF	0.22µF	68kΩ	470Ω
2k	2000pF	0.1µF	68kΩ	470Ω
4k	1100pF	0.056µF	62kΩ	470Ω
8k	510pF	0.022µF	68kΩ	510Ω
16k	330pF	0.012µF	51kΩ	510Ω

LME49726 Bill of Materials

Description	Designator	Part Number	Manufacturer	Quantity/Brd
Ceramic Capacitor 0.1uF, 10%, 50V 0805 SMD	C1, C2, C5–C8	08055C104KAT2A	AVX	2
Tantalum Capacitor 2.2uF,10%, 20V, A-size	C9, C11	T491A225K020AT	Kemet	Not Stuff
Tantalum Capacitor 10uF,10%, 20V, B-size	C3, C4	T491B106K020AT	Kemet	2
Resistor 0Ω, 1/8W 1% 0805 SMD	R1, R4, R6, R9, R13, R14	CRCW08050000Z0EA	Vishay	6
Header, 2-Pin	JP1, JP2, JP3, JP4	HDR1X2	Header 2	4
Header, 3-Pin	JP5	HDR1X3	Header 3	1
Resistor 10kΩ, 1/8W 1% 0805 SMD	R2, R3, R7, R8	CRCW080510K0FKEA	Vishay	4
Dual Rail-to-Rail Op Amp	U1	LME49726	National Semiconductor	1
Resistor 100meg/open 1/8W 0805 SMD	R5, R10, R11, R12	OPEN N/A	N/A	0

LME49726 Board Circuit



LME49726 Demo Board Views

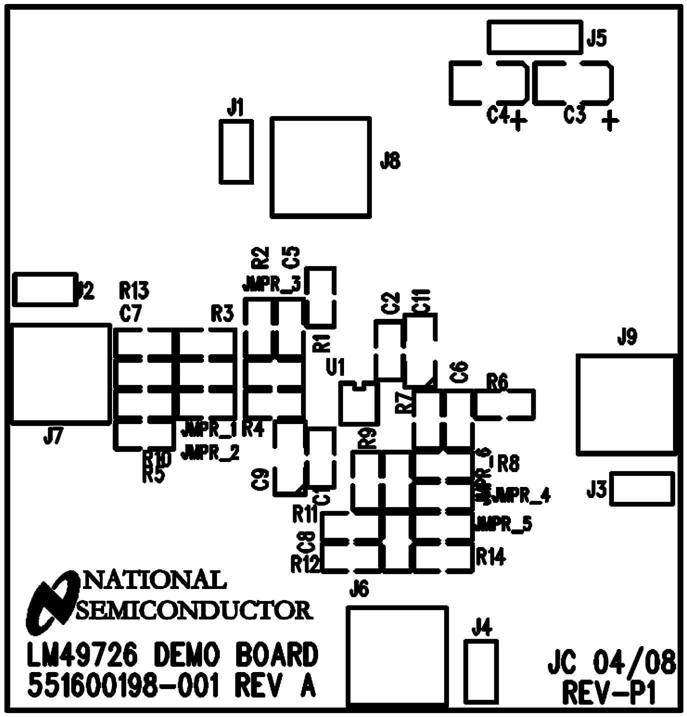


Figure 26. Top Silkscreen

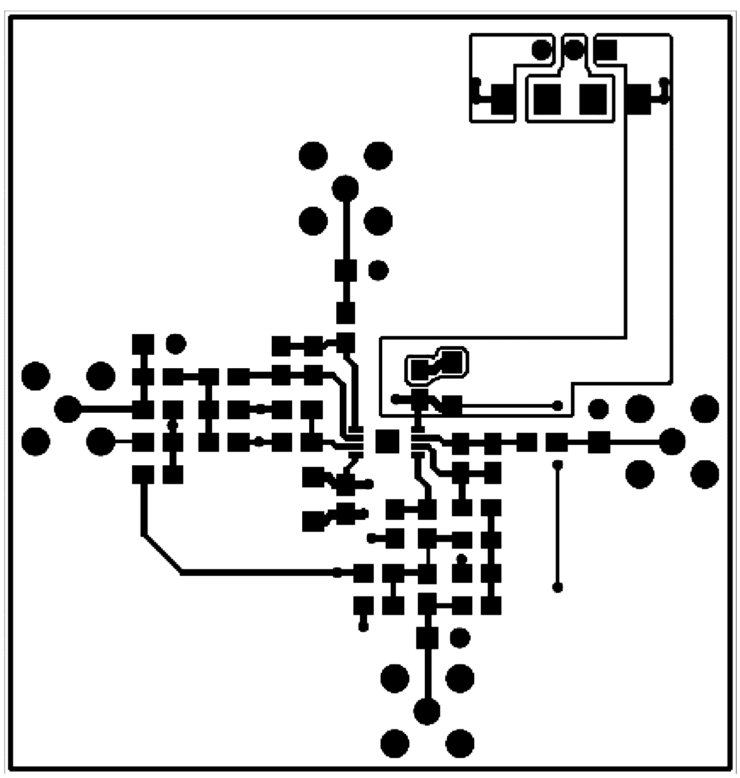


Figure 27. Top Layer

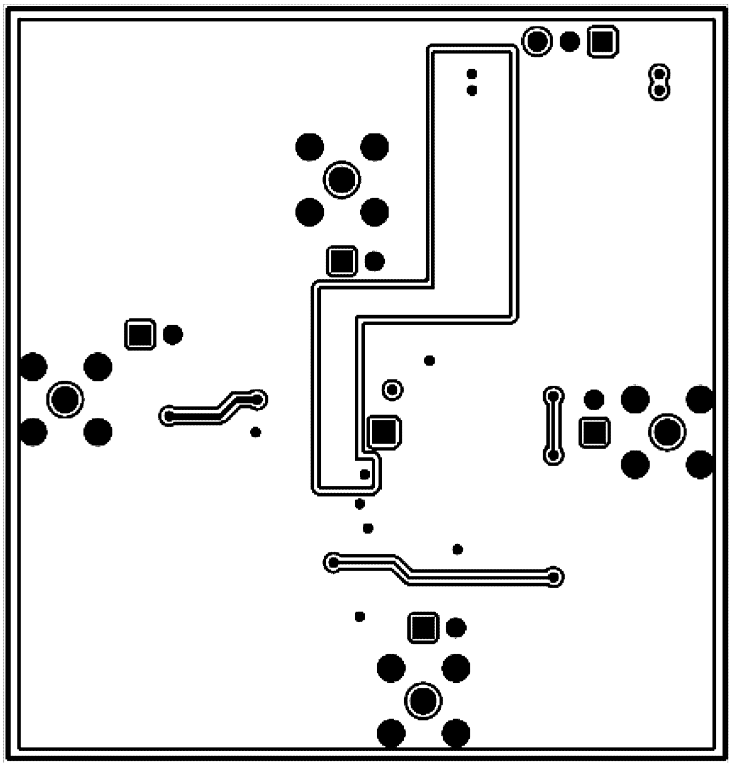


Figure 28. Bottom Layer

Revision History

Rev	Date	Description
1.0	11/05/08	Initial release.
1.01	05/25/10	Increased Operating Temperature Range.
1.02	07/14/11	Added curves 30038602 and 03 and input text edits.
1.03	07/19/11	Re-released the D/S to the WEB after adding curves 30038602 and 03 .

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LME49726MY/NOPB	ACTIVE	MSOP-PowerPAD	DGN	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	ZA3	Samples
LME49726MYX/NOPB	ACTIVE	MSOP-PowerPAD	DGN	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	ZA3	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

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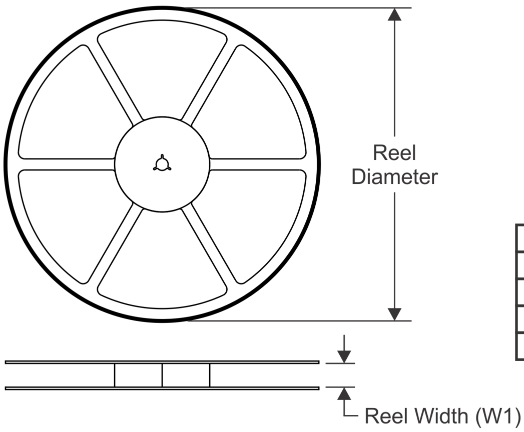
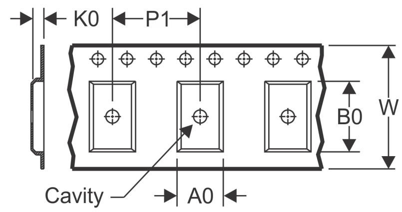
TAPE AND REEL INFORMATION

REEL DIMENSIONS

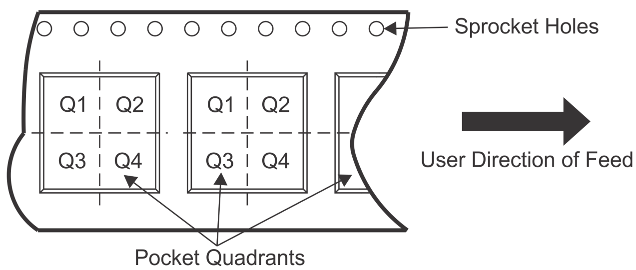


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

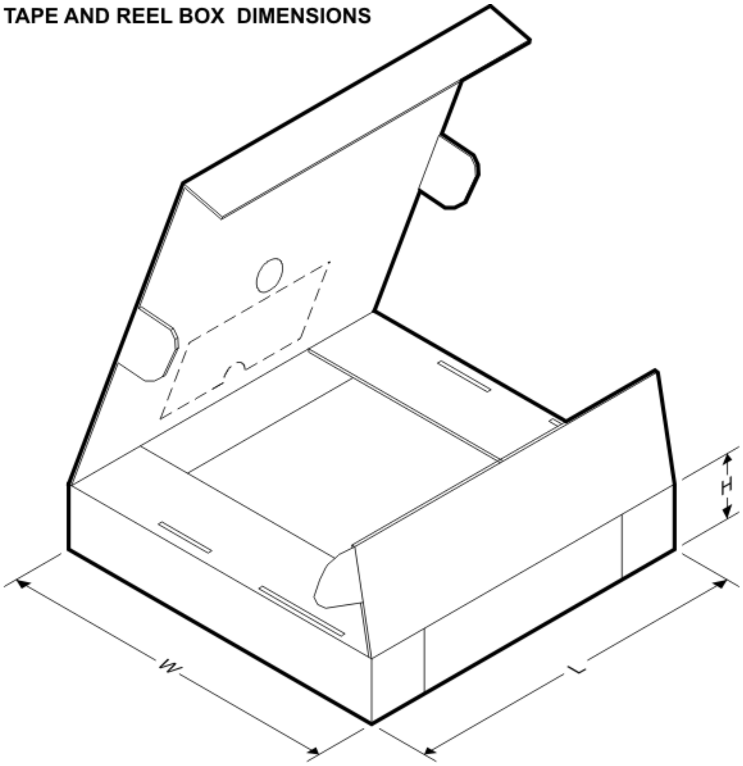
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LME49726MY/NOPB	MSOP-Power PAD	DGN	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LME49726MYX/NOPB	MSOP-Power PAD	DGN	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

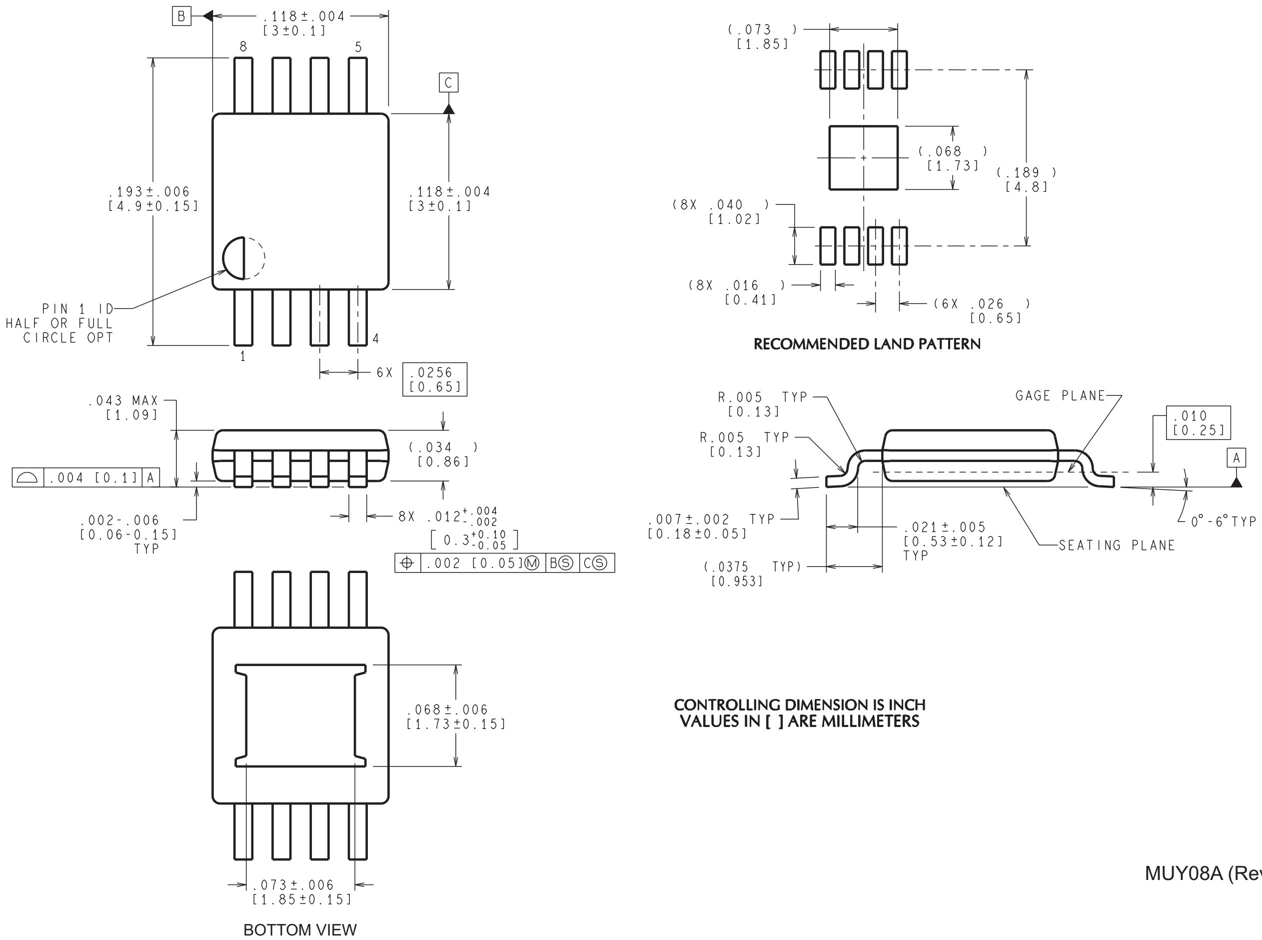
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LME49726MY/NOPB	MSOP-PowerPAD	DGN	8	1000	203.0	190.0	41.0
LME49726MYX/NOPB	MSOP-PowerPAD	DGN	8	3500	349.0	337.0	45.0

DGN0008A



MUY08A (Rev A)

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