National Semiconductor

LM6161/LM6261/LM6361 High Speed Operational Amplifier

General Description

The LM6161 family of high-speed amplifiers exhibits an excellent speed-power product in delivering 300 V/μs and 50 MHz unity gain stability with only 5 mA of supply current. Further power savings and application convenience are possible by taking advantage of the wide dynamic range in operating supply voltage which extends all the way down to +5V.

These amplifiers are built with National's VIP™ (Vertically Integrated PNP) process which provides fast PNP transistors that are true complements to the already fast NPN devices. This advanced junction-isolated process delivers high speed performance without the need for complex and expensive dielectric isolation.

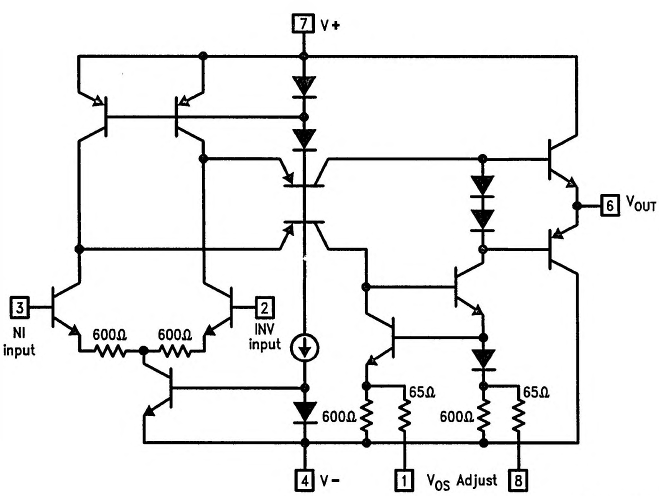
Features

- High slew rate — 300 V/μs
- High unity gain freq — 50 MHz
- Low supply current — 5 mA
- Fast settling — 120 ns to 0.1%
- Low differential gain — <0.1%
- Low differential phase — 0.1°
- Wide supply range — 4.75V to 32V
- Stable with unlimited capacitive load
- Well behaved; easy to apply

Applications

- Video amplifier
- High-frequency filter
- Wide-bandwidth signal conditioning

Simplified Schematic



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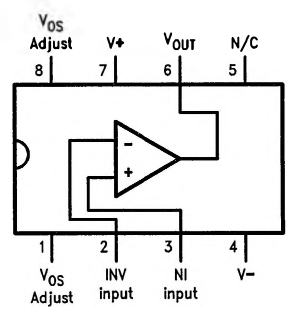
Connection Diagram



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Order Number LM6161J or LM6261J
See NS Package Number J08A

Order Number LM6261N or LM6361N
See NS Package Number N08E

Order Number LM6361M
See NS Package Number M08A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ($V^+ - V^-$)	36V
Differential Input Voltage (Note 8)	±8V
Common-Mode Voltage Range (Note 12)	(V^+ − 0.7V) to (V^- − 7V)
Output Short Circuit to GND (Note 1)	Continuous
Soldering Information	
Dual-In-Line Package (N, J)	
Soldering (10 sec.)	260°C
Small Outline Package (M)	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Storage Temp Range	−65°C to +150°C
Max Junction Temperature	150°C
ESD Tolerance (Notes 8 and 9)	±700V

Operating Ratings

Temperature Range (Note 2)	
LM6161	$-55°C \leq T_J \leq +125°C$
LM6261	$-25°C \leq T_J \leq +85°C$
LM6361	$0°C \leq T_J \leq +70°C$
Supply Voltage Range	4.75V to 32V

DC Electrical Characteristics (Note 3)

Parameter	Conditions	Typ	LM6161 Tested Limit (Note 4)	LM6161 Design Limit (Note 5)	LM6261 Tested Limit (Note 4)	LM6261 Design Limit (Note 5)	LM6361 Tested Limit (Note 4)	LM6361 Design Limit (Note 5)	Units
Input Offset Voltage		5	7 **10**		7	**9**	20	**22**	mV max
Input Offset Voltage Average Drift		10							μV/°C
Input Bias Current		2	3 **6**		3	**5**	5	**6**	μA max
Input Offset Current		150	350 **800**		350	**600**	1500	**1900**	nA max
Input Offset Current Average Drift		0.4							nA/°C
Input Resistance	Differential	325							kΩ
Input Capacitance	Av = +1 @ 10 MHz	1.5							pF
Large Signal Voltage Gain	V_{OUT} = ±10V, R_L = 2 kΩ (Note 11)	750	550 **300**		550	**400**	400	**350**	V/V min
	R_L = 10 kΩ	2900							V/V
Input Common-Mode Voltage Range	Supply = ±15V	+14.0	+13.9 **+13.8**		+13.9	**+13.8**	+13.8	**+13.7**	Volts min
		−13.2	−12.9 **−12.7**		−12.9	**−12.7**	−12.8	**−12.7**	Volts min
	Supply = +5V (Note 6)	4.0	3.9 **3.8**		3.9	**3.8**	3.8	**3.7**	Volts min
		1.8	2.0 **2.2**		2.0	**2.2**	2.1	**2.2**	Volts max
Common-Mode Rejection Ratio	$-10V \leq V_{CM} \leq +10V$	94	80 **74**		80	**76**	72	**70**	dB min
Power Supply Rejection Ratio	$\pm 10V \leq V\pm \leq \pm 16V$	90	80 **74**		80	**76**	72	**70**	dB min

DC Electrical Characteristics (Note 3) (Continued)

Parameter	Conditions	Typ	LM6161		LM6261		LM6361		Units
			Tested Limit (Note 4)	Design Limit (Note 5)	Tested Limit (Note 4)	Design Limit (Note 5)	Tested Limit (Note 4)	Design Limit (Note 5)	
Output Voltage Swing	Supply = ±15V and R_L = 2 kΩ	+14.2	+13.5 **+13.3**		+13.5	**+13.3**	+13.4	**+13.3**	Volts min
		−13.4	−13.0 **−12.7**		−13.0	**−12.8**	−12.9	**−12.8**	Volts min
	Supply = +5V and R_L = 2 kΩ (Note 6)	4.2	3.5 **3.3**		3.5	**3.3**	3.4	**3.3**	Volts min
		1.3	1.7 **2.0**		1.7	**1.9**	1.8	**1.9**	Volts max
Output Short Circuit Current	Souce	65	30 **20**		30	**25**	30	**25**	mA min
	Sink	65	30 **20**		30	**25**	30	**25**	mA min
Supply Current		5.0	6.5 **6.8**		6.5	**6.7**	6.8	**6.9**	mA max

AC Electrical Characteristics (Notes 3 & 7)

Parameter	Conditions	Typ	LM6161		LM6261		LM6361		Units
			Tested Limit (Note 4)	Design Limit (Note 5)	Tested Limit (Note 4)	Design Limit (Note 5)	Tested Limit (Note 4)	Design Limit (Note 5)	
Gain-Bandwidth Product	@ F = 20 MHz	50	40 **30**		40	**35**	35	**32**	MHz min
	Supply = ±5V	35							MHz
Slew Rate	Av = +1 (Note 10)	300	200 **180**		200	**180**	200	**180**	V/μs min
	Supply = ±5V	200							V/μs
Power Bandwidth	V_{OUT} = 20 V_{pp}	4.5							MHz
Settling Time	10V Step to 0.1% Av = −1, R_L = 2 kΩ	120							ns
Phase Margin		45							Deg
Differential Gain	NTSC, Av = +4	<0.1							%
Differential Phase	NTSC, Av = +4	0.1							Deg
Input Noise Voltage	f = 10 kHz	15							$nV/\sqrt{Hz}$
Input Noise Current	f = 10 kHz	1.5							$pA/\sqrt{Hz}$

Note 1: Continuous short-circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.

Note 2: The typical junction-to-ambient thermal resistance of the molded plastic DIP (N) is 105°C/W, the molded plastic SO (M) package is 155°C/W, and the cerdip (J) package is 125°C/W. All numbers apply for packages soldered directly into a printed circuit board.

Note 3: Unless otherwise specified, all limits guaranteed for $T_A = T_j$ = 25°C with supply voltage = ±15V, V_{CM} = 0V, and $R_L \geq$ 100 kΩ. **Boldface** limits apply over the range listed under "Operating Temperature Range" with $T_A = T_j$ in the "Absolute Maximum Ratings" section.

Note 4: All limits guaranteed at room temperature (standard type face) and at **temperature extremes (bold type face)**. All limits are 100% production tested.

Note 5: All limits guaranteed at **temperature extremes (bold type face)** via correlation using standard Statistical Quality Control (SQC) methods.

Note 6: For single supply operation, the following conditions apply: V^+ = 5V, V^- = 0V, V_{CM} = 2.5V, V_{OUT} = 2.5V. Pin 1 & Pin 8 (Vos Adjust) are each connected to Pin 4 (V−) to realize maximum output swing. This connection will degrade V_{OS}, V_{OS} Drift, and Input Voltage Noise.

Note 7: $C_L \leq$ 5 pF.

Note 8: In order to achieve optimum AC performance, the input stage was designed without protective clamps. Exceeding the maximum differential input voltage results in reverse breakdown of the base-emitter junction of one of the input transistors and probable degradation of the input parameters (especially Vos, Ios, and Noise).

Note 9: The average voltage that the weakest pin combinations (those involving Pin 2 or Pin 3) can withstand and still conform to the datasheet limits. The test circuit used consists of the human body model of 100 pF in series with 1500Ω.

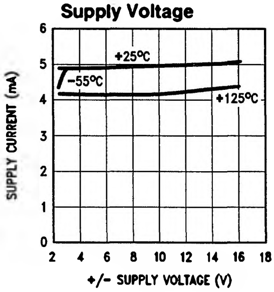
Note 10: V_{IN} = 8V step. For supply = ±5V, V_{IN} = 5V step.

Note 11: Voltage Gain is the total output swing (20V) divided by the input signal required to produce that swing.

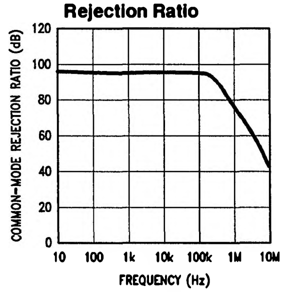
Note 12: The voltage between V^+ and either input pin must not exceed 36V.

Typical Performance Characteristics (R_L = 10 kΩ, T_A = 25°C unless otherwise specified)

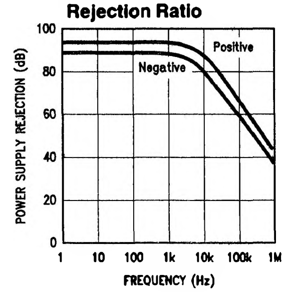
Supply Current vs Supply Voltage



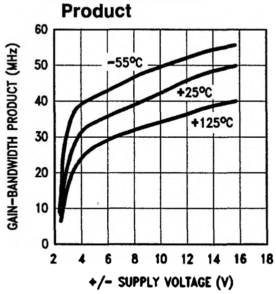
Common-Mode Rejection Ratio



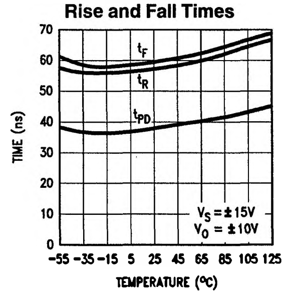
Power Supply Rejection Ratio



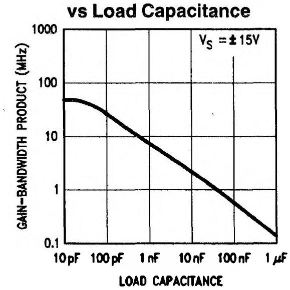
Gain-Bandwidth Product



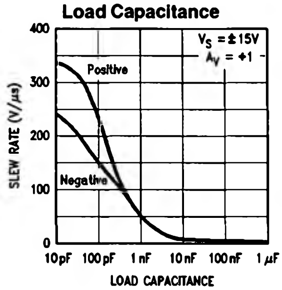
Propagation Delay Rise and Fall Times



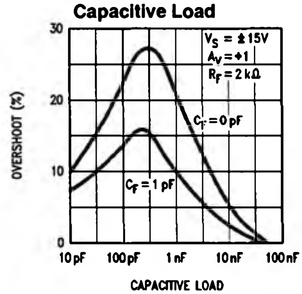
Gain-Bandwidth Product vs Load Capacitance



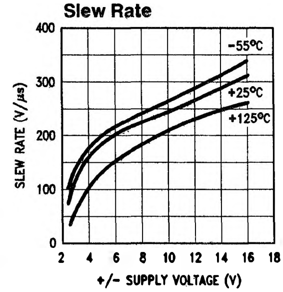
Slew Rate vs Load Capacitance



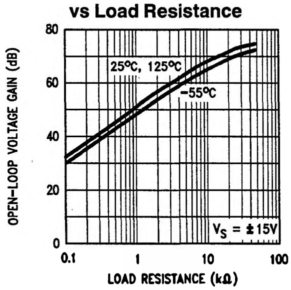
Overshoot vs Capacitive Load



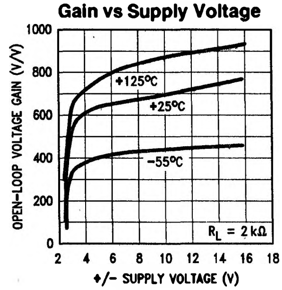
Slew Rate



Voltage Gain vs Load Resistance



Gain vs Supply Voltage



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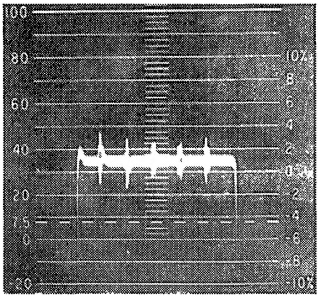
Typical Performance Characteristics

(R_L = 10 kΩ, T_A = 25°C unless otherwise specified) (Continued)

Differential Gain (Note)



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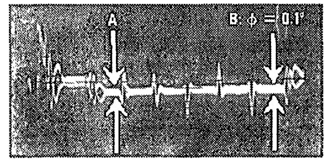
Differential Phase (Note)



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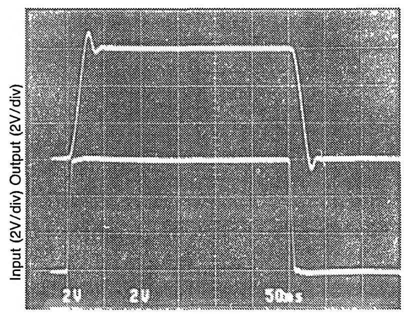
Note: Differential gain and differential phase measured for four series LM6361 op amps configured as unity-gain followers, in series with an LM6321 buffer. Error added by LM6321 is negligible. Test performed using Tektronix Type 520 NTSC test system.

Step Response; Av = +1



(50 ns/div)

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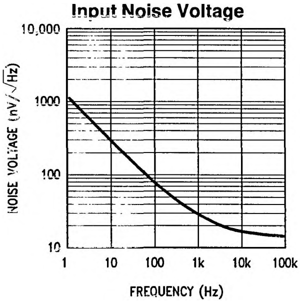
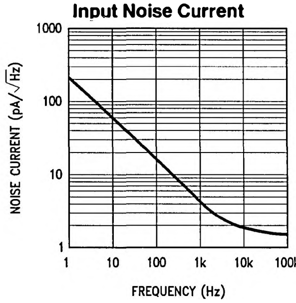
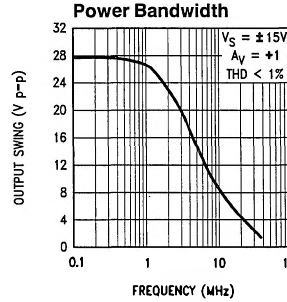
Input Noise Voltage



Input Noise Current



Power Bandwidth



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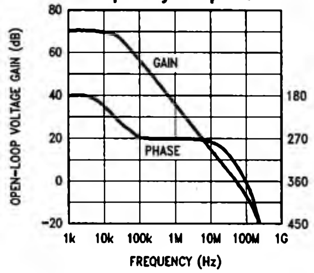
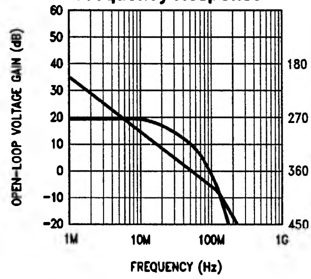
Typical Performance Characteristics

(R_L = 10 kΩ, T_A = 25°C unless otherwise specified) (Continued)

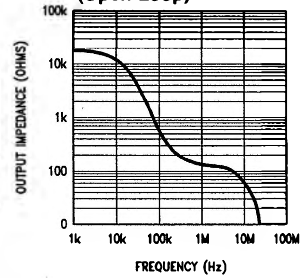
Open-Loop Frequency Response



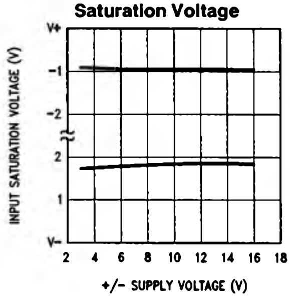
Open-Loop Frequency Response



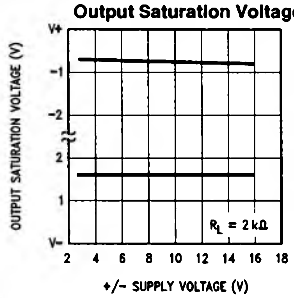
Output Impedence (Open-Loop)



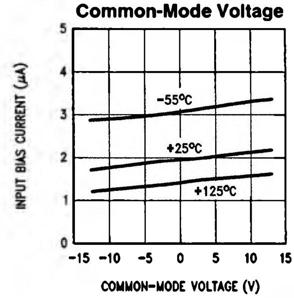
Common-Mode Input Saturation Voltage



Output Saturation Voltage



Bias Current vs Common-Mode Voltage



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Applications Tips

The LM6361 has been compensated for unity-gain operation. Since this compensation involved adding emitter-degeneration resistors to the op amp's input stage, the open-loop gain was reduced as the stability increased. Gain error due to reduced A_{VOL} is most apparent at high gains; thus, for gains between 5 and 25, the less-compensated LM6364 should be used, and the uncompensated LM6365 is appropriate for gains of 25 or more. The LM6361, LM6364, and LM6365 have the same high slew rate, regardless of their compensation.

The LM6361 is unusually tolerant of capacitive loads. Most op amps tend to oscillate when their load capacitance is greater than about 200 pF (especially in low-gain circuits). The LM6361's compensation is effectively increased with load capacitance, reducing its bandwidth and increasing its stability.

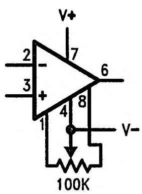
Power supply bypassing is not as critical for the LM6361 as it is for other op amps in its speed class. Bypassing will, however, improve the stability and transient response and is recommended for every design. 0.01 μF to 0.1 μF ceramic capacitors should be used (from each supply "rail" to ground); if the device is far away from its power supply source, an additional 2.2 μF to 10 μF of tantalum may provide extra noise reduction.

Keep all leads short to reduce stray capacitance and lead inductance, and make sure ground paths are low-impedance, especially where heavier currents will be flowing. Stray capacitance in the circuit layout can cause signal coupling across adjacent nodes and can cause gain to unintentionally vary with frequency.

Breadboarded circuits will work best if they are built using generic PC boards with a good ground plane. If the op amps are used with sockets, as opposed to being soldered into the circuit, the additional input capacitance may degrade circuit performance.

Typical Applications

Offset Voltage Adjustment



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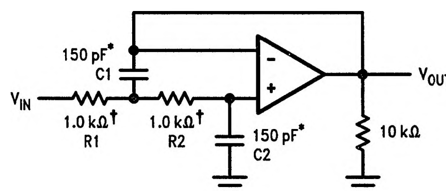
1 MHz Low-Pass Filter



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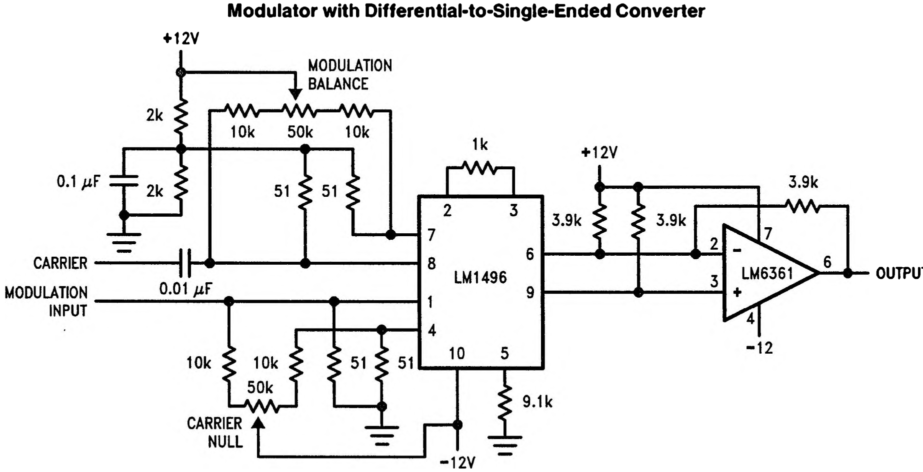
†1% tolerance

*Matching determines filter precision

$f_c = 2\pi\sqrt{(R1\ R2\ C1\ C2)}^{-1}$

Modulator with Differential-to-Single-Ended Converter



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