National Semiconductor Corporation

PRELIMINARY

LM6161/LM6261/LM6361 High Speed Operational Amplifier

General Description

The LM6161 family of high-speed amplifiers exhibits an excellent speed-power product in delivering 300 V/μs and 50 MHz unity gain stability with only 5 mA of supply current. Further power savings and application convenience are possible by taking advantage of the wide dynamic range in operating supply voltage which extends all the way down to +5V.

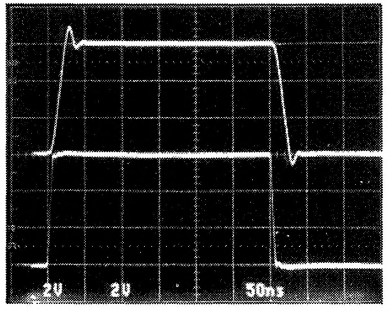
These amplifiers are built with National's new VIP™ (Vertically Integrated PNP) process which provides fast PNP transistors that are true complements to the already fast NPN devices. This advanced junction-isolated process delivers high speed performance without the need for complex and expensive dielectric isolation.

Features

■ High slew rate	300 V/μs
■ High unity gain freq	50 MHz
■ Low supply current	5 mA
■ Fast settling	120 ns to 0.1%
■ Low differential gain	<0.1%
■ Low differential phase	0.1°
■ Wide supply range	4.75V to 32V
■ Stable with unlimited capacitive load	
■ Well behaved; easy to apply	

Typical AC Characteristics

Step Response; Av = +1



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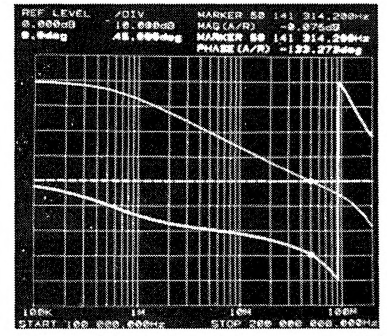
Gain & Phase; Av = +100



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Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage ($V^+ - V^-$)	36V
Differential Input Voltage (Note 8)	±8V
CM Voltage	$(V^+ - 0.7V)$ to $(V^- - 7V)$
Output Short Circuit to GND (Note 1)	Continuous
Lead Temperature (Soldering, 10 sec.)	260°C
Storage Temp Range	−65°C to +150°C
Operating Temperature Range (Note 2)	
LM6161	−55°C to +125°C
LM6261	−25°C to +85°C
LM6361	0°C to +70°C
Max Junction Temperature	150°C
ESD Tolerance (Notes 8 and 9)	±700V
Operating Supply Voltage Range	4.75V to 32V

DC Electrical Characteristics (Note 3)

Parameter	Conditions	Typ	LM6161		LM6261		LM6361		Units
			Tested Limit (Note 4)	Design Limit (Note 5)	Tested Limit (Note 4)	Design Limit (Note 5)	Tested Limit (Note 4)	Design Limit (Note 5)	
Input Offset Voltage		5	7 **10**		7	**9**	20	**22**	mV max
Input Offset Voltage Average Drift		10							µV/°C
Input Bias Current		2	3 **6**		3	**5**	5	**6**	µA max
Input Offset Current		150	350 **800**		350	**600**	1500	**1900**	nA max
Input Offset Current Average Drift		0.4							nA/°C
Input Resistance	Differential	325							kΩ
Input Capacitance	Av = +1 @ 10 MHz	1.5							pF
Large Signal Voltage Gain	V_{OUT} = ±10V, R_L = 2 kΩ (Note 11)	750	550 **300**		550	**400**	400	**350**	V/V min
	R_L = 10 kΩ	2900							V/V
Input Common-Mode Voltage Range	Supply = ±15V	+14.0	+13.9 **+13.8**		+13.9	**+13.8**	+13.8	**+13.7**	Volts min
		−13.2	−12.9 **−12.7**		−12.9	**−12.7**	−12.8	**−12.7**	Volts min
	Supply = +5V (Note 6)	4.0	3.9 **3.8**		3.9	**3.8**	3.8	**3.7**	Volts min
		1.8	2.0 **2.2**		2.0	**2.2**	2.1	**2.2**	Volts max
Common-Mode Rejection Ratio	$-10V \le V_{CM} \le +10V$	94	80 **74**		80	**76**	72	**70**	dB min
Power Supply Rejection Ratio	$\pm 10V \le V\pm \le \pm 16V$	90	80 **74**		80	**76**	72	**70**	dB min
Output Voltage Swing	Supply = ±15V and R_L = 2 kΩ	+14.2	+13.5 **+13.3**		+13.5	**+13.3**	+13.4	**+13.3**	Volts min
		−13.4	−13.0 **−12.7**		−13.0	**−12.8**	−12.9	**−12.8**	Volts min
	Supply = +5V and R_L = 2 kΩ (Note 6)	4.2	3.5 **3.3**		3.5	**3.3**	3.4	**3.3**	Volts min
		1.3	1.7 **2.0**		1.7	**1.9**	1.8	**1.9**	Volts max
Output Short Circuit Current	Souce	65	30 **20**		30	**25**	30	**25**	mA min
	Sink	65	30 **20**		30	**25**	30	**25**	mA min
Supply Current		5.0	6.5 **6.8**		6.5	**6.7**	6.8	**6.9**	mA max

AC Electrical Characteristics (Notes 3 & 7)

Parameter	Conditions	Typ	LM6161		LM6261		LM6361		Units
			Tested Limit (Note 4)	Design Limit (Note 5)	Tested Limit (Note 4)	Design Limit (Note 5)	Tested Limit (Note 4)	Design Limit (Note 5)	
Gain-Bandwidth Product	@ F = 20 MHz	50	40 **32**		40	**35**	35	**32**	MHZ min
	$V^+ = \pm 5V$	35							MHz
Slew Rate	Av = +1 (Note 10)	300	225 **200**		225	**210**	200	**180**	V/μs min
	$V^+ = \pm 5V$	200							V/μs
Power Bandwidth	$V_{OUT} = 20\ V_{PP}$	4.5							MHz
Settling Time	10V Step to 0.1% Av = −1, R_L = 2 kΩ	120							ns
Phase Margin		45							Deg
Differential Gain	NTSC, Av = +4	<0.1							%
Differential Phase	NTSC, Av = +4	0.1							Deg
Input Noise Voltage	f = 10 kHz	15							$nV/\sqrt{Hz}$
Input Noise Current	f = 10 kHz	1.5							$pA/\sqrt{Hz}$

Note 1: Continuous short-circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.

Note 2: The typical junction-to-ambient thermal resistance of the molded plastic DIP (N) is 105°C/W, the molded plastic SO (M) package is 155°C/W, the cerdip (J) package is 125°C/W, and the TO-5 (H) package is 155°C/W. All numbers apply for packages soldered directly into a printed circuit board.

Note 3: Unless otherwise specified, all limits guaranteed for $T_A = T_j = 25°C$ with supply voltage = ±15V, V_{CM} = 0V, and $R_L \geq 100\ k\Omega$. **Boldface** limits apply over the range listed under "Operating Temperature Range" with $T_A = T_j$ in the "Absolute Maximum Ratings" section.

Note 4: Guaranteed and 100% production tested. These limits are used to calculate outgoing AQL levels.

Note 5: Guaranteed but not 100% production tested. These limits are not used to calculate outgoing AQL levels.

Note 6: For single supply operation, the following conditions apply: $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 2.5V$, $V_{OUT} = 2.5V$. Pin 1 & Pin 8 (Vos Adjust) are each connected to Pin 4 (V^-) to realize maximum output swing. This connection will degrade V_{OS}, V_{OS} Drift, and Input Voltage Noise.

Note 7: $C_L \leq 5$ pF.

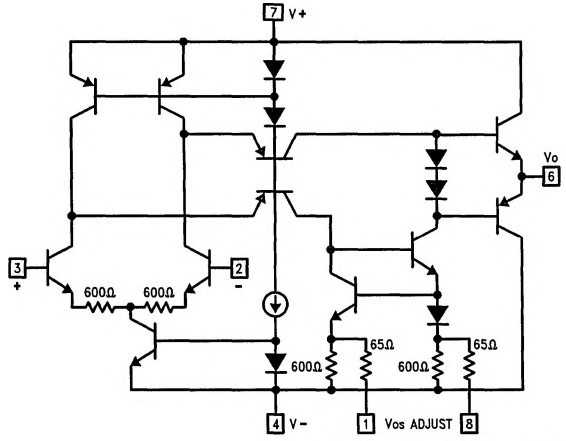
Note 8: In order to achieve optimum AC performance, the input stage was designed without protective clamps. Exceeding the maximum differential input voltage results in reverse breakdown of the base-emitter junction of one of the input transistors and probable degradation of the input parameters (especially Vos, Ios, and Noise).

Note 9: The average voltage that the weakest pin combinations (those involving Pin 2 or Pin 3) can withstand and still conform to the datasheet limits. The test circuit used consists of the human body model of 100 pF in series with 1500Ω.

Note 10: V_{IN} = 8V step. For $V^+ = \pm 5V$, V_{IN} = 5V step.

Note 11: Voltage Gain is the total output swing (20V) divided by the input signal required to produce that swing.

Simplified Schematic and Pin Assignments



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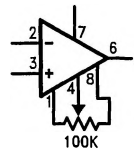
V_{OS} Adjust Circuit



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