LM6172QML Dual High Speed, Low Power, Low Distortion, Voltage Feedback Amplifiers

Check for Samples: LM6172QML

FEATURES

- **Available with Radiation Guarantee**
  - **High Dose Rate 300 krad(Si)**
  - **ELDRS Free 100 krad(Si)**
- **Easy to Use Voltage Feedback Topology**
- **High Slew Rate 3000V/μs**
- **Wide Unity-Gain Bandwidth 100MHz**
- **Low Supply Current 2.3mA / Amplifier**
- **High Output Current 50mA / Amplifier**
- **Specified for ±15V and ±5V operation**

APPLICATIONS

- **Scanner I- to -V Converters**
- **ADSL/HDSL Drivers**
- **Multimedia Broadcast Systems**
- **Video Amplifiers**
- **NTSC, PAL® and SECAM Systems**
- **ADC/DAC Buffers**
- **Pulse Amplifiers and Peak Detectors**

DESCRIPTION

The LM6172 is a dual high speed voltage feedback amplifier. It is unity-gain stable and provides excellent DC and AC performance. With 100MHz unity-gain bandwidth, 3000V/μs slew rate and 50mA of output current per channel, the LM6172 offers high performance in dual amplifiers; yet it only consumes 2.3mA of supply current each channel.

The LM6172 operates on ±15V power supply for systems requiring large voltage swings, such as ADSL, scanners and ultrasound equipment. It is also specified at ±5V power supply for low voltage applications such as portable video systems.

The LM6172 is built with National's advanced VIP™ III (Vertically Integrated PNP) complementary bipolar process.

Connection Diagram

8-Pin DIP

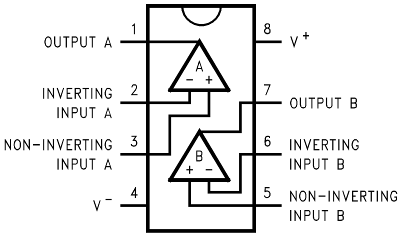

Figure 1. Top View

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16LD Ceramic SOIC

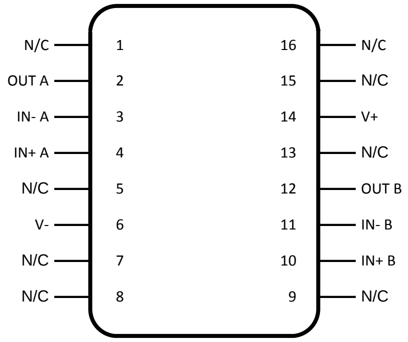
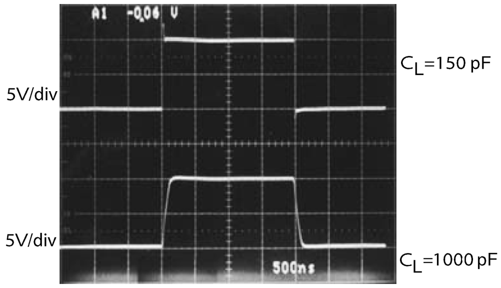
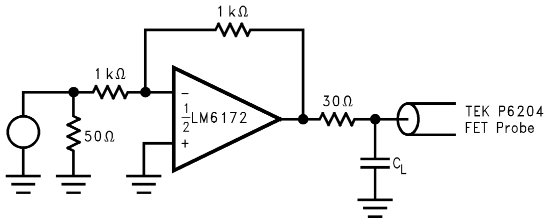


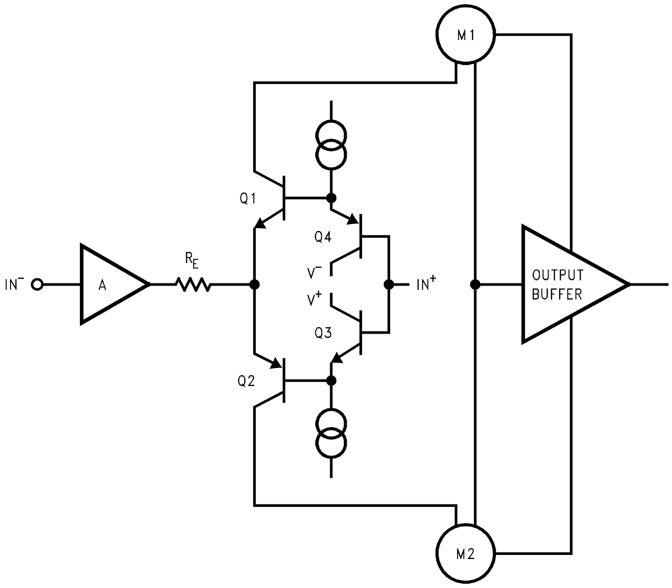
Figure 2. Top View

LM6172 Driving Capacitive Load





LM6172 Simplified Schematic (Each Amplifier)



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)

Supply Voltage ($V^+ - V^-$)	36V
Differential Input Voltage (2)	±10V
Maximum Junction Temperature	150°C
Power Dissipation (3), (4)	1.03W
Output Short Circuit to Ground (5)	Continuous
Storage Temperature Range	$-65°C \le T_A \le +150°C$
Common Mode Voltage Range	V^+ +0.3V to V^- −0.3V
Input Current	±10mA
Thermal Resistance (6)	
θ_{JA}	
8LD Ceramic Dip (Still Air)	100°C/W
8LD Ceramic Dip (500LF/Min Air Flow)	46°C/W
16LD Ceramic SOIC (Still Air) “WG”	124°C/W
16LD Ceramic SOIC (500LF/Min Air Flow) “WG”	74°C/W
16LD Ceramic SOIC (Still Air) “GW”	135°C/W
16LD Ceramic SOIC (500LF/Min Air Flow) “GW”	85°C/W
θ_{JC}	
8LD Ceramic Dip (4)	2°C/W
16LD Ceramic SOIC “WG” (4)	6°C/W
16LD Ceramic SOIC “GW”	7°C/W
Package Weight	
8LD Ceramic Dip	980mg
16LD Ceramic SOIC “WG”	365mg
16LD Ceramic SOIC “GW”	410mg
ESD Tolerance (7)	4KV

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(2) Differential Input Voltage is measured at $V_S = \pm 15V$.
(3) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax} (maximum junction temperature), θ_{JA} (package junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is $P_{Dmax} = (T_{Jmax} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower.
(4) The package material for these devices allows much improved heat transfer over our standard ceramic packages. In order to take full advantage of this improved heat transfer, heat sinking must be provided between the package base (directly beneath the die), and either metal traces on, or thermal vias through, the printed circuit board. Without this additional heat sinking, device power dissipation must be calculated using θ_{JA}, rather than θ_{JC}, thermal resistance. It must not be assumed that the device leads will provide substantial heat transfer out the package, since the thermal resistance of the leadframe material is very poor, relative to the material of the package base. The stated θ_{JC} thermal resistance is for the package material only, and does not account for the additional thermal resistance between the package base and the printed circuit board. The user must determine the value of the additional thermal resistance and must combine this with the stated value for the package, to calculate the total allowed power dissipation for the device.
(5) Continuous short circuit operation can result in exceeding the maximum allowed junction temperature of 150°C
(6) All numbers apply for packages soldered directly into a PC board.
(7) Human body model, 1.5 kΩ in series with 100 pF.

Recommended Operating Conditions (1)

Supply Voltage	$5.5V \le V_S \le 36V$
Operating Temperature Range	$-55°C \le T_A \le +125°C$

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Quality Conformance Inspection

Table 1. Mil-Std-883, Method 5005 - Group A

Subgroup	Description	Temp (°C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55
12	Settling time at	+25
13	Settling time at	+125
14	Settling time at	-55

LM6172 (±5V) Electrical Characteristics (1) DC Parameters

The following conditions apply, unless otherwise specified. T_J = 25°C, V^+ = +5V, V^- = −5V, V_{CM} = 0V & R_L > 1MΩ

Symbol	Parameter	Conditions	Notes	Min	Max	Units	Sub-groups
V_{IO}	Input Offset Voltage				1.0	mV	1
					3.0	mV	2, 3
I_{IB}	Input Bias Current				2.5	µA	1
					3.5	µA	2, 3
I_{IO}	Input Offset Current				1.5	µA	1
					2.2	µA	2, 3
CMRR	Common Mode Rejection Ratio	V_{CM} = ±2.5V		70		dB	1
				65		dB	2, 3
PSRR	Power Supply Rejection Ratio	V_S = ±15V to ±5V		75		dB	1
				70		dB	2, 3
A_V	Large Signal Voltage Gain	R_L = 1KΩ	(2)	70		dB	1
			(2)	65		dB	2, 3
		R_L = 100Ω	(2)	65		dB	1
			(2)	60		dB	2, 3
V_O	Output Swing	R_L = 1KΩ		3.1	-3.1	V	1
				3.0	-3.0	V	2, 3
		R_L = 100Ω		2.5	-2.4	V	1
				2.4	-2.3	V	2, 3
I_L	Output Current (Open Loop)	Sourcing R_L = 100Ω	(3)	25		mA	1
			(3)	24		mA	2, 3
		Sinking R_L = 100Ω	(3)		-24	mA	1
			(3)		-23	mA	2, 3
I_S	Supply Current	Both Amplifiers			6.0	mA	1
					7.0	mA	2, 3

(1) Pre and post irradiation limits are identical to those listed under AC and DC electrical characteristics. These parts may be dose rate sensitive in a space environment and demonstrate enhanced low dose rate effect. Radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in Mil-Std-883, Method 1019.5, Condition A.

(2) Large signal voltage gain is the total output swing divided by the input signal required to produce that swing. For V_S = ±15V, V_{OUT} = ±5V. For V_S = ±5V, V_{OUT} = ±1V.

(3) The open loop output current is guaranteed by measurement of the open loop output voltage swing using 100Ω output load.

LM6172 (±5V) Electrical Characteristics (1) DC Drift Parameters (1)

The following conditions apply, unless otherwise specified. $T_J = 25°C$, $V^+ = +5V$, $V^- = -5V$, $V_{CM} = 0V$ & $R_L > 1M\Omega$
Delta calculations performed on QMLV devices at group B , subgroup 5.

Symbol	Parameter	Conditions	Notes	Min	Max	Units	Sub-groups
V_{IO}	Input Offset Voltage			-0.25	0.25	mV	1
I_{IB}	Input Bias Current			-0.50	0.50	µA	1
I_{IO}	Input Ofset Current			-0.25	0.25	µA	1

(1) Pre and post irradiation limits are identical to those listed under AC and DC electrical characteristics. These parts may be dose rate sensitive in a space environment and demonstrate enhanced low dose rate effect. Radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in Mil-Std-883, Method 1019.5, Condition A.

LM6172 (±15V) Electrical Characteristics DC Parameters (1)

The following conditions apply, unless otherwise specified. T_J = 25°C, V^+ = +15V, V^- = −15V, V_{CM} = 0V, & R_L = 1MΩ

Symbol	Parameter	Conditions	Notes	Min	Max	Units	Sub-groups
V_{IO}	Input Offset Voltage				1.5	mV	1
					3.5	mV	2, 3
I_{IB}	Input Bias Current				3.0	µA	1
					4.0	µA	2, 3
I_{IO}	Input Offset Current				2.0	µA	1
					3.0	µA	2, 3
CMRR	Common Mode Rejection Ratio	V_{CM} = ±10V		70		dB	1
				65		dB	2, 3
PSRR	Power Supply Rejection Ratio	V_S = ±15V to ±5V		75		dB	1
				70		dB	2, 3
A_V	Large Signal Voltage Gain	R_L = 1KΩ	(2)	75		dB	1
			(2)	70		dB	2, 3
		R_L = 100Ω	(2)	65		dB	1
			(2)	60		dB	2, 3
V_O	Output Swing	R_L = 1KΩ		12.5	-12.5	V	1
				12	-12	V	2, 3
		R_L = 100Ω		6.0	-6.0	V	1
				5.0	-5.0	V	2, 3
I_L	Output Current (Open Loop)	Sourcing R_L = 100Ω	(3)	60		mA	1
			(3)	50		mA	2, 3
		Sinking R_L = 100Ω	(3)		-60	mA	1
			(3)		-50	mA	2, 3
I_S	Supply Current	Both Amplifiers			8.0	mA	1
					9.0	mA	2, 3

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(1) Pre and post irradiation limits are identical to those listed under AC and DC electrical characteristics. These parts may be dose rate sensitive in a space environment and demonstrate enhanced low dose rate effect. Radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in Mil-Std-883, Method 1019.5, Condition A.

(2) Large signal voltage gain is the total output swing divided by the input signal required to produce that swing. For V_S = ±15V, V_{OUT} = ±5V. For V_S = ±5V, V_{OUT} = ±1V.

(3) The open loop output current is guaranteed by measurement of the open loop output voltage swing using 100Ω output load.

LM6172 (±15V) Electrical Characteristics AC Parameters (1)

The following conditions apply, unless otherwise specified. $T_J = 25°C$, $V^+ = +15V$, $V^- = -15V$, $V_{CM} = 0V$

Symbol	Parameter	Conditions	Notes	Min	Max	Units	Sub-groups
SR	Slew Rate	$A_V = 2$, $V_I = ±2.5V$ 3nS Rise & Fall time	(2), (3)	1700		V/µS	4
GBW	Unity-Gain Bandwidth		(4)	80		MHz	4

(1) Pre and post irradiation limits are identical to those listed under AC and DC electrical characteristics. These parts may be dose rate sensitive in a space environment and demonstrate enhanced low dose rate effect. Radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in Mil-Std-883, Method 1019.5, Condition A.
(2) See AN0009 for SR test circuit.
(3) Slew Rate measured between ±4V.
(4) See AN0009 for GBW test circuit.

LM6172 (±15V) Electrical Characteristics DC Drift Parameters [(1)]

The following conditions apply, unless otherwise specified. $T_J = 25°C$, $V^+ = +15V$, $V^- = -15V$, $V_{CM} = 0V$
Delta calculations performed on QMLV devices at group B , subgroup 5.

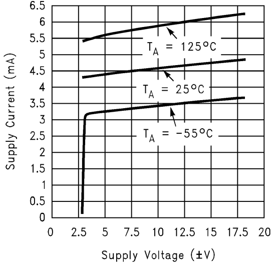
Symbol	Parameter	Conditions	Notes	Min	Max	Units	Sub-groups
V_{IO}	Input Offset Voltage			-0.25	0.25	mV	1
I_{IB}	Input Bias Current			-0.50	0.50	µA	1
I_{IO}	Input Offset Current			-0.25	0.25	µA	1

(1) Pre and post irradiation limits are identical to those listed under AC and DC electrical characteristics. These parts may be dose rate sensitive in a space environment and demonstrate enhanced low dose rate effect. Radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in Mil-Std-883, Method 1019.5, Condition A.

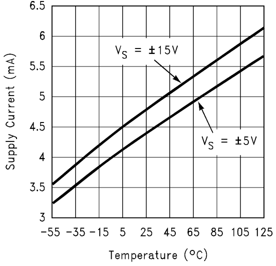
Typical Performance Characteristics

Unless otherwise noted, $T_A = 25°C$

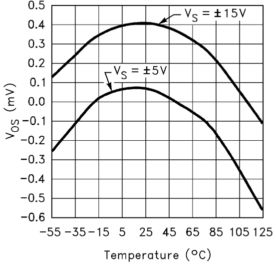
Supply Voltage vs. Supply Current



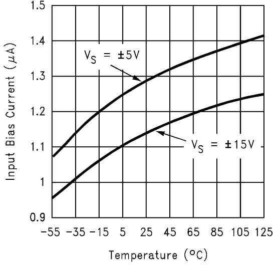
Supply Current vs. Temperature



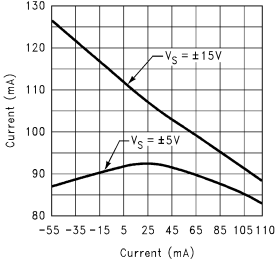
Input Offset Voltage vs. Temperature



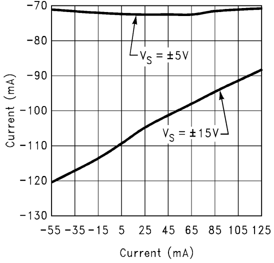
Input Bias Current vs. Temperature



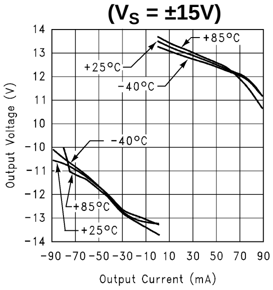
Short Circuit Current vs. Temperature (Sourcing)



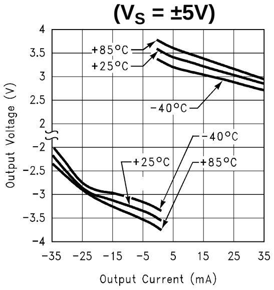
Short Circuit Current vs. Temperature (Sinking)



Output Voltage vs. Output Current ($V_S = ±15V$)



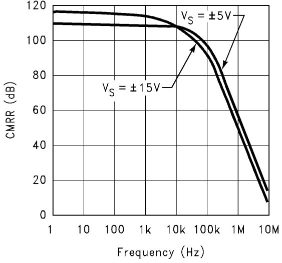
Output Voltage vs. Output Current ($V_S = ±5V$)



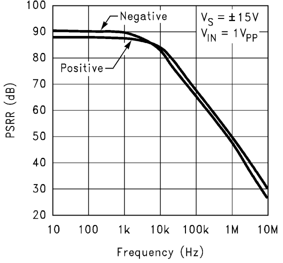
Typical Performance Characteristics (continued)

Unless otherwise noted, T_A = 25°C

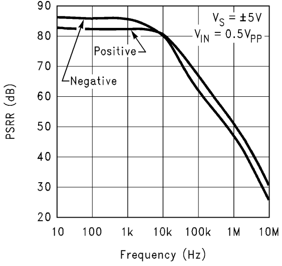
CMRR vs. Frequency



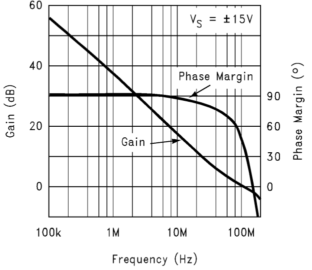
PSRR vs. Frequency



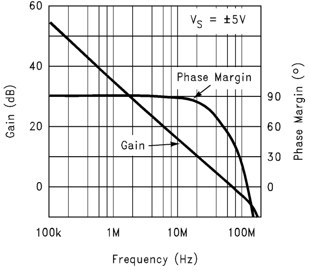
PSRR vs. Frequency



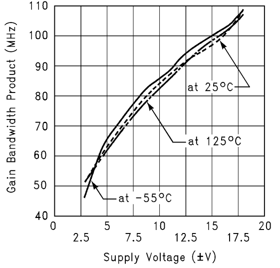
Open-Loop Frequency Response



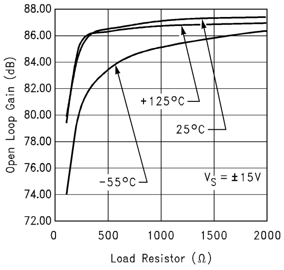
Open-Loop Frequency Response



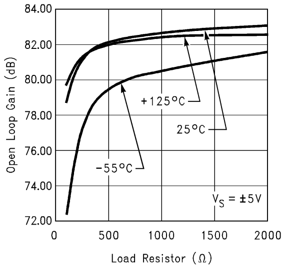
Gain-Bandwidth Product vs. Supply Voltage at Different Temperature



Large Signal Voltage Gain vs. Load



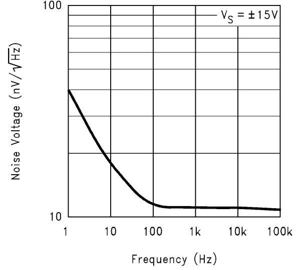
Large Signal Voltage Gain vs. Load



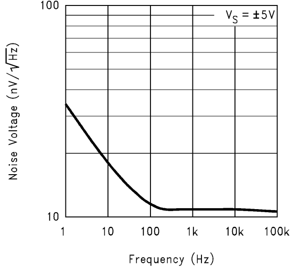
Typical Performance Characteristics (continued)

Unless otherwise noted, T_A = 25°C

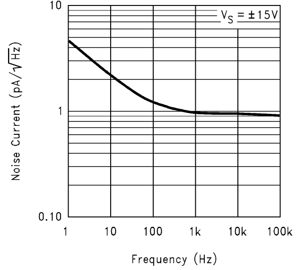
**Input Voltage Noise
vs.
Frequency**



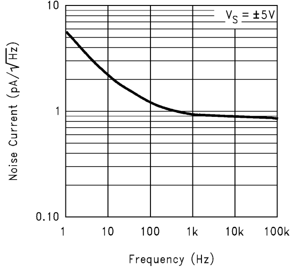
**Input Voltage Noise
vs.
Frequency**



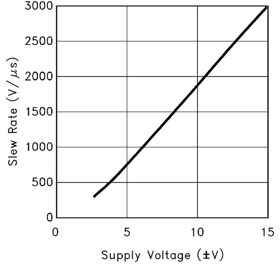
**Input Current Noise
vs.
Frequency**



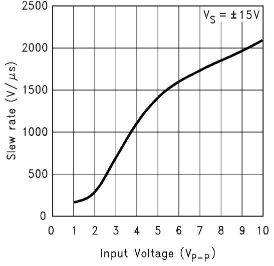
**Input Current Noise
vs.
Frequency**



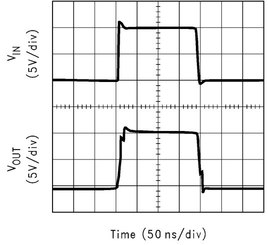
**Slew Rate
vs.
Supply Voltage**



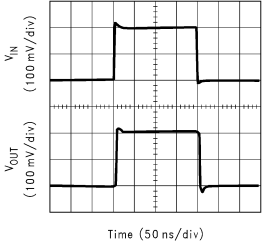
**Slew Rate
vs.
Input Voltage**



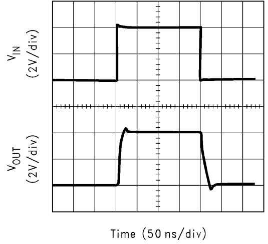
**Large Signal Pulse Response
A_V = +1, V_S = ±15V**



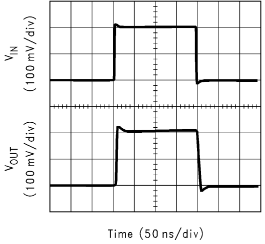
**Small Signal Pulse Response
A_V = +1, V_S = ±15V**



**Large Signal Pulse Response
A_V = +1, V_S = ±5V**



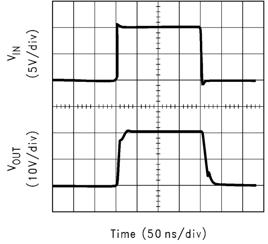
**Small Signal Pulse Response
A_V = +1, V_S = ±5V**



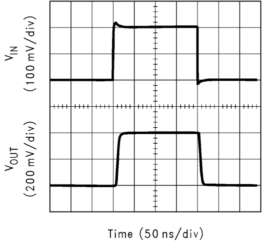
Typical Performance Characteristics (continued)

Unless otherwise noted, T_A = 25°C

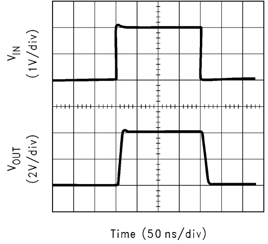
Large Signal Pulse Response
$A_V = +2, V_S = \pm15V$



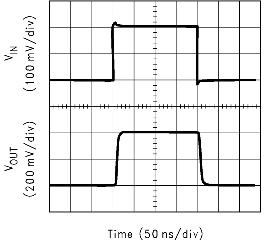
Small Signal Pulse Response
$A_V = +2, V_S = \pm15V$



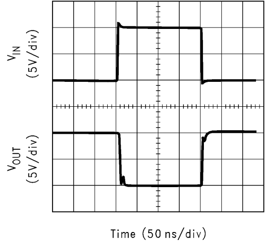
Large Signal Pulse Response
$A_V = +2, V_S = \pm5V$



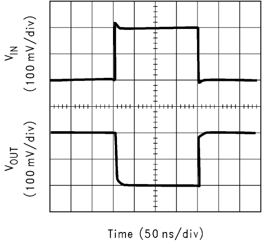
Small Signal Pulse Response
$A_V = +2, V_S = \pm5V$



Large Signal Pulse Response
$A_V = -1, V_S = \pm15V$



Small Signal Pulse Response
$A_V = -1, V_S = \pm15V$



Large Signal Pulse Response
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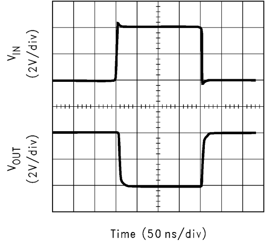
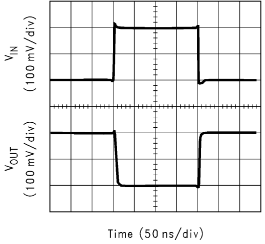
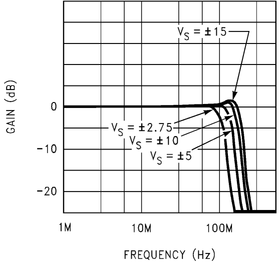


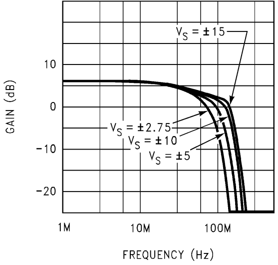
Small Signal Pulse Response
$A_V = -1, V_S = \pm5V$



Closed Loop Frequency Response
vs.
Supply Voltage
(A_V = +1)



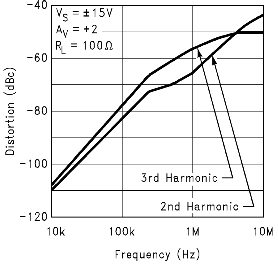
Closed Loop Frequency Response
vs.
Supply Voltage
(A_V = +2)



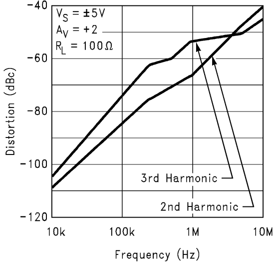
Typical Performance Characteristics (continued)

Unless otherwise noted, T_A = 25°C

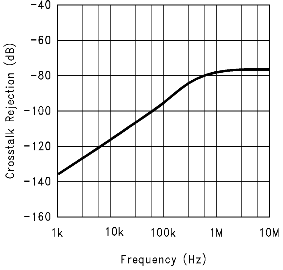
Harmonic Distortion vs. Frequency (V_S = ±15V)



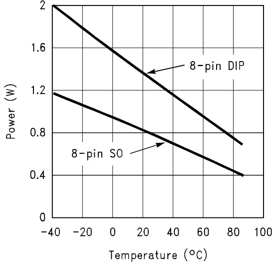
Harmonic Distortion vs. Frequency (V_S = ±5V)



Crosstalk Rejection vs. Frequency



Maximum Power Dissipation vs. Ambient Temperature



APPLICATION NOTES

LM6172 PERFORMANCE DISCUSSION

The LM6172 is a dual high-speed, low power, voltage feedback amplifier. It is unity-gain stable and offers outstanding performance with only 2.3mA of supply current per channel. The combination of 100MHz unity-gain bandwidth, 3000V/μs slew rate, 50mA per channel output current and other attractive features makes it easy to implement the LM6172 in various applications. Quiescent power of the LM6172 is 138mW operating at ±15V supply and 46mW at ±5V supply.

LM6172 CIRCUIT OPERATION

The class AB input stage in LM6172 is fully symmetrical and has a similar slewing characteristic to the current feedback amplifiers. In the LM6172 Simplified Schematic (Page 2), Q1 through Q4 form the equivalent of the current feedback input buffer, R_E the equivalent of the feedback resistor, and stage A buffers the inverting input. The triple-buffered output stage isolates the gain stage from the load to provide low output impedance.

LM6172 SLEW RATE CHARACTERISTIC

The slew rate of LM6172 is determined by the current available to charge and discharge an internal high impedance node capacitor. This current is the differential input voltage divided by the total degeneration resistor R_E. Therefore, the slew rate is proportional to the input voltage level, and the higher slew rates are achievable in the lower gain configurations.

When a very fast large signal pulse is applied to the input of an amplifier, some overshoot or undershoot occurs. By placing an external series resistor such as 1kΩ to the input of LM6172, the slew rate is reduced to help lower the overshoot, which reduces settling time.

REDUCING SETTLING TIME

The LM6172 has a very fast slew rate that causes overshoot and undershoot. To reduce settling time on LM6172, a 1kΩ resistor can be placed in series with the input signal to decrease slew rate. A feedback capacitor can also be used to reduce overshoot and undershoot. This feedback capacitor serves as a zero to increase the stability of the amplifier circuit. A 2pF feedback capacitor is recommended for initial evaluation. When the LM6172 is configured as a buffer, a feedback resistor of 1kΩ must be added in parallel to the feedback capacitor.

Another possible source of overshoot and undershoot comes from capacitive load at the output. Please see the section “Driving Capacitive Loads” for more detail.

DRIVING CAPACITIVE LOADS

Amplifiers driving capacitive loads can oscillate or have ringing at the output. To eliminate oscillation or reduce ringing, an isolation resistor can be placed as shown in Figure 3. The combination of the isolation resistor and the load capacitor forms a pole to increase stability by adding more phase margin to the overall system. The desired performance depends upon the value of the isolation resistor; the bigger the isolation resistor, the more damped (slow) the pulse response becomes. For LM6172, a 50Ω isolation resistor is recommended for initial evaluation.

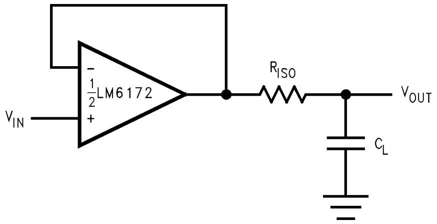


Figure 3. Isolation Resistor Used to Drive Capacitive Load

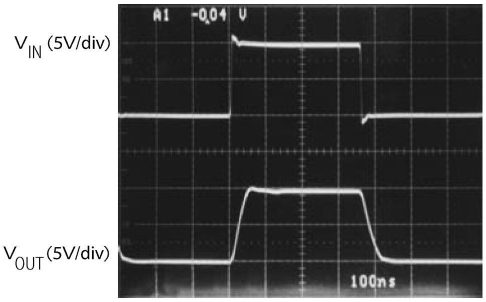


Figure 4. The LM6172 Driving a 510pF Load with a 30Ω Isolation Resistor

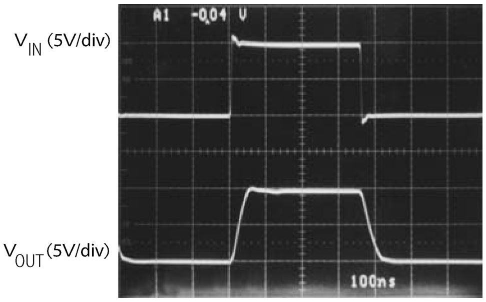


Figure 5. The LM6172 Driving a 220 pF Load with a 50Ω Isolation Resistor

LAYOUT CONSIDERATION

Printed Circuit Boards And High Speed Op Amps

There are many things to consider when designing PC boards for high speed op amps. Without proper caution, it is very easy to have excessive ringing, oscillation and other degraded AC performance in high speed circuits. As a rule, the signal traces should be short and wide to provide low inductance and low impedance paths. Any unused board space needs to be grounded to reduce stray signal pickup. Critical components should also be grounded at a common point to eliminate voltage drop. Sockets add capacitance to the board and can affect frequency performance. It is better to solder the amplifier directly into the PC board without using any socket.

Using Probes

Active (FET) probes are ideal for taking high frequency measurements because they have wide bandwidth, high input impedance and low input capacitance. However, the probe ground leads provide a long ground loop that will produce errors in measurement. Instead, the probes can be grounded directly by removing the ground leads and probe jackets and using scope probe jacks.

Components Selection And Feedback Resistor

It is important in high speed applications to keep all component leads short because wires are inductive at high frequency. For discrete components, choose carbon composition-type resistors and mica-type capacitors. Surface mount components are preferred over discrete components for minimum inductive effect.

Large values of feedback resistors can couple with parasitic capacitance and cause undesirable effects such as ringing or oscillation in high speed amplifiers. For LM6172, a feedback resistor less than 1kΩ gives optimal performance.

COMPENSATION FOR INPUT CAPACITANCE

The combination of an amplifier's input capacitance with the gain setting resistors adds a pole that can cause peaking or oscillation. To solve this problem, a feedback capacitor with a value

$$C_F > (R_G \times C_{IN})/R_F \quad (1)$$

can be used to cancel that pole. For LM6172, a feedback capacitor of 2pF is recommended. Figure 6 illustrates the compensation circuit.

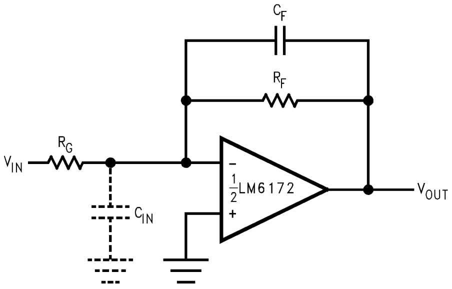


Figure 6. Compensating for Input Capacitance

POWER SUPPLY BYPASSING

Bypassing the power supply is necessary to maintain low power supply impedance across frequency. Both positive and negative power supplies should be bypassed individually by placing 0.01μF ceramic capacitors directly to power supply pins and 2.2μF tantalum capacitors close to the power supply pins.

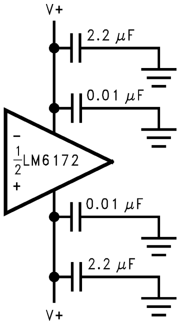


Figure 7. Power Supply Bypassing

TERMINATION

In high frequency applications, reflections occur if signals are not properly terminated. Figure 8 shows a properly terminated signal while Figure 9 shows an improperly terminated signal.

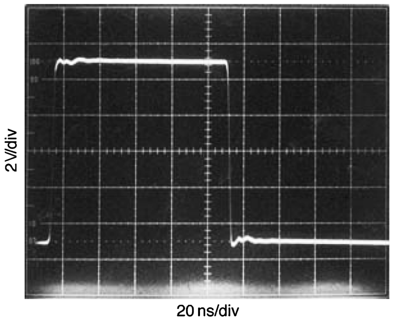


Figure 8. Properly Terminated Signal

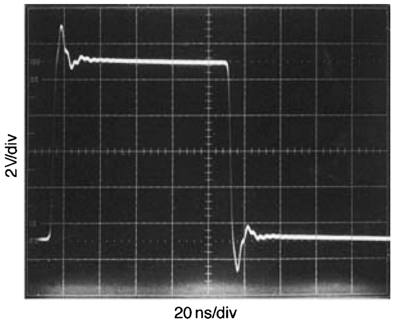


Figure 9. Improperly Terminated Signal

To minimize reflection, coaxial cable with matching characteristic impedance to the signal source should be used. The other end of the cable should be terminated with the same value terminator or resistor. For the commonly used cables, RG59 has 75Ω characteristic impedance, and RG58 has 50Ω characteristic impedance.

POWER DISSIPATION

The maximum power allowed to dissipate in a device is defined as:

$$P_D = (T_{J(max)} - T_A)/\theta_{JA} \quad (2)$$

Where P_D is the power dissipation in a device

$T_{J(max)}$ is the maximum junction temperature

T_A is the ambient temperature

θ_{JA} is the thermal resistance of a particular package

For example, for the LM6172 in a SO-16 package, the maximum power dissipation at 25°C ambient temperature is 1000mW.

Thermal resistance, θ_{JA}, depends on parameters such as die size, package size and package material. The smaller the die size and package, the higher θ_{JA} becomes. The 8-pin DIP package has a lower thermal resistance (95°C/W) than that of 8-pin SO (160°C/W). Therefore, for higher dissipation capability, use an 8-pin DIP package.

The total power dissipated in a device can be calculated as:

$$P_D = P_Q + P_L \quad (3)$$

P_Q is the quiescent power dissipated in a device with no load connected at the output. P_L is the power dissipated in the device with a load connected at the output; it is not the power dissipated by the load.

Furthermore,

P_Q: **=** supply current x total supply voltage with no load

P_L: **=** output current x (voltage difference between supply voltage and output voltage of the same supply)

For example, the total power dissipated by the LM6172 with V_S = ±15V and both channels swinging output voltage of 10V into 1kΩ is

P_D: **=** $P_Q + P_L$

: **=** 2[(2.3mA)(30V)] + 2[(10mA)(15V − 10V)]

: **=** 138mW + 100mW

: **=** 238mW

Application Circuits

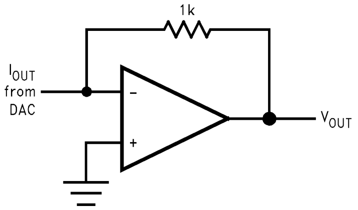


Figure 10. I- to -V Converters

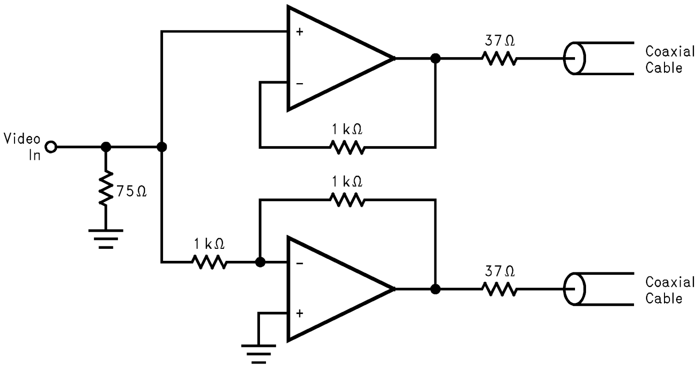


Figure 11. Differential Line Driver

Table 2. Revision History

Released	Revision	Section	Changes
12/08/2010	A	New Release, Corporate format	1 MDS data sheet converted into one Corp. data sheet format. MNLM6172AM-X-RH Rev 0A0 will be archived.
10/05/2011	B	Features, Ordering Information, Abs Max Ratings, Footnotes	Update Radiation, Add new ELDRS FREE die id, 'GW' NSID'S w/coresponding SMD numbers. Add 'GW' Theta JA & Theta JC along with weight.Add Note 15, Modify Note 14. LM6172QML Rev A will be archived.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
5962-9560401QPA	ACTIVE	CDIP	NAB	8	40	TBD	CU SNPB	Level-1-NA-UNLIM	
5962-9560402QXA	ACTIVE	CLGA	NAC	16	42	TBD	CU SNPB	Level-1-NA-UNLIM	
5962F9560401QPA	ACTIVE	CDIP	NAB	8	40	TBD	CU SNPB	Level-1-NA-UNLIM	
5962F9560401VPA	ACTIVE	CDIP	NAB	8	40	TBD	CU SNPB	Level-1-NA-UNLIM	
5962F9560402VXA	ACTIVE	CLGA	NAC	16	42	TBD	CU SNPB	Level-1-NA-UNLIM	
5962R9560403VXA	ACTIVE	CLGA	NAC	16	42	TBD	CU SNPB	Level-1-NA-UNLIM	
LM6172AMGW-QML	ACTIVE	CLGA	NAC	16	42	TBD	CU SNPB	Level-1-NA-UNLIM	
LM6172AMGWFQMLV	ACTIVE	CLGA	NAC	16	42	TBD	CU SNPB	Level-1-NA-UNLIM	
LM6172AMGWRLQV	ACTIVE	CLGA	NAC	16	42	TBD	CU SNPB	Level-1-NA-UNLIM	
LM6172AMJ-QML	ACTIVE	CDIP	NAB	8	40	TBD	CU SNPB	Level-1-NA-UNLIM	
LM6172AMJFQML	ACTIVE	CDIP	NAB	8	40	TBD	CU SNPB	Level-1-NA-UNLIM	
LM6172AMJFQMLV	ACTIVE	CDIP	NAB	8	40	TBD	CU SNPB	Level-1-NA-UNLIM	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF LM6172QML, LM6172QML-SP :

- Military: LM6172QML

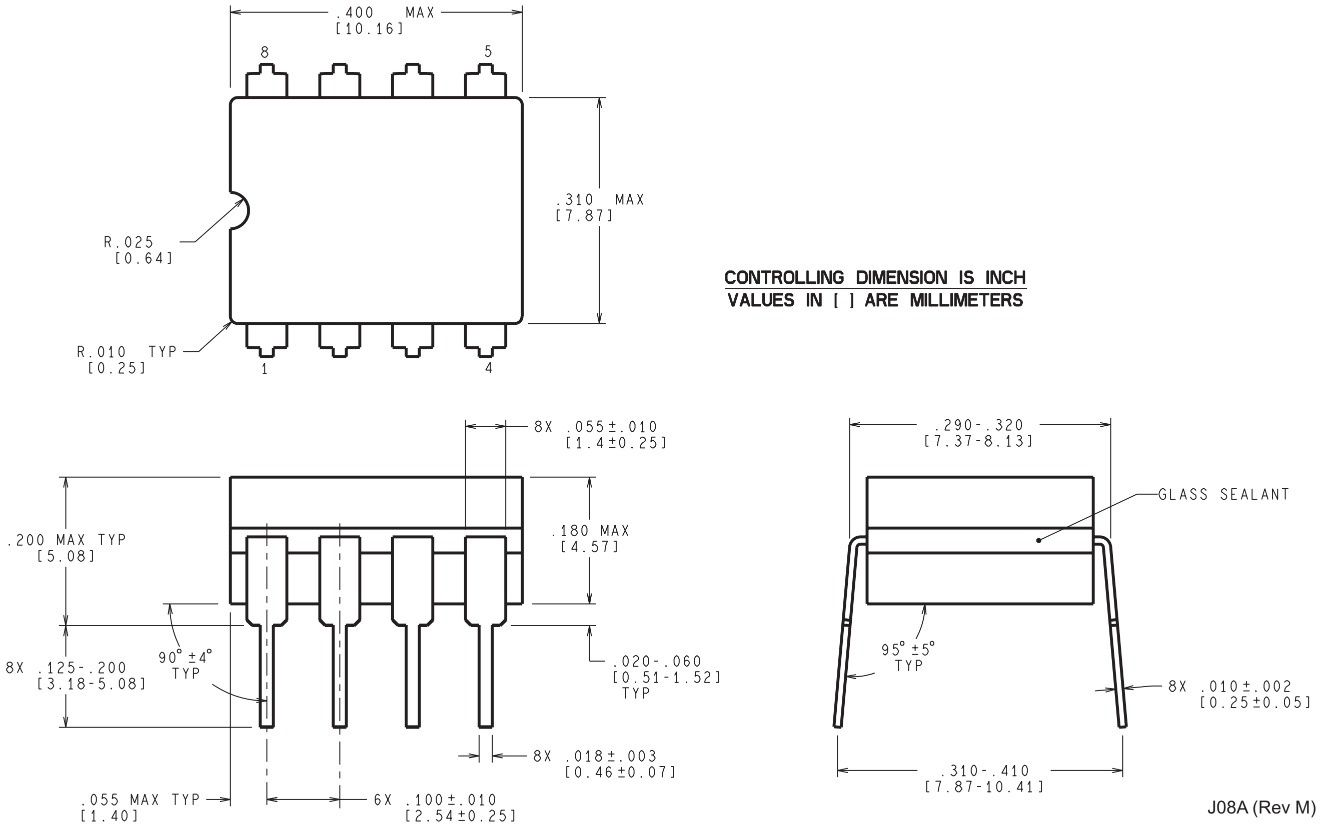
- Space: LM6172QML-SP

NOTE: Qualified Version Definitions:

- Military - QML certified for Military and Defense Applications

- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

NAB0008A



J08A (Rev M)

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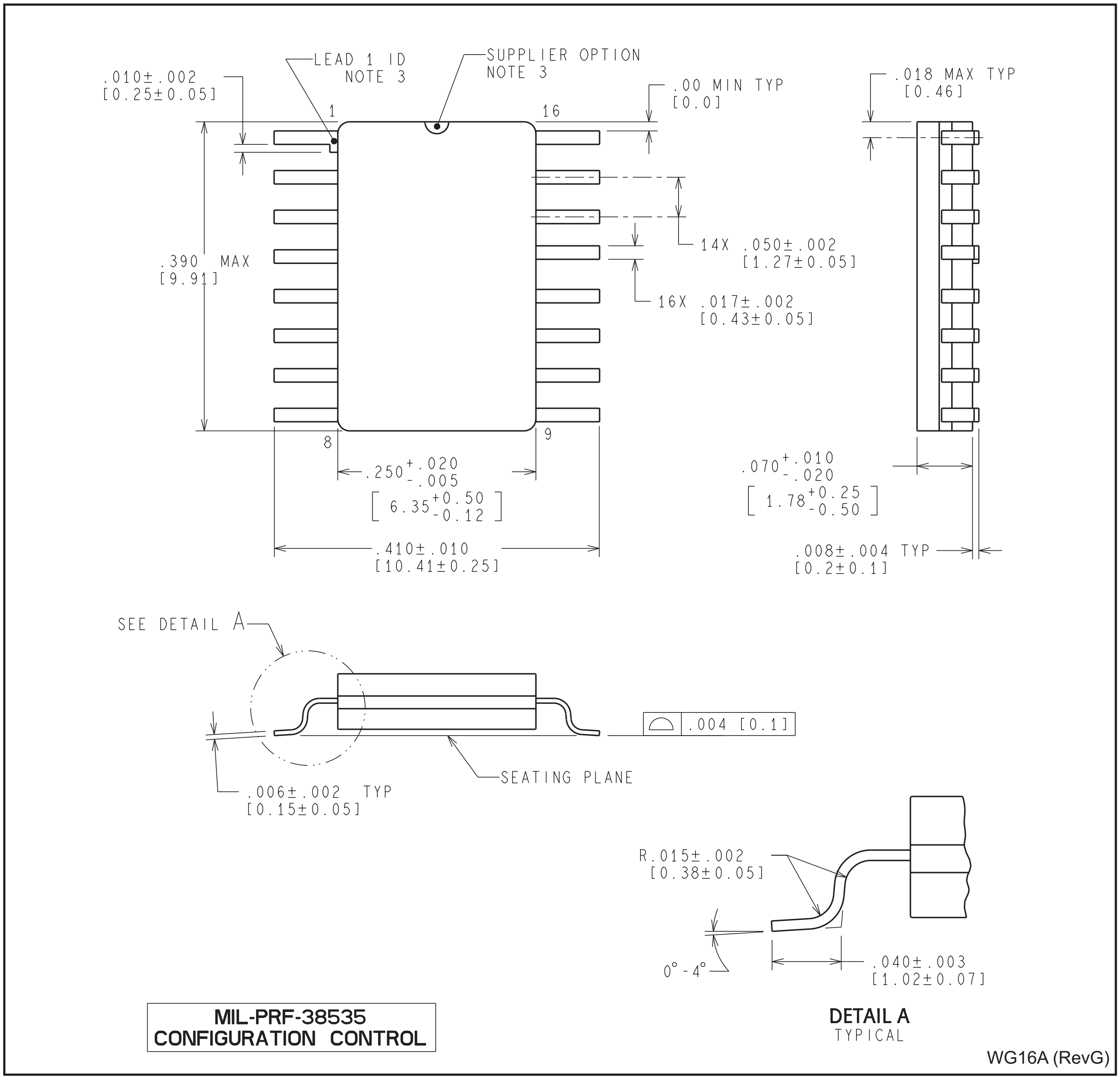
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.006±.002 TYP
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R.015±.002
[0.38±0.05]
0°-4°
.040±.003
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