

LM5113-Q1 Automotive 90-V, 1.2-A, 5-A, Half Bridge GaN Driver

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
 - Device Temperature Grade 1: -40°C to 125°C Ambient Operating Temperature Range
 - Device HBM ESD Classification Level 1C
 - Device CDM ESD Classification Level C6
- Independent High-Side and Low-Side TTL Logic Inputs
- 1.2-A Peak Source, 5-A Peak Sink Output Current
- High-Side Floating Bias Voltage Rail Operates up to 100-VDC
- Internal Bootstrap Supply Voltage Clamping
- Split Outputs for Adjustable Turnon and Turnoff Strength
- $0.6\text{-}\Omega$ Pulldown, $2.1\text{-}\Omega$ Pullup Resistance
- Fast Propagation Times (28 ns Typical)
- Excellent Propagation Delay Matching (1.5 ns Typical)
- Supply Rail Undervoltage Lockout
- Low Power Consumption

2 Applications

- Mobile Wireless Chargers
- Audio Power Amplifiers
- Audio Power Supplies
- Current-Fed Push-Pull Converters
- Half- and Full-Bridge Converters
- Synchronous Buck Converters

3 Description

The LM5113-Q1 is designed to drive both the high-side and the low-side enhancement mode Gallium Nitride (GaN) FETs or silicon MOSFETs in a synchronous buck, boost, or half bridge configuration for automotive applications. The device has an integrated 100-V bootstrap diode and independent inputs for the high-side and low-side outputs for maximum control flexibility. The high-side bias voltage is internally clamped at 5.2 V, which prevents the gate voltage from exceeding the maximum gate-source voltage rating of enhancement mode GaN FETs. The inputs of the device are TTL-logic compatible, which can withstand input voltages up to 14 V regardless of the VDD voltage. The LM5113-Q1 has split-gate outputs, providing flexibility to adjust the turnon and turnoff strength independently.

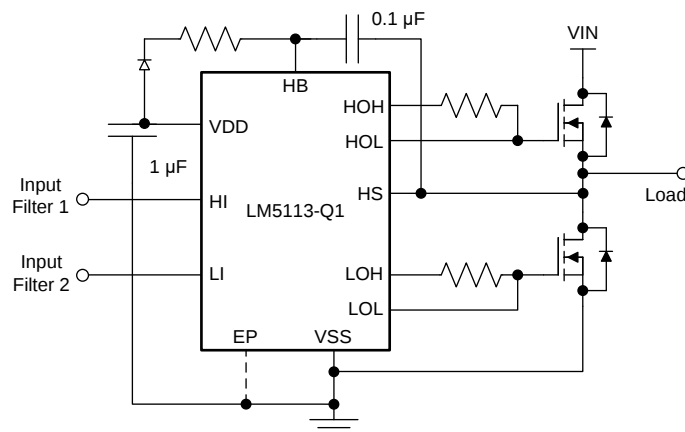
In addition, the strong sink capability of the LM5113-Q1 maintains the gate in the low state, preventing unintended turnon during switching. The LM5113-Q1 can operate up to several MHz. The LM5113-Q1 is available in a standard 10-pin WSON package with an exposed pad to aid power dissipation.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM5113-Q1	WSON (10)	4.00 mm × 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Application Diagram



Copyright © 2017, Texas Instruments Incorporated



Table of Contents

1 Features	1	7.4 Device Functional Modes.....	13
2 Applications	1	8 Application and Implementation	14
3 Description	1	8.1 Application Information.....	14
4 Revision History	2	8.2 Typical Application	15
5 Pin Configuration and Functions	3	9 Power Supply Recommendations	19
6 Specifications	4	10 Layout	20
6.1 Absolute Maximum Ratings	4	10.1 Layout Guidelines	20
6.2 ESD Ratings	4	10.2 Layout Example	20
6.3 Recommended Operating Conditions.....	4	11 Device and Documentation Support	21
6.4 Thermal Information	4	11.1 Documentation Support	21
6.5 Electrical Characteristics	5	11.2 Receiving Notification of Documentation Updates	21
6.6 Switching Characteristics	6	11.3 Community Resources.....	21
6.7 Typical Characteristics.....	8	11.4 Trademarks	21
7 Detailed Description	11	11.5 Electrostatic Discharge Caution.....	21
7.1 Overview	11	11.6 Glossary	21
7.2 Functional Block Diagram	11	12 Mechanical, Packaging, and Orderable	21
7.3 Feature Description.....	11	Information	21

4 Revision History

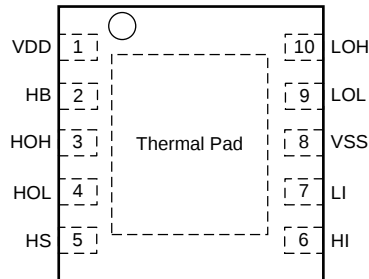
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (November 2017) to Revision B	Page
• Changed data sheet title from: LM5113-Q1 Automotive 90V, 1.2A/5A, Half Bridge GaN Driver to: LM5113-Q1 Automotive 90-V, 1.2-A, 5-A, Half Bridge GaN Driver.....	1
• Added input filter references to <i>Simplified Application Diagram</i>	1
• Added EXT HI and EXT LO references to the <i>Functional Block Diagram</i>	11
• Changed the last paragraph and add new images to the <i>Input and Output</i> section	11

Changes from Original (March 2017) to Revision A	Page
• Changed data sheet title from: LM5113-Q1 Automotive 80V, 1.2A/5A, Half Bridge GaN Driver to: LM5113-Q1 Automotive 90V, 1.2A/5A, Half Bridge GaN Driver	1
• Changed the <i>Simplified Application Diagram</i>	1
• Changed the <i>Functional Block Diagram</i>	11
• Added content to the <i>Input and Output</i> section.....	11
• Added content to the <i>Start-up and UVLO</i> section	12

5 Pin Configuration and Functions

DPR Package
10-Pin WSON With Exposed Thermal Pad
Top View



Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NO.	NAME		
1	VDD	P	5-V positive gate drive supply: locally decouple to VSS using low-ESR/ESL capacitor located as close as possible to the IC.
2	HB	P	High-side gate driver bootstrap rail: connect the positive terminal of the bootstrap capacitor to HB and the negative terminal to HS. The bootstrap capacitor must be placed as close to the IC as possible.
3	HOH	O	High-side gate driver turnon output: connect to the gate of high-side GaN FET with a short, low inductance path. A gate resistor can be used to adjust the turnon speed.
4	HOL	O	High-side gate driver turnoff output: connect to the gate of high-side GaN FET with a short, low inductance path. A gate resistor can be used to adjust the turnoff speed.
5	HS	P	High-side GaN FET source connection: connect to the bootstrap capacitor negative terminal and the source of the high-side GaN FET.
6	HI	I	High-side driver control input. The LM5113-Q1 inputs have TTL type thresholds. Unused inputs must be tied to ground and not left open.
7	LI	I	Low-side driver control input. The LM5113-Q1 inputs have TTL type thresholds. Unused inputs must be tied to ground and not left open.
8	VSS	G	Ground return: all signals are referenced to this ground.
9	LOL	O	Low-side gate driver sink-current output: connect to the gate of the low-side GaN FET with a short, low inductance path. A gate resistor can be used to adjust the turnoff speed.
10	LOH	O	Low-side gate driver source-current output: connect to the gate of high-side GaN FET with a short, low inductance path. A gate resistor can be used to adjust the turnon speed.
EP	—	—	Exposed pad: TI recommends that the exposed pad on the bottom of the package be soldered to ground plane on the printed-circuit board to aid thermal dissipation.

(1) I = Input, O = Output, G = Ground, P = Power

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

	MIN	MAX	UNIT
VDD to VSS	−0.3	7	V
HB to HS	−0.3	7	V
LI or HI input	−0.3	15	V
LOH, LOL output	−0.3	VDD + 0.3	V
HOH, HOL output	V _{HS} − 0.3	V _{HB} + 0.3	V
HS to VSS	−5	93	V
HB to VSS	0	100	V
Operating junction temperature		150	°C
Storage temperature, T _{stg}	−55	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

	VALUE	UNIT
V _(ESD) Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 ⁽¹⁾	±1000
	Charged-device model (CDM), per AEC Q100-011	±1500

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
VDD	4.5		5.5	V
LI or HI input	0		14	V
HS	−5		90	V
HB	V _{HS} + 4		V _{HS} + 5.5	V
HS slew rate			50	V/ns
Operating junction temperature	−40		125	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		LM5113-Q1	UNIT
		DPR (WSON)	
		10 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	37.5	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	35.8	°C/W
R _{θJB}	Junction-to-board thermal resistance	14.7	°C/W
ψ _{JT}	Junction-to-top characterization parameter	0.3	°C/W
ψ _{JB}	Junction-to-board characterization parameter	14.9	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	4.1	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

Specifications are $T_J = 25^\circ\text{C}$. Unless otherwise specified: $V_{DD} = V_{HB} = 5\text{ V}$, $V_{SS} = V_{HS} = 0\text{ V}$.
No load on LOL and HOL or HOH and HOL⁽¹⁾.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY CURRENTS							
I _{DD}	VDD quiescent current	LI = HI = 0 V	T _J = 25°C	0.07		mA	
			T _J = −40°C to 125°C	0.1			
I _{DDO}	VDD operating current	f = 500 kHz	T _J = 25°C	2		mA	
			T _J = −40°C to 125°C	3			
I _{HB}	Total HB quiescent current	LI = HI = 0 V	T _J = 25°C	0.08		mA	
			T _J = −40°C to 125°C	0.1			
I _{HBO}	Total HB operating current	f = 500 kHz	T _J = 25°C	1.5		mA	
			T _J = −40°C to 125°C	2.5			
I _{HBS}	HB to VSS quiescent current	HS = HB = 90 V	T _J = 25°C	0.1		μA	
			T _J = −40°C to 125°C	10			
I _{HBSO}	HB to VSS operating current	f = 500 kHz	T _J = 25°C	0.4		mA	
			T _J = −40°C to 125°C	1			
INPUT PINS							
V _{IR}	Input voltage threshold	Rising edge	T _J = 25°C	2.06		V	
			T _J = −40°C to 125°C	1.89	2.18		
V _{IF}	Input voltage threshold	Falling edge	T _J = 25°C	1.66		V	
			T _J = −40°C to 125°C	1.48	1.76		
V _{IHYS}	Input voltage hysteresis			400		mV	
R _I	Input pulldown resistance	T _J = 25°C		200		kΩ	
		T _J = −40°C to 125°C	100	300			
UNDERVOLTAGE PROTECTION							
V _{DDR}	VDD rising threshold	T _J = 25°C		3.8		V	
		T _J = −40°C to 125°C	3.2	4.5			
V _{DDH}	VDD threshold hysteresis			0.2		V	
V _{HBR}	HB rising threshold	T _J = 25°C		3.2		V	
		T _J = −40°C to 125°C	2.5	3.9			
V _{HBH}	HB threshold hysteresis			0.2		V	
BOOTSTRAP DIODE							
V _{DL}	Low-current forward voltage	I _{VDD-HB} = 100 μA	T _J = 25°C	0.45		V	
			T _J = −40°C to 125°C	0.65			
V _{DH}	High-current forward voltage	I _{VDD-HB} = 100 mA	T _J = 25°C	0.90		V	
			T _J = −40°C to 125°C	1			
R _D	Dynamic resistance	I _{VDD-HB} = 100 mA	T _J = 25°C	1.85		Ω	
			T _J = −40°C to 125°C	3.60			
	HB-HS clamp regulation voltage		T _J = 25°C	5.2		V	
			T _J = −40°C to 125°C	4.7	5.45		

(1) Parameters that show only a typical value are ensured by design and may not be tested in production.

LM5113-Q1

SNVSAR1B – MARCH 2017 – REVISED MARCH 2018

www.ti.com
Electrical Characteristics (continued)

Specifications are $T_J = 25^\circ\text{C}$. Unless otherwise specified: $V_{DD} = V_{HB} = 5\text{ V}$, $V_{SS} = V_{HS} = 0\text{ V}$.
No load on LOL and HOL or HOH and HOL⁽¹⁾.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
LOW- AND HIGH-SIDE GATE DRIVER							
V _{OL}	Low-level output voltage	I _{HOL} = I _{LOL} = 100 mA	T _J = 25°C	0.06		0.10	V
			T _J = −40°C to 125°C				
V _{OH}	High-level output voltage V _{OH} = V _{DD} − LOH or V _{OH} = HB − HOH	I _{HOH} = I _{LOH} = 100 mA	T _J = 25°C	0.21		0.31	V
			T _J = −40°C to 125°C				
I _{OHL}	Peak source current	HOH, LOH = 0 V		1.2			A
I _{OLL}	Peak sink current	HOL, LOL = 5 V		5			A
I _{OHLK}	High-level output leakage current	HOH, LOH = 0 V	T _J = −40°C to 125°C	1.5			μA
I _{OLLK}	Low-level output leakage current	HOL, LOL = 5 V	T _J = −40°C to 125°C	1.5			μA

6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{LPHL}	LO turnoff propagation delay	LI falling to LOL falling	$T_J = 25^\circ\text{C}$		26.5		ns
			$T_J = -40^\circ\text{C to } 125^\circ\text{C}$			45	
t_{LPLH}	LO turnon propagation delay	LI rising to LOH rising	$T_J = 25^\circ\text{C}$		28.0		ns
			$T_J = -40^\circ\text{C to } 125^\circ\text{C}$			45	
t_{HPHL}	HO turnoff propagation delay	HI falling to HOL falling	$T_J = 25^\circ\text{C}$		26.5		ns
			$T_J = -40^\circ\text{C to } 125^\circ\text{C}$			45	
t_{HPLH}	HO turnon propagation delay	HI rising to HOH rising	$T_J = 25^\circ\text{C}$		28		ns
			$T_J = -40^\circ\text{C to } 125^\circ\text{C}$			45.0	
t_{MON}	Delay matching LO on and HO off	$T_J = 25^\circ\text{C}$			1.5		ns
		$T_J = -40^\circ\text{C to } 125^\circ\text{C}$				8	
t_{MOFF}	Delay matching LO off and HO on	$T_J = 25^\circ\text{C}$			1.5		ns
		$T_J = -40^\circ\text{C to } 125^\circ\text{C}$				8	
t_{HRC}	HO rise time (0.5 V – 4.5 V)	$C_L = 1000\text{ pF}$			7		ns
t_{LRC}	LO rise time (0.5 V – 4.5 V)	$C_L = 1000\text{ pF}$			7		ns
t_{HFC}	HO fall time (0.5 V – 4.5 V)	$C_L = 1000\text{ pF}$			3.5		ns
t_{LFC}	LO fall time (0.5 V – 4.5 V)	$C_L = 1000\text{ pF}$			3.5		ns
t_{PW}	Minimum input pulse width that changes the output				10		ns
t_{BS}	Bootstrap diode reverse recovery time	$I_F = 100\text{ mA}$, $I_R = 100\text{ mA}$			40		ns

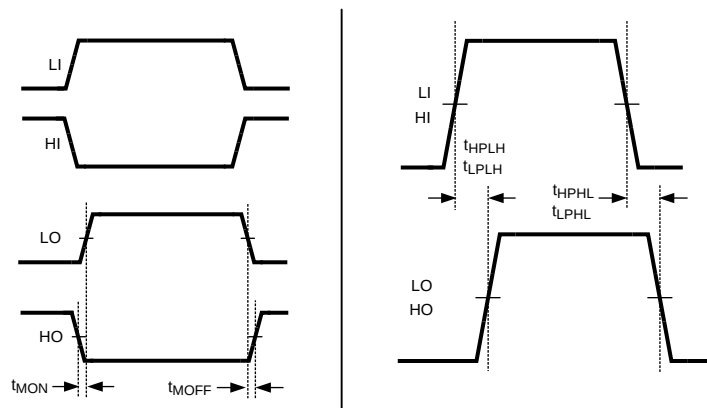


Figure 1. Timing Diagram

6.7 Typical Characteristics

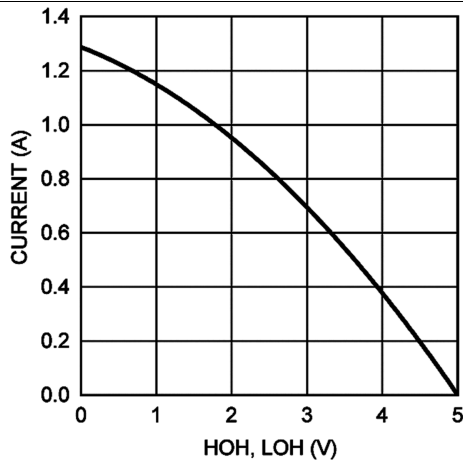


Figure 2. Peak Source Current vs Output Voltage

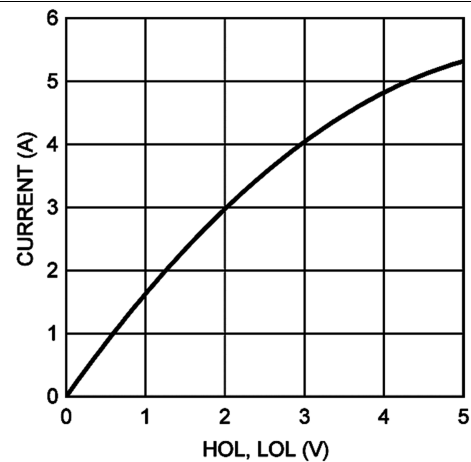
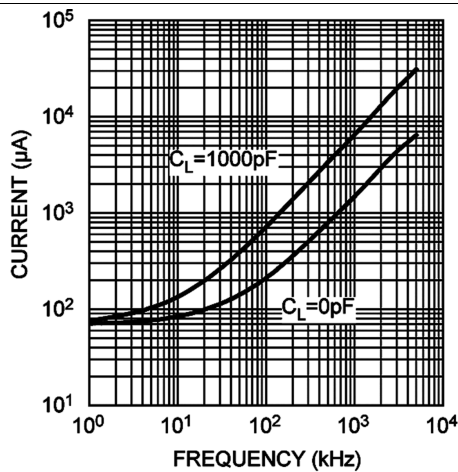
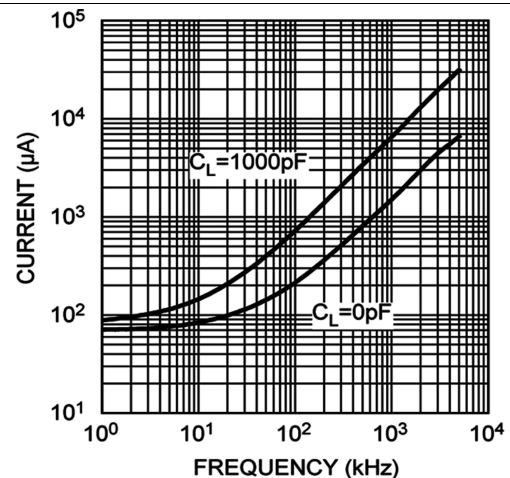
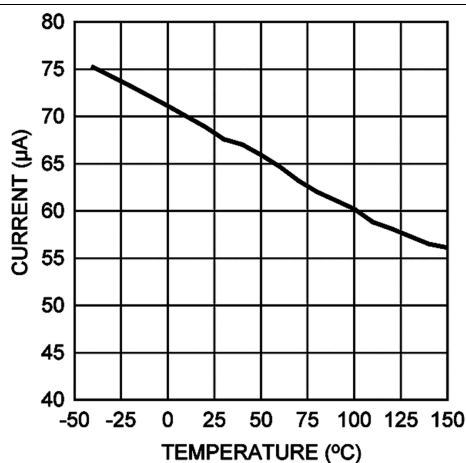
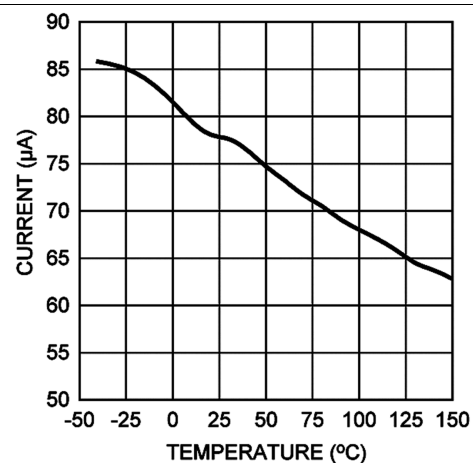


Figure 3. Peak Sink Current vs Output Voltage


 Figure 4. I_{DD} vs Frequency

 Figure 5. I_{HBO} vs Frequency

 Figure 6. I_{DD} vs Temperature

 Figure 7. I_{HB} vs Temperature

Typical Characteristics (continued)

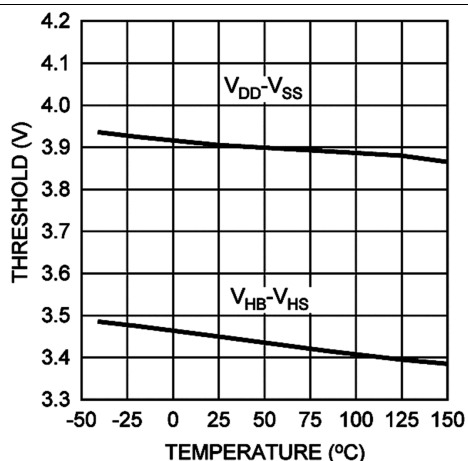


Figure 8. UVLO Rising Thresholds vs Temperature

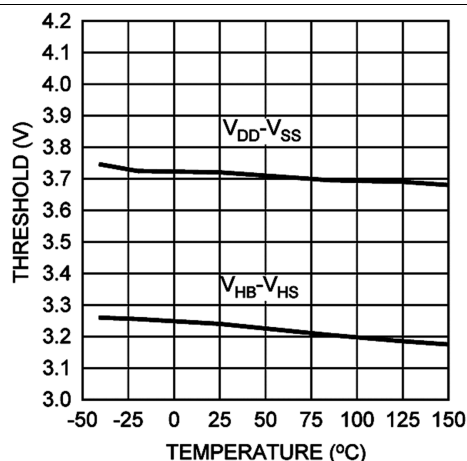


Figure 9. UVLO Falling Thresholds vs Temperature

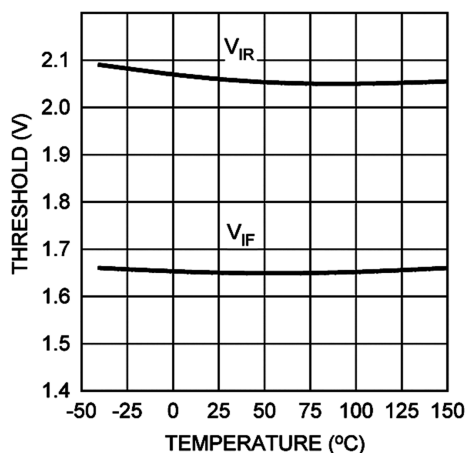


Figure 10. Input Thresholds vs Temperature

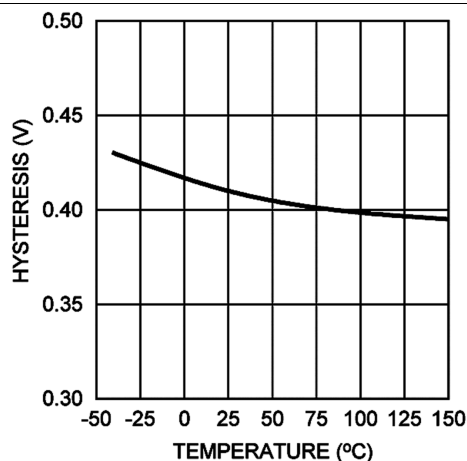


Figure 11. Input Threshold Hysteresis vs Temperature

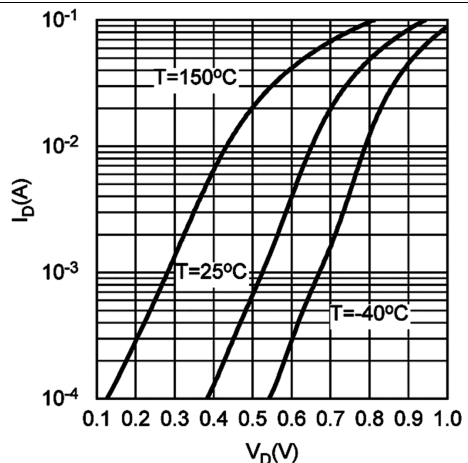


Figure 12. Bootstrap Diode Forward Voltage

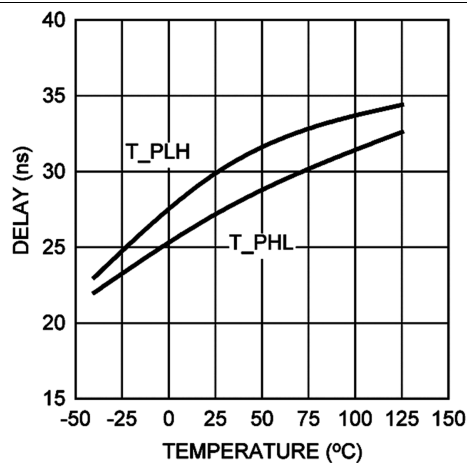
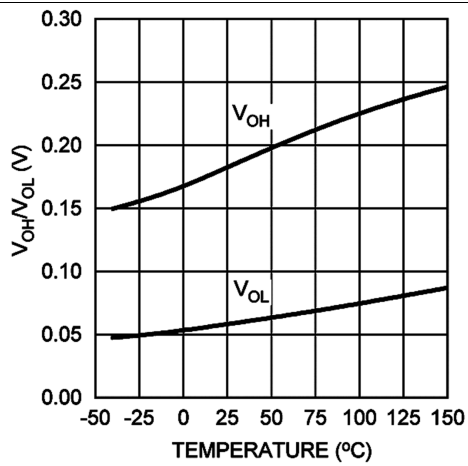


Figure 13. Propagation Delay vs Temperature

Typical Characteristics (continued)


Note: Unless otherwise specified, $V_{DD} = V_{HB} = 5\text{ V}$,
 $V_{SS} = V_{HS} = 0\text{ V}$.

Figure 14. LO and HO Gate Drive – High/Low Level Output Voltage vs Temperature

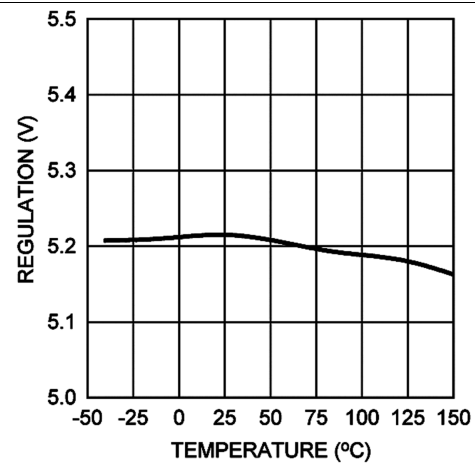


Figure 15. HB Regulation Voltage vs Temperature

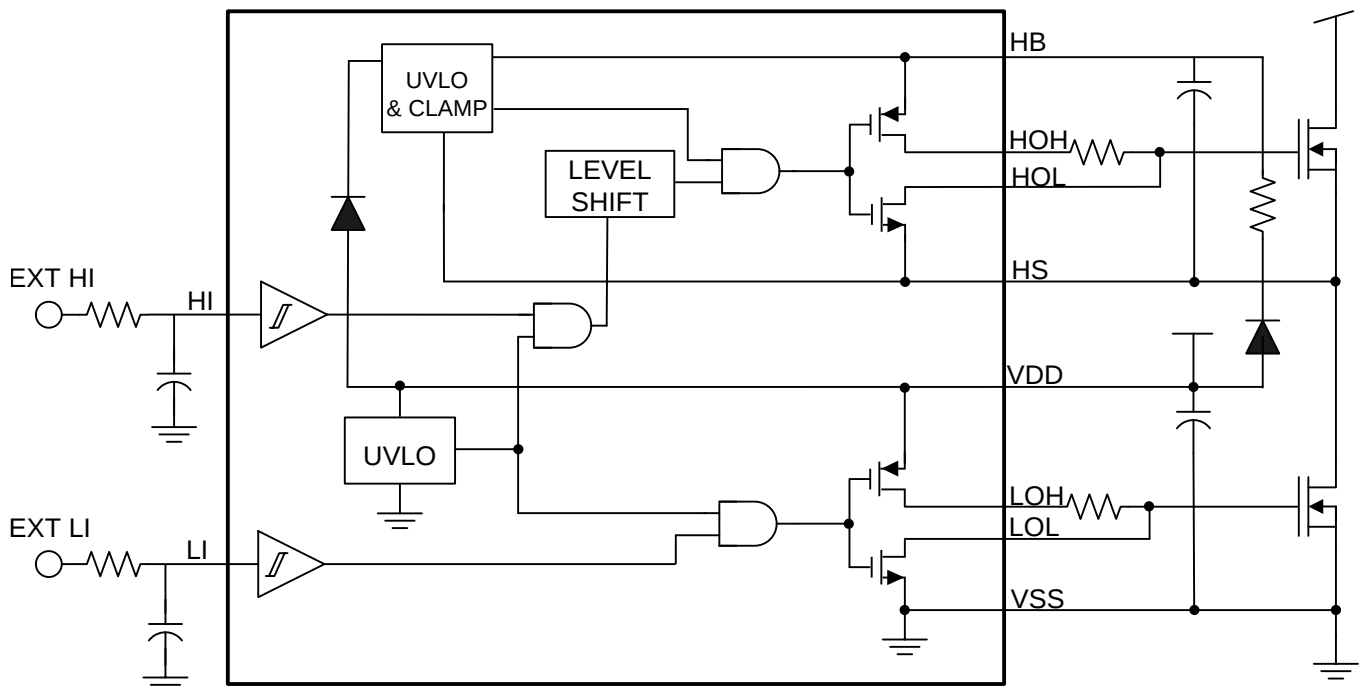
7 Detailed Description

7.1 Overview

The LM5113-Q1 is a high-frequency, high- and low- side gate driver for enhancement mode Gallium Nitride (GaN) FETs in a synchronous buck, boost, or half bridge configuration. The high-side bias voltage is generated using a bootstrap technique and is internally clamped at 5.2 V, which prevents the gate voltage from exceeding the maximum gate-source voltage rating of enhancement mode GaN FETs. The LM5113-Q1 has split-gate outputs with strong sink capability, providing flexibility to adjust the turnon and turnoff strength independently.

The LM5113-Q1 can operate up to several MHz, and is available in a standard 10-pin WSON package that contains an exposed pad to aid power dissipation.

7.2 Functional Block Diagram



Copyright © 2017, Texas Instruments Incorporated

7.3 Feature Description

7.3.1 Input and Output

The input pins of the LM5113-Q1 are independently controlled with TTL input thresholds and can withstand voltages up to 12 V regardless of the VDD voltage. This allows the inputs to be directly connected to the outputs of an analog PWM controller with up to 12-V power supply, eliminating the need for a buffer stage.

The output pulldown and pullup resistance of LM5113-Q1 is optimized for enhancement mode GaN FETs to achieve high frequency and efficient operation. The 0.6-Ω pulldown resistance provides a robust low impedance turnoff path necessary to eliminate undesired turnon induced by high dv/dt or high di/dt. The 2.1-Ω pullup resistance helps reduce the ringing and over-shoot of the switch node voltage. The split outputs of the LM5113-Q1 offer flexibility to adjust the turnon and turnoff speed by independently adding additional impedance in either the turnon path, the turnoff path, or both.

If the input signal for either of the two channels, HI or LI, is not used, the control pin must be tied to either VDD or VSS. These inputs must not be left floating.

Feature Description (continued)

Additionally, the input signals avoid pulses shorter than 3 ns by using the input filter to the HI and LI input pins. The values and part numbers of the circuit components are shown in the [Figure 16](#).

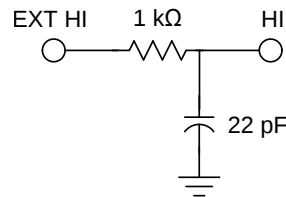
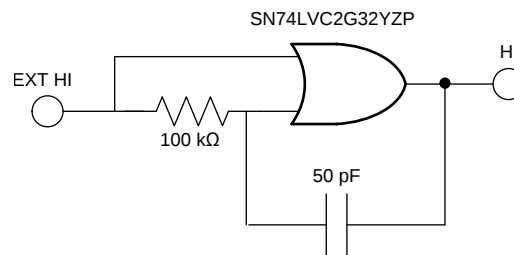


Figure 16. Input Filter 1 (High-Side Input Filter)

If short pulses or short delays are required, the circuit in [Figure 17](#) is recommended.



Copyright © 2017, Texas Instruments Incorporated

Figure 17. Input Filter 1 for Short Pulses (High-Side Input Filter)

7.3.2 Start-Up and UVLO

The LM5113-Q1 has an undervoltage lockout (UVLO) on both the VDD and bootstrap supplies. When the VDD voltage is below the threshold voltage of 3.8 V, both the HI and LI inputs are ignored to prevent the GaN FETs from being partially turned on. Also, if there is insufficient VDD voltage, the UVLO actively pulls the LOL and HOL low. When the VDD voltage is above its UVLO threshold, but the HB to HS bootstrap voltage is below the UVLO threshold of 3.2 V, only HOL is pulled low. Both UVLO threshold voltages have 200 mV of hysteresis to avoid chattering.

The startup voltage sequencing for this device is as follows: VDD voltage first, with the VIN voltage present thereafter.

The LM5113-Q1 requires an external bootstrap diode with a 100 Ω series resistor from VDD to HB to charge the high side supply on a cycle by cycle basis. The recommended bootstrap diode options are BAT46, BAT41, or LL4148.

Table 1. VDD UVLO Feature Logic Operation

CONDITION ($V_{HB-HS} > V_{HBR}$ for all cases below)	HI	LI	HO	LO
$V_{DD} - V_{SS} < V_{DDR}$ during device start-up	H	L	L	L
$V_{DD} - V_{SS} < V_{DDR}$ during device start-up	L	H	L	L
$V_{DD} - V_{SS} < V_{DDR}$ during device start-up	H	H	L	L
$V_{DD} - V_{SS} < V_{DDR}$ during device start-up	L	L	L	L
$V_{DD} - V_{SS} < V_{DDR} - V_{DDH}$ after device start-up	H	L	L	L
$V_{DD} - V_{SS} < V_{DDR} - V_{DDH}$ after device start-up	L	H	L	L
$V_{DD} - V_{SS} < V_{DDR} - V_{DDH}$ after device start-up	H	H	L	L
$V_{DD} - V_{SS} < V_{DDR} - V_{DDH}$ after device start-up	L	L	L	L

Table 2. V_{HB-HS} UVLO Feature Logic Operation

CONDITION ($V_{DD} > V_{DDR}$ for all cases below)	HI	LI	HO	LO
$V_{HB-HS} < V_{HBR}$ during device start-up	H	L	L	L
$V_{HB-HS} < V_{HBR}$ during device start-up	L	H	L	H
$V_{HB-HS} < V_{HBR}$ during device start-up	H	H	L	H
$V_{HB-HS} < V_{HBR}$ during device start-up	L	L	L	L
$V_{HB-HS} < V_{HBR} - V_{HBH}$ after device start-up	H	L	L	L
$V_{HB-HS} < V_{HBR} - V_{HBH}$ after device start-up	L	H	L	H
$V_{HB-HS} < V_{HBR} - V_{HBH}$ after device start-up	H	H	L	H
$V_{HB-HS} < V_{HBR} - V_{HBH}$ after device start-up	L	L	L	L

7.3.3 HS Negative Voltage and Bootstrap Supply Voltage Clamping

Due to the intrinsic nature of enhancement mode GaN FETs, the source-to-drain voltage of the bottom switch is usually higher than a diode forward voltage drop when the gate is pulled low. This causes negative voltage on HS pin. Moreover, this negative voltage transient may become even more pronounced due to the effects of board layout and device drain/source parasitic inductances. With high-side driver using the floating bootstrap configuration, negative HS voltage can lead to an excessive bootstrap voltage, which can damage the high-side GaN FET. The LM5113-Q1 solves this problem with an internal clamping circuit that prevents the bootstrap voltage from exceeding 5.2 V typical.

7.3.4 Level Shift

The level-shift circuit is the interface from the high-side input to the high-side driver stage, which is referenced to the switch node (HS). The level shift allows control of the HO output, which is referenced to the HS pin and provides excellent delay matching with the low-side driver. Typical delay matching between LO and HO is around 1.5 ns.

7.4 Device Functional Modes

Table 3 shows the device truth table.

Table 3. Truth Table

HI	LI	HOH	HOL	LOH	LOL
L	L	Open	L	Open	L
L	H	Open	L	H	Open
H	L	H	Open	Open	L
H	H	H	Open	H	Open

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

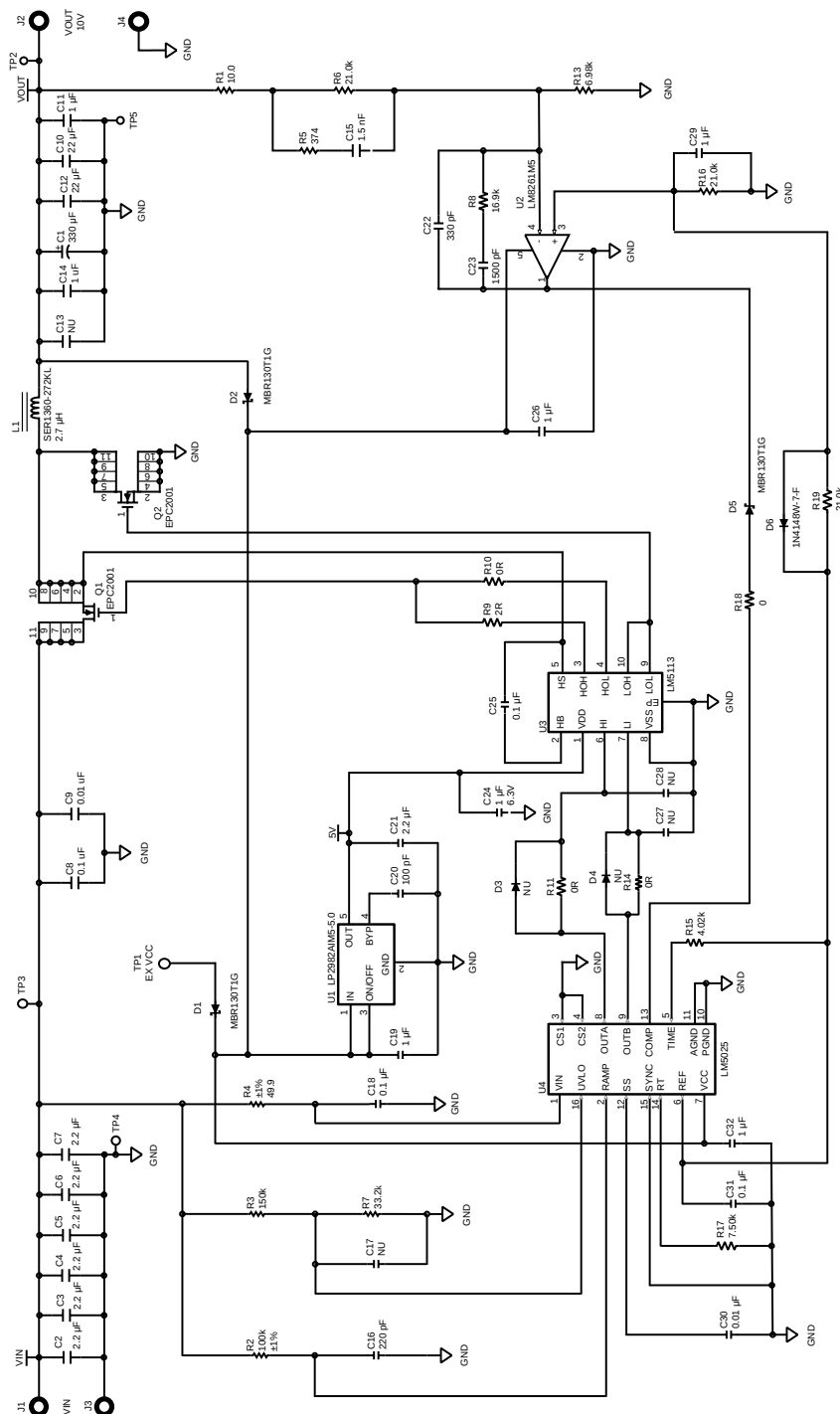
8.1 Application Information

To operate GaN transistors at very high switching frequencies and to reduce associated switching losses, a powerful gate driver is employed between the PWM output of controller and the gates of the GaN transistor. Also, gate drivers are indispensable when the outputs of the PWM controller do not meet the voltage or current levels needed to directly drive the gates of the switching devices. With the advent of digital power, this situation is often encountered because the PWM signal from the digital controller is often a 3.3-V logic signal, which cannot effectively turn on a power switch. A level-shift circuit is needed to boost the 3.3-V signal to the gate-drive voltage (such as 12 V) to fully turn on the power device and minimize conduction losses. Traditional buffer-drive circuits based on NPN/PNP bipolar transistors in totem-pole arrangement prove inadequate with digital power because they lack level-shifting capability. Gate drivers effectively combine both the level-shifting and buffer-drive functions. Gate drivers also address other needs such as minimizing the effect of high-frequency switching noise (by placing the high-current driver IC physically close to the power switch), driving gate-drive transformers and controlling floating power-device gates, reducing power dissipation and thermal stress in controllers by moving gate-charge power losses from the controller into the driver.

The LM5113-Q1 is a MHz high- and low-side gate driver for enhancement mode GaN FETs in a synchronous buck, boost, or half-bridge configuration. The high-side bias voltage is generated using a bootstrap technique and is internally clamped at 5.2 V, which prevents the gate voltage from exceeding the maximum gate-source voltage rating of enhancement mode GaN FETs. The LM5113-Q1 has split gate outputs with strong sink capability, providing flexibility to adjust the turnon and turnoff strength independently.

8.2 Typical Application

The circuit in [Figure 18](#) shows a synchronous buck converter to evaluate the LM5113-Q1 device. Detailed synchronous buck converter specifications are listed in [Design Requirements](#). The active clamping voltage mode controller LM5025 is used for close-loop control and generates the PWM signals of the buck switch and the synchronous switch. For more information, see [Figure 18](#).



Input 15 V to 60 V, output 10 V, 800 kHz

Figure 18. LP5113-Q1 Application Circuit

Typical Application (continued)

8.2.1 Design Requirements

Table 4 lists the design requirements for the typical application.

Table 4. Design Parameters

PARAMETER	SPECIFICATION
Input operating range	15 – 60 V
Output voltage	10 V
Output current, 48-V input	10 A
Output current, 60-V input	7 A
Efficiency at 48 V, 10 A	>90%
Frequency	800 kHz

8.2.2 Detailed Design Procedure

This procedure outlines the design considerations of LM5113-Q1 in a synchronous buck converter with enhancement mode GaN FET. Refer to Figure 18 for component names and network locations. For additional design help, see Figure 18.

8.2.2.1 VDD Bypass Capacitor

The VDD bypass capacitor provides the gate charge for the low-side and high-side transistors and to absorb the reverse recovery charge of the bootstrap diode. The required bypass capacitance can be calculated with Equation 1.

$$C_{VDD} > \frac{Q_{gH} + Q_{gL} + Q_{rr}}{\Delta V}$$

where

- Q_{gH} and Q_{gL} are gate charge of the high-side and low-side transistors, respectively.
- Q_{rr} is the reverse recovery charge of the bootstrap diode, which is typically around 4 nC.
- ΔV is the maximum allowable voltage drop across the bypass capacitor. (1)

TI recommends a 0.1-μF or larger value, good quality, ceramic capacitor. The bypass capacitor must be placed as close as possible to the pins of the IC to minimize the parasitic inductance.

8.2.2.2 Bootstrap Capacitor

The bootstrap capacitor provides the gate charge for the high-side switch, DC bias power for HB UVLO circuit, and the reverse recovery charge of the bootstrap diode. The required bypass capacitance can be calculated with Equation 2.

$$C_{BST} > \frac{Q_{gH} + I_{HB} \times t_{ON} + Q_{rr}}{\Delta V}$$

where

- I_{HB} is the quiescent current of the high-side driver.
- t_{on} is the maximum on-time period of the high-side transistor. (2)

A good-quality, ceramic capacitor must be used for the bootstrap capacitor. TI recommends placement of the bootstrap capacitor as close as possible to the HB and HS pin.

8.2.2.3 Power Dissipation

The power consumption of the driver is an important measure that determines the maximum achievable operating frequency of the driver. It must be kept below the maximum power-dissipation limit of the package at the operating temperature. The total power dissipation of the LM5113-Q1 is the sum of the gate driver losses and the bootstrap diode power loss.

The gate driver losses are incurred by charge and discharge of the capacitive load. It can be approximated as:

$$P = (C_{\text{LoadH}} + C_{\text{LoadL}}) \times V_{\text{DD}}^2 \times f_{\text{SW}}$$

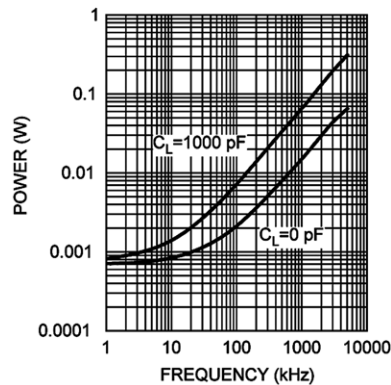
where

- C_{LoadH} and C_{LoadL} are the high-side and the low-side capacitive loads, respectively. (3)

It can also be calculated with the total input gate charge of the high-side and the low-side transistors as:

$$P = (Q_{\text{gH}} + Q_{\text{gL}}) \times V_{\text{DD}} \times f_{\text{SW}} \quad (4)$$

There are some additional losses in the gate drivers due to the internal CMOS stages used to buffer the LO and HO outputs. Figure 19 shows the measured gate-driver power dissipation versus frequency and load capacitance. At higher frequencies and load capacitance values, the power dissipation is dominated by the power losses driving the output loads and agrees well with the above equations. This plot can be used to approximate the power losses due to the gate drivers.



Gate-driver power dissipation (LO+HO), VDD = +5 V

Figure 19. Neglecting Bootstrap Diode Losses

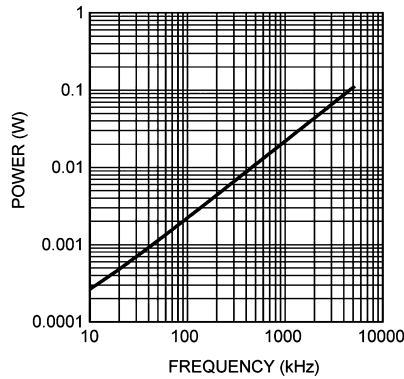
The bootstrap diode power loss is the sum of the forward bias power loss that occurs while charging the bootstrap capacitor and the reverse bias power loss that occurs during reverse recovery. Because each of these events happens once per cycle, the diode power loss is proportional to the operating frequency. Larger capacitive loads require more energy to recharge the bootstrap capacitor resulting in more losses. Higher input voltages (V_{IN}) to the half bridge also result in higher reverse recovery losses.

Figure 20 and Figure 21 show the forward bias power loss and the reverse bias power loss of the bootstrap diode, respectively. The plots are generated based on calculations and lab measurements of the diode reverse time and current under several operating conditions. The plots can be used to predict the bootstrap diode power loss under different operating conditions.

LM5113-Q1

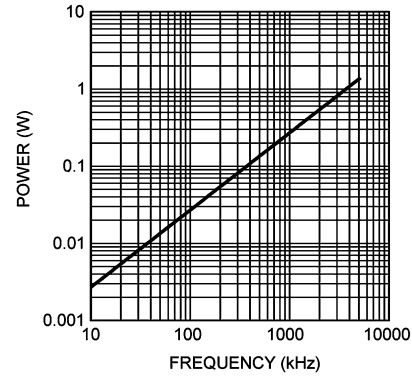
SNVSAR1B – MARCH 2017 – REVISED MARCH 2018

www.ti.com



The load of high-side driver is a GaN FET with total gate charge of 10 nC.

Figure 20. Forward Bias Power Loss of Bootstrap Diode $V_{IN} = 50$ V



The load of high-side driver is a GaN FET with total gate charge of 10 nC.

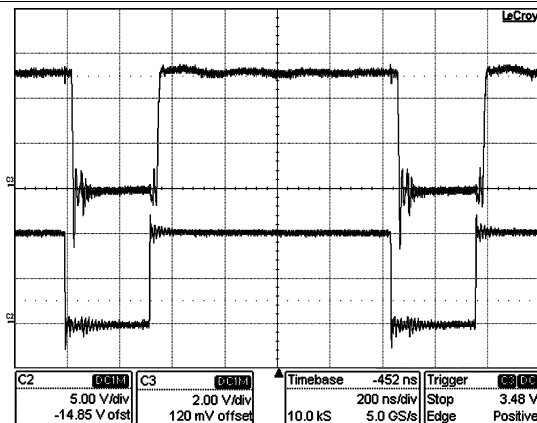
Figure 21. Reverse Recovery Power Loss of Bootstrap Diode $V_{IN} = 50$ V

The sum of the driver loss and the bootstrap diode loss is the total power loss of the IC. For a given ambient temperature, the maximum allowable power loss of the IC can be defined as [Equation 5](#).

$$P = \frac{(T_J - T_A)}{\theta_{JA}}$$

(5)

8.2.3 Application Curves



Conditions:

Input Voltage = 48 V DC, Load Current = 5 A

Traces:

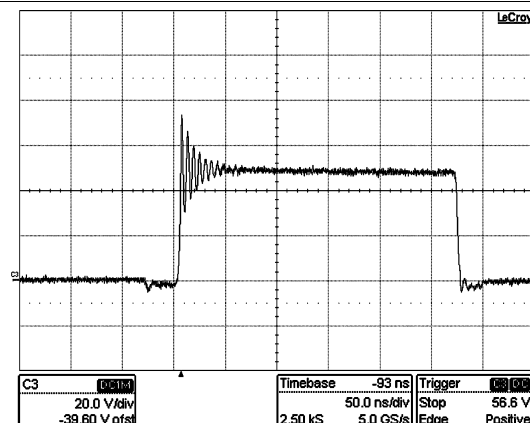
Top Trace: Gate of Low-Side eGaN FET, Volt/div = 2 V

Bottom Trace: LI of LM5113-Q1, Volt/div = 5 V

Bandwidth Limit = 600 MHz

Horizontal Resolution = 0.2 μ s/div

Figure 22. Low-Side Driver Input and Output



Conditions:

Input Voltage = 48 V DC,

Load Current = 10 A

Traces:

Trace: Switch-Node Voltage, Volts/div = 20 V

Bandwidth Limit = 600 MHz

Horizontal Resolution = 50 ns/div

Figure 23. Switch-Node Voltage

9 Power Supply Recommendations

The recommended bias supply voltage range for LM5113-Q1 is from 4.5 V to 5.5 V. The lower end of this range is governed by the internal undervoltage lockout (UVLO) protection feature of the VDD supply circuit. TI recommends keeping proper margin to allow for transient voltage spikes while not violating the LM5113-Q1 absolute maximum VDD voltage rating and the GaN transistor gate breakdown voltage limit.

The UVLO protection feature also involves a hysteresis function. This means that once the device is operating in normal mode, if the VDD voltage drops, the device continues to operate in normal mode as far as the voltage drop does not exceed the hysteresis specification, VDDH. If the voltage drop is more than hysteresis specification, the device shuts down. Therefore, while operating at or near the 4.5-V range, the voltage ripple on the VDD power supply output must be smaller than the hysteresis specification of LM5113-Q1 UVLO to avoid triggering device shutdown.

A local bypass capacitor must be placed between the VDD and VSS pins. This capacitor must be located as close as possible to the device. A low-ESR, ceramic surface-mount capacitor is recommended. TI recommends using 2 capacitors across VDD and GND: a 100-nF ceramic surface-mount capacitor for high frequency filtering placed very close to VDD and GND pin, and another surface-mount capacitor, 220-nF to 10- μ F, for IC bias requirements.

10 Layout

10.1 Layout Guidelines

Small gate capacitance and miller capacitance enable enhancement mode GaN FETs to operate with fast switching speed. The induced high dv/dt and di/dt , coupled with a low gate-threshold voltage and limited headroom of enhancement mode GaN FETs gate voltage, make the circuit layout crucial to the optimum performance. Following are some recommendations.

1. The first priority in designing the layout of the driver is to confine the high peak currents that charge and discharge the GaN FETs gate into a minimal physical area. This decreases the loop inductance and minimize noise issues on the gate terminal of the GaN FETs. The GaN FETs must be placed close to the driver.
2. The second high current path includes the bootstrap capacitor, the local ground referenced VDD bypass capacitor, and low-side GaN FET. The bootstrap capacitor is recharged on a cycle-by-cycle basis through the bootstrap diode from the ground referenced VDD capacitor. The recharging occurs in a short time interval and involves high peak current. Minimizing this loop length and area on the circuit board is important to ensure reliable operation.
3. The parasitic inductance in series with the source of the high-side FET and the low-side FET can impose excessive negative voltage transients on the driver. TI recommends connecting the HS pin and VSS pin to the respective source of the high-side and low-side transistors with a short and low-inductance path.
4. The parasitic source inductance, along with the gate capacitor and the driver pulldown path, can form an LCR resonant tank, resulting in gate voltage oscillations. An optional resistor or ferrite bead can be used to damp the ringing.
5. Low ESR/ESL capacitors must be connected close to the IC, between VDD and VSS pins and between the HB and HS pins to support the high peak current being drawn from VDD during turnon of the FETs. Keeping guideline number 1 above (minimized GaN FETs gate driver loop) as the first priority, it is also desirable to place the VDD decoupling capacitor and the HB to HS bootstrap capacitor on the same side of the PC board as the driver. The inductance of vias can impose excessive ringing on the IC pins.
6. To prevent excessive ringing on the input power bus, good decoupling practices are required by placing low-ESR ceramic capacitors adjacent to the GaN FETs.

Figure 24 and Figure 25 show recommended layout patterns for the 10-pin WSON package. Two cases are considered: (1) Without any gate resistors, and (2) with an optional turnon gate resistor. Note that 0402 surface mount package is assumed for the passive components in Figure 24 and Figure 25.

10.2 Layout Example

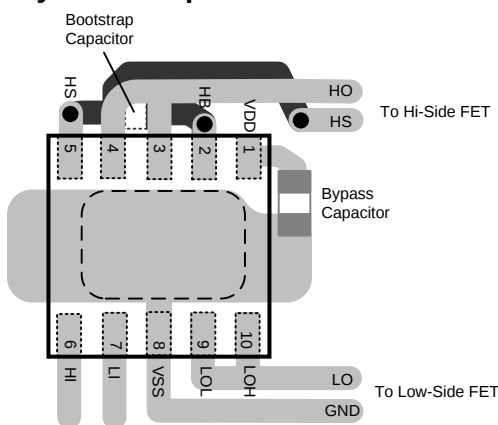


Figure 24. 10-Pin WSON Without Gate Resistors

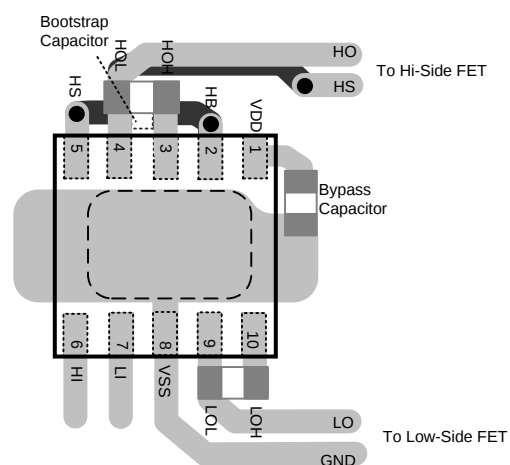


Figure 25. 10-Pin WSON With HOH and LOH Gate Resistors

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see:

[AN-2149 LM5113 Evaluation Board](#) (SNVA484)

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this datasheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM5113QDPRRQ1	ACTIVE	WSO	DPR	10	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L5113Q	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF LM5113-Q1 :

-
- Catalog: [LM5113](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM5113QDPRRQ1	WSO	DPR	10	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

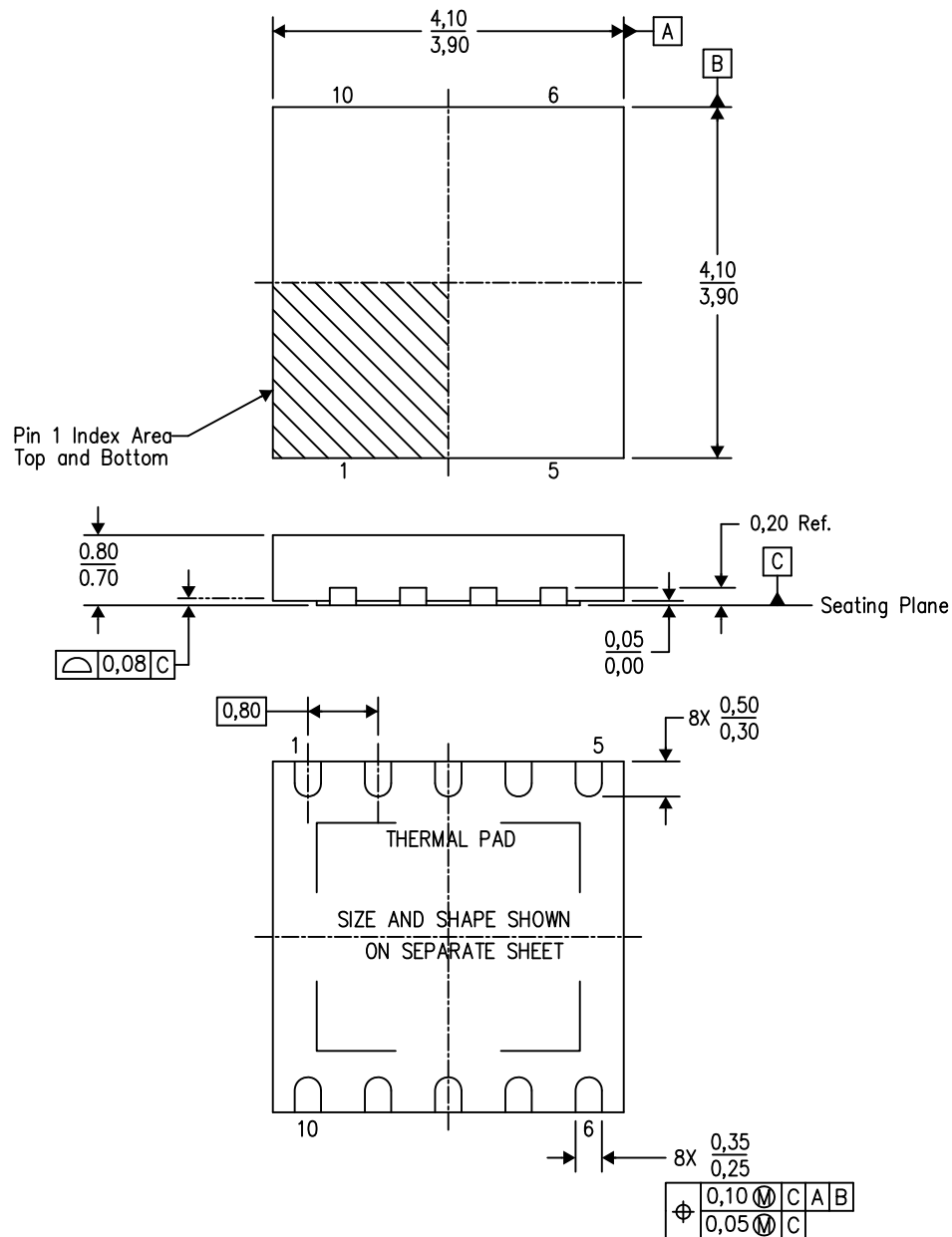


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM5113QDPRRQ1	WSO8	DPR	10	4500	367.0	367.0	35.0

DPR (S-PWSON-N10)

PLASTIC SMALL OUTLINE NO-LEAD



4211532/B 04/12

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - SON (Small Outline No-Lead) package configuration.
 - The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.