National Semiconductor

LM1525A/LM3525A/LM1527A/LM3527A Pulse Width Modulator

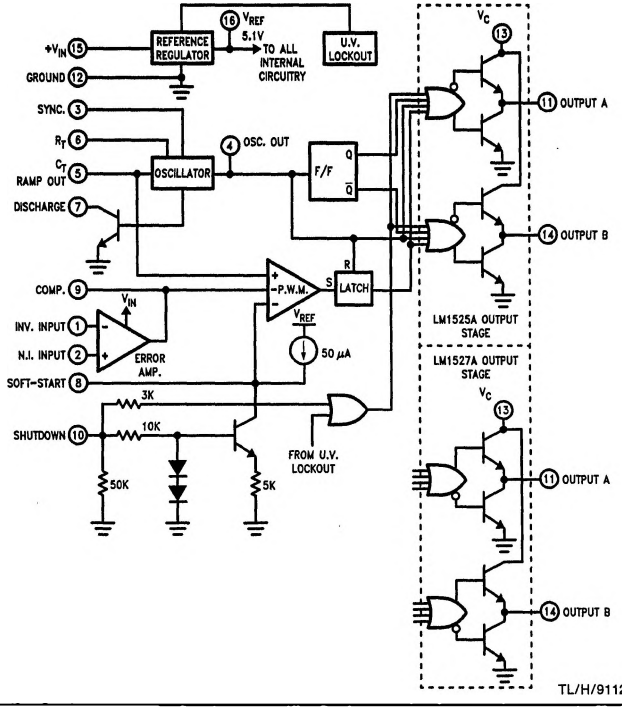
General Description

The LM1525A/1527A series of pulse-width-modulator integrated circuits are designed to offer improved performance and lowered external parts count when used to implement all types of switching power supplies. The on-chip +5.1V reference is trimmed to ±1% initial accuracy, and the input common mode range of the error amplifier includes the reference voltage, eliminating external potentiometers and dividers. A Sync input to the oscillator permits multiple devices to be slaved together, or a single device to be synchronized to an external system clock. A single resistor between the C_T pin and the Discharge pin provides a wide range of deadtime adjustment. These devices also feature built-in soft-start circuitry with only a timing capacitor required externally. A Shutdown pin controls both the soft-start circuitry and the output stages, providing instantaneous turn-off with soft-start recycle for slow turn-on. These functions are also controlled by an undervoltage lockout which keeps the outputs off and the soft-start capacitor discharged for input voltages less than that required for normal operation. The undervoltage lockout circuitry features approximately 200 mV of hysteresis to prevent threshold oscillations. Another unique feature of these improved PWM integrated circuits is the latch following the comparator (thus preventing double-pulsing). Once a PWM pulse has been terminated for any reason, the outputs will remain OFF for the duration of that period. The latch is reset with each clock pulse. The output stages are totem-pole designs capable of sourcing or sinking more than 200 mA. The LM1525A output stage features NOR logic, resulting in LOW outputs for an OFF stage. The LM1527A uses OR logic which results in HIGH outputs when OFF.

Features

- 8 to 35V operation
- 5.1V reference trimmed to ±1%
- 100 Hz to 500 kHz oscillator range
- Separate oscillator sync terminal
- Adjustable deadtime control
- Internal soft-start
- Input undervoltage lockout with hysteresis
- Latching P.W.M. to prevent multiple pulses
- Dual source/sink output drivers

Block & Connection Diagrams



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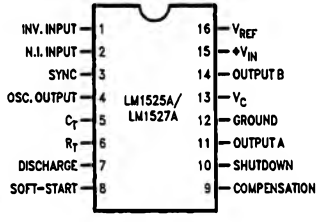

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Top View

Order Number LM1525AJ, LM3525AJ, LM1527AJ, LM3527AJ, LM3525AN or LM3527AN
See NS Package Number J16A or N16A

Absolute Maximum Ratings (Note 7)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Input Voltage (Pins 13, and 15)	−0.3V to +40V
Reference Output Current (Pin 16)	50 mA DC
Reference Output Short Circuit	5 Seconds
Output Current (Pins 11, 14)	±200 mA
Oscillator Current (Pins 5, 6, 7) (Note 8)	5 mA DC
Op Amp Inputs: V_{CM} (Pins 1, 2) V_{DIFF}	−0.3V to +V_{in} ±6V
Logic Inputs	−0.3V to +5.5V
Storage Temperature	−65°C to +150°C
Operating Temperature Range ($T_{min} \le T_j \le T_{max}$)	
LM1525A, LM1527A	−55°C to +150°C
LM3525A, LM3527A	0°C to +150°C
Lead Temperature (Soldering, 4 Seconds)	
J Package	+300°C
N Package	+260°C
Power Dissipation (Note 9)	1 Watt
ESD Tolerance	
Czap = 100 pF, Rzap = 1.5k	2000V

Electrical Characteristics

V_{in} = 20 V_{dc}, **Boldface** limits apply from T_{MIN} to T_{MAX} (Note 1), all other limits T_j = 25°C unless otherwise noted

Parameter	Conditions	LM1525A LM1527A			LM3525A LM3527A			Units
		Typical	Tested Limit (Note 2)	Design Limit (Note 3)	Typical	Tested Limit (Note 2)	Design Limit (Note 3)	
REFERENCE SECTION								
Reference Voltage Output	T_j = 25°C	5.10	5.05 5.15		5.10	5.00 5.20		V_{min} V_{max}
Line Regulation	+8.0V ≤ V_{in} ≤ + 35V	10	**20**		10	15	**20**	mV_{max}
Load Regulation	0 mA ≤ I_L ≤ 20 mA	20	**50**		20	20	**50**	mV_{max}
Temperature Stability		20		**50**	20		**50**	mV_{max}
Reference Voltage Output	+8.0V ≤ V_{in} ≤ +35V 0 mA ≤ I_L ≤ 20 mA And Over Operating Temp.	5.08	**5.20** **5.00**		5.08		**5.25** **4.95**	V_{max} V_{min}
Short Circuit Current	T_j = 25°C V_{ref} = 0V	70	100		70	100		mA_{max}
Output Noise Voltage	10 Hz ≤ f ≤ 10 kHz T_j = 25°C	40		200	40		200	μV_{rms} max
Long Term Stability	T_j = 125°C	20		50	20		50	mV/KHour
OSCILLATOR SECTION (Note 4) Unless otherwise specified								
Initial Accuracy	T_j = 25°C	±2	±6		±2	±6		%
Accuracy of Freq. vs. Temp.		±3	**±8**		±3		**±10**	%
Voltage Stability	8.0V ≤ V_{in} ≤ 35V	±0.3	**±1**		±0.3	±2	**±2**	%
Temperature Stability	$\Delta F_{osc}/F_{osc}$	±3		**±6**	±3		**±6**	%
Minimum Frequency	R_T = 300 kΩ, C_T = 0.1 μF, R_D = 0 (Note 5)	70	**100**		70	90	**100**	Hz max
Maximum Frequency	R_T = 2.0 kΩ, C_T = 1 nF, R_D = 0	450	**400**		450	430	**400**	kHz min
Current Mirror $I_{pin\ 5}$	I_{RT} = 2.0 mA	2.0	**1.7** **2.2**		2.0	1.8 2.1	**1.7** **2.2**	mA_{min} mA_{max}
Clock Amplitude	At pin 4	3.5		**3.0**	3.5		**3.0**	V_{min}
Clock Width	T_j = 25°C	0.5		1.0 0.3	0.5		1.0 0.3	μs max μs min
Sync Threshold	(Note 6)	1.8	**1.2** **2.8**		1.8	1.25 2.8	**1.2** **2.8**	V min V max
Sync Input Current	Sync Voltage = 3.5V	1.0	**2.5**		1.0	2.30	**2.5**	mA_{max}

Electrical Characteristics

V_{in} = 20 V_{dc}, **Boldface** limits apply from T_{MIN} to T_{MAX} (Note 1), all other limits T_j = 25°C unless otherwise noted (Continued)

Parameter	Conditions	LM1525A LM1527A			LM3525A LM3527A			Units
		Typical	Tested Limit (Note 2)	Design Limit (Note 3)	Typical	Tested Limit (Note 2)	Design Limit (Note 3)	
ERROR AMPLIFIER SECTION V_{CM} = 5.1V, Unless otherwise noted								
Input Offset Voltage		0.5	**5**		2	7	**10**	mV_{max}
Input Bias Current		1	**10**		1	2	**10**	μA_{max}
Input Offset Current		0.1	**1**		0.1	0.8	**1**	μA_{max}
DC Open Loop Gain	$R_L \geq 10\ M\Omega$	80	**66**		80	66	**60**	dB min
Gain Bandwidth Product	A_V = 0, T_j = 25°C $C_L \leq 30$ pF	2		1	2		1	MHz_{min}
Output Low Level		0.2	**0.5**		0.2	0.4	**0.5**	V_{max}
Output High Level		5.6	**3.8**		5.6	4.1	**3.8**	V_{min}
Common Mode Rejection	V_{CM} = 1.5V to 5.2V	80	**66**		80	70	**66**	dB min
Supply Voltage Rejection	V_{IN} = 8V to 35V	90	**60**		90	64	**60**	dB min
P.W.M. COMPARATOR								
Minimum Duty Cycle			**0**			0	**0**	% max
Maximum Duty Cycle		49	**45**		49	46	**45**	% min
Input Threshold	Zero Duty Cycle	0.9	**0.6**		0.9	0.70	**0.6**	V_{min}
Input Threshold	Max. Duty Cycle	3.3	**3.6**		3.3	3.6	**3.6**	V_{max}
Input Bias Current		0.05		**1.0**	0.05		**1.0**	μA_{max}
SOFT-START SECTION								
Soft Start Current	$V_{SHUTDOWN}$ = 0V	50	**80** **25**		50	74 36	**80** **25**	μA_{max} μA_{min}
Soft Start Voltage	$V_{SHUTDOWN}$ = 2.0V	0.35	**0.6**		0.35	0.5	**0.6**	V_{max}
Shutdown Input Current	$V_{SHUTDOWN}$ = 2.5V	0.4	**1.0**		0.4	0.85	**1.0**	mA_{max}
OUTPUT DRIVERS (Each Output) V_C = 20V, Unless otherwise noted								
Undervoltage Lockout Hysteresis		0.2			0.2			V
Output Low Level	I_{SINK} = 20 mA	0.2	**0.4**		0.2	0.35	**0.4**	V_{max}
	I_{SINK} = 100 mA	1.0	**2.0**		1.0	1.9	**2.0**	V_{max}
Output High Level	I_{SOURCE} = 20 mA	19	**18**		19	18.2	**18**	V_{min}
	I_{SOURCE} = 100 mA	18	**17**		18	17.4	**17**	V_{min}
Undervoltage Lockout	V_{COMP} and V_{SS} = High	7	**8** **6**		7	7.7 6.3	**8** **6**	V_{max} V_{min}
Collector Leakage	LM1525A and LM3525A Only V_C = 35V		**200**			120	**200**	μA_{max}
Rise Time	C_L = 1 nf, T_j = 25°C	100		600	100		600	ns max
Fall Time	C_L = 1 nf, T_j = 25°C	50		300	50		300	ns max

Electrical Characteristics

V_{in} = 20 V_{dc}, **Boldface** limits apply from T_{MIN} to T_{MAX} (Note 1), all other limits T_j = 25°C unless otherwise noted (Continued)

Parameter	Conditions	LM1525A LM1527A			LM3525A LM3527A			Units
		Typical	Tested Limit (Note 2)	Design Limit (Note 3)	Typical	Tested Limit (Note 2)	Design Limit (Note 3)	
Shutdown Delay	V_{SD} = 3V, C_L = 0, T_j = 25°C	200		500	200		500	ns max
TOTAL STANDBY CURRENT								
Supply Current	V_{IN} = 35V	13	**18**		13	14.5	**20**	mA

Note 1: Unless otherwise noted these specifications apply: −55°C < T_j < +125°C for LM1525A and LM1527A, 0°C < T_j < +125°C for LM3525A and LM3527A.

Note 2: Tested limits are guaranteed and 100% tested in production.

Note 3: Design limits are guaranteed (but not 100% production tested) over the indicated temperature and supply ranges.

Note 4: Tested at F_{osc} = 40 kHz (Rt = 3.6k, Ct = 0.01 μF, Rd = 0).

Note 5: These specifications are also guaranteed with Rt = 150k, Ct = 0.2 μF, Rd = 0.

Note 6: Tested with a pulse of width 500 ns and amplitudes of 1.2 and 2.8V at 50 kHz.

Note 7: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its rated operating conditions. See Note 1 and conditions.

Note 8: Do not ground pin 6.

Note 9: For operation at elevated temperatures, devices in the J package must be derated based on thermal resistance of 90°C/W (junction to ambient), or 85°C/W in the N package.

SHUTDOWN OPTIONS (See Block Diagram)

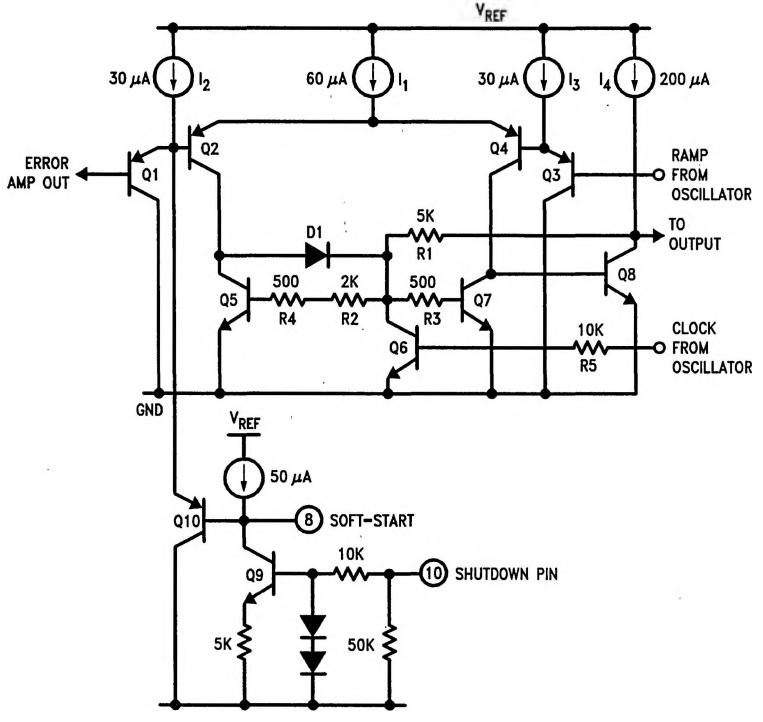
1. Since both the compensation and soft-start terminals (pins 9 and 8) have current source pull-ups, either can readily accept a pull-down signal which only has to sink a maximum of 100 μA to turn off the outputs. This is subject to the added requirement of discharging whatever external capacitance may be attached to these pins.
2. An alternative approach is the use of the shutdown circuitry of pin 10. Activating this circuit by applying a positive-going pulse at pin 10 will result in the output of the comparator going high, and thus turning off the outputs. The pulse will start the fast discharge of the soft-start capacitor. If the shutdown command is short, the PWM signal is terminated without significant discharge of the soft-start capacitor, thus allowing, for example, a convenient implementation of pulse-by-pulse current limiting. Holding pin 10 high for a long time will ultimately discharge the soft-start capacitor, thus recycling slow turn on upon release. This method of shutdown is the fastest shutdown possible.

SYNCHRONIZATION PROCEDURE

The device may be synchronized to an external clock; however the following points have to be observed: a) The frequency of the free-running oscillator of the device must be set at least 10% less than the frequency of the external clock. b) The external clock pulse must be at least 300 ns wide but must not exceed the free-running pulse width (pin 4) by more than 200 ns. c) The amplitude of the external pulse must be between 2 and 5V.

Multiple devices may be synchronized together by connecting all pin 4's together and all pin 5's together; pins 6 and 7 of slave oscillator must be left open.

LM1525A Comparator



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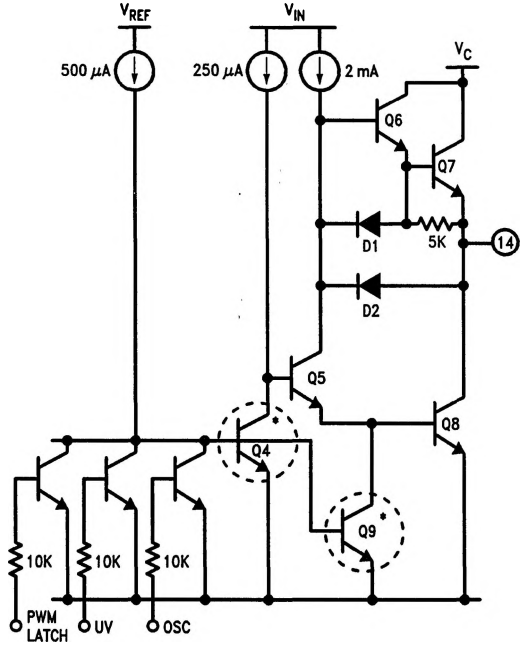
LM1525A Output Section



*Q_4 omitted in LM1527A.
Q_9 replaced by a 2K resistor in LM1527A.

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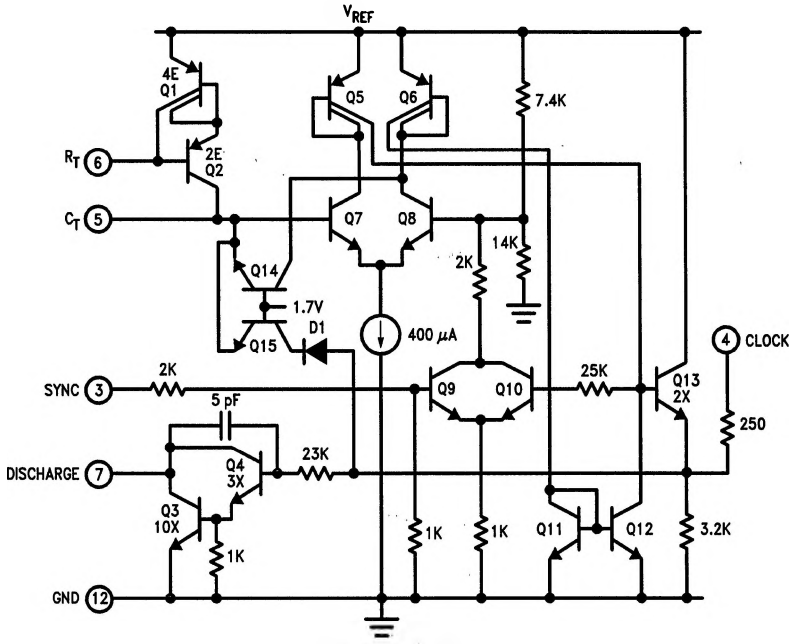
LM1525A Oscillator



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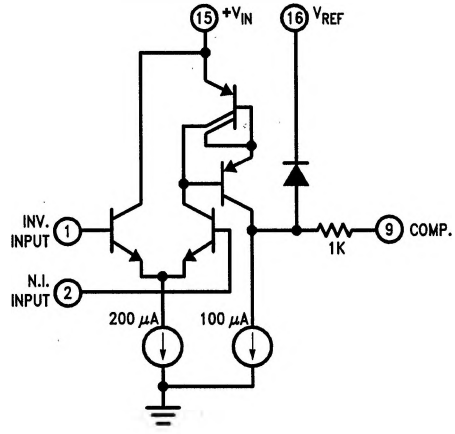
LM1525A Error Amplifier



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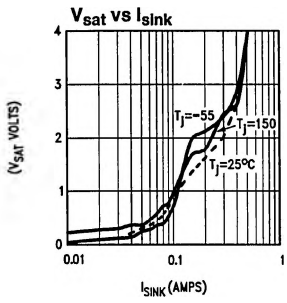
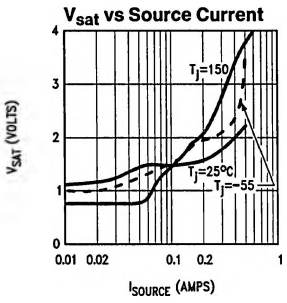
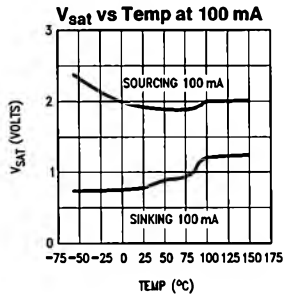
V_{sat} vs I_{sink}



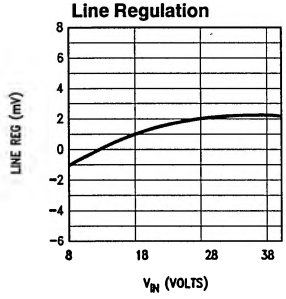
V_{sat} vs Source Current



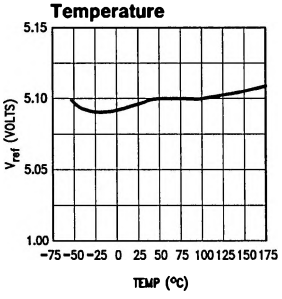
V_{sat} vs Temp at 100 mA



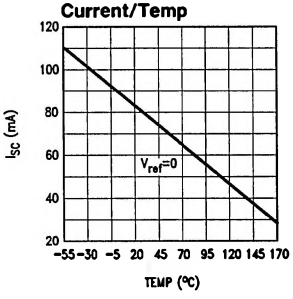
Line Regulation



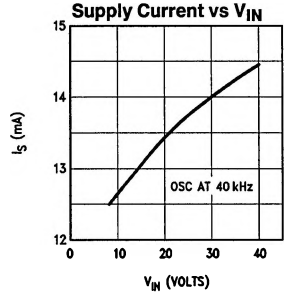
Typical V_{ref} vs Temperature



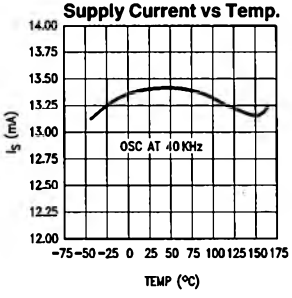
V_{ref} Short-Circuit Current/Temp



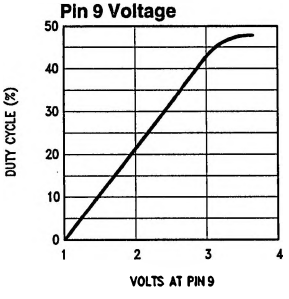
Supply Current vs V_{IN}



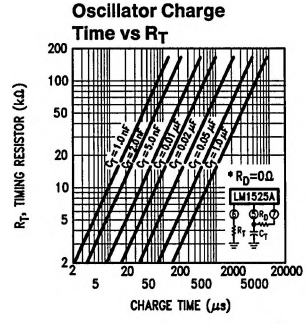
Supply Current vs Temp.



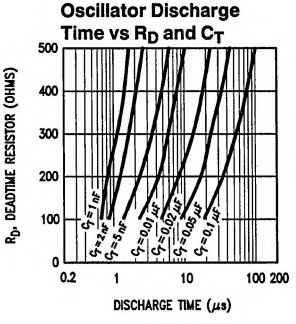
Duty Cycle vs Pin 9 Voltage



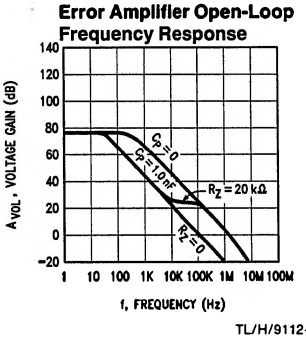
Oscillator Charge Time vs R_T



Oscillator Discharge Time vs R_D and C_T



Error Amplifier Open-Loop Frequency Response



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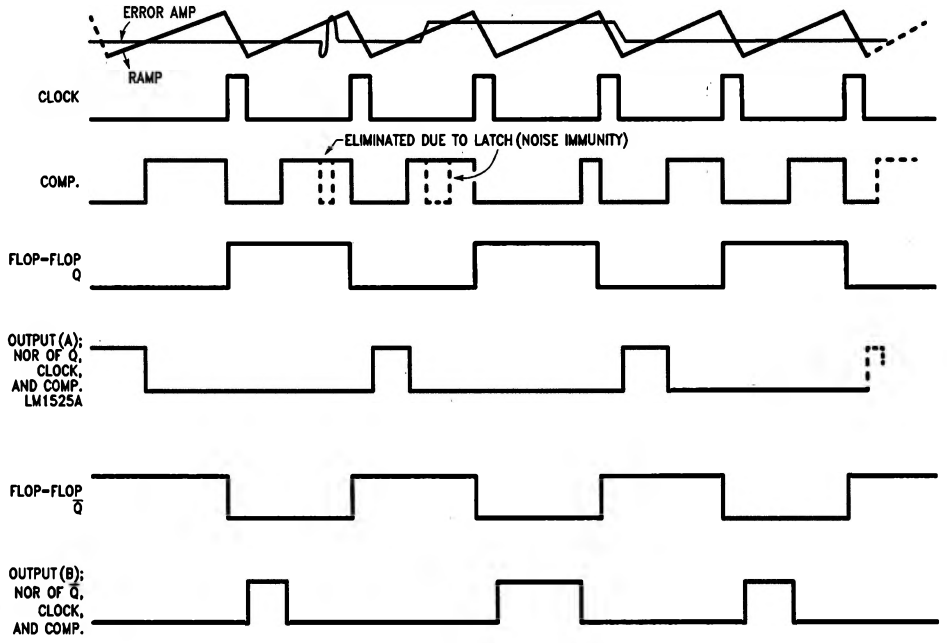
LM1525A Typical Timing Diagram



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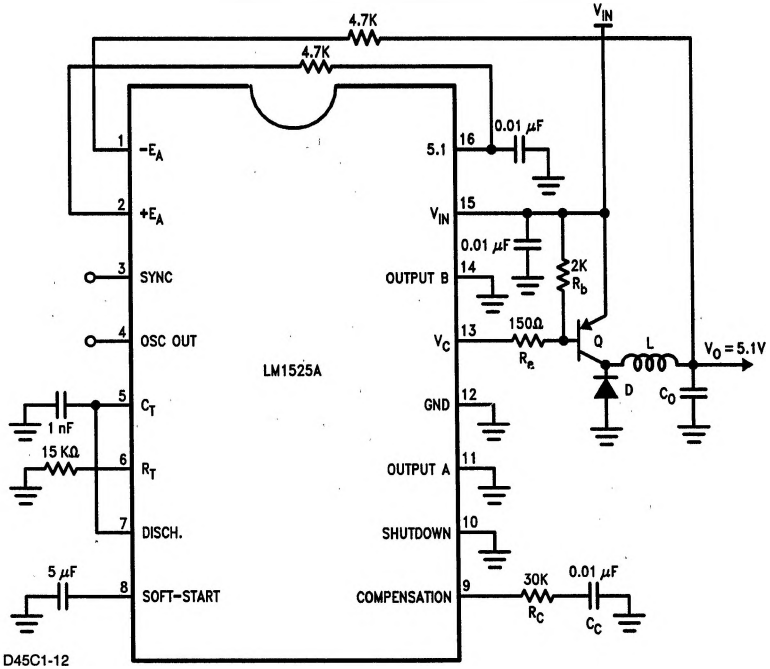
Typical Applications

5 Watt Single Ended Step Down Converter



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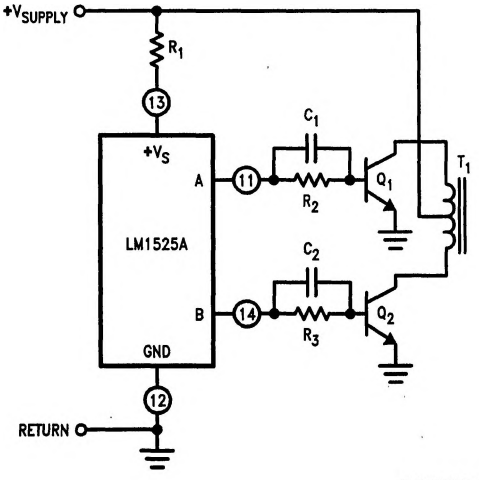
V_{IN} = 28V Q = D45C1-12
V_{OUT} = 5.1V D = IN5821
L = 150 µH
C_O = 500 µF

Typical Applications (Continued)

Bipolar Drive for Push-Pull Converters



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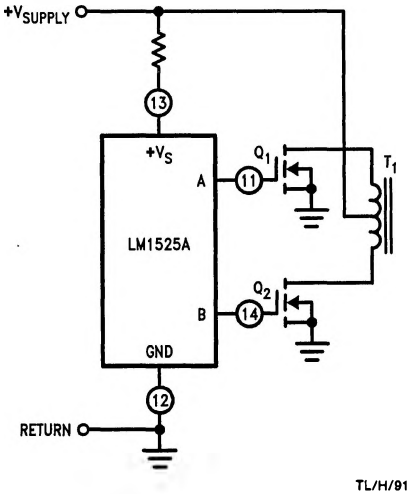
3 MOSFET Drive for Push-Pull Converters



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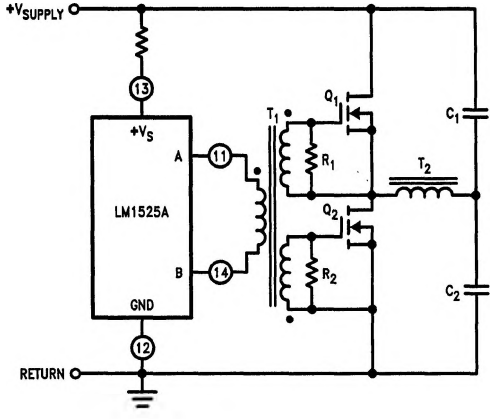
Direct Drive for Transformer



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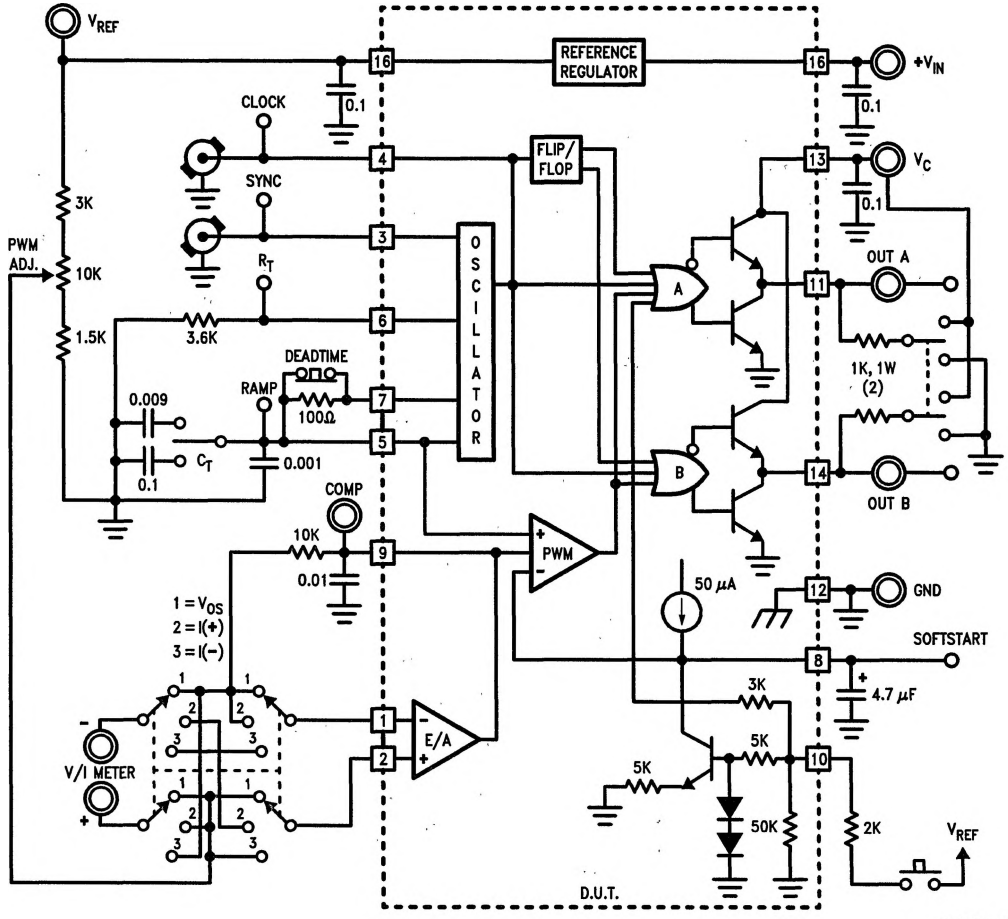
Typical Applications (Continued)

LM1525A/1527A Lab Test Fixture



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