LM193JAN Low Power Low Offset Voltage Dual Comparators

Check for Samples: LM193JAN

FEATURES

- **Wide supply**
  - **Voltage range: 5.0V_{DC} to 36V_{DC}**
  - **Single or dual supplies: ±2.5V_{DC} to ±18V_{DC}**
- **Very low supply current drain (0.4 mA) — independent of supply voltage**
- **Low input biasing current: 25 nA typ**
- **Low input offset current: ±3 nA typ**
- **Maximum offset voltage +5mV Max @ 25°C**
- **Input common-mode voltage range includes ground**
- **Differential input voltage range equal to the power supply voltage**
- **Low output saturation voltage,: 250 mV at 4 mA typ**
- **Output voltage compatible with TTL, DTL, ECL, MOS and CMOS logic systems**

ADVANTAGES

- **High precision comparators**
- **Reduced V_{OS} drift over temperature**
- **Eliminates need for dual supplies**
- **Allows sensing near ground**
- **Compatible with all forms of logic**
- **Power drain suitable for battery operation**

DESCRIPTION

The LM193 series consists of two independent precision voltage comparators with an offset voltage specification as low as 2.0 mV max for two comparators which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators also have a unique characteristic in that the input common-mode voltage range includes ground, even though operated from a single power supply voltage.

Application areas include limit comparators, simple analog to digital converters; pulse, squarewave and time delay generators; wide range VCO; MOS clock timers; multivibrators and high voltage digital logic gates. The LM193 series was designed to directly interface with TTL and CMOS. When operated from both plus and minus power supplies, the LM193 series will directly interface with MOS logic where their low power drain is a distinct advantage over standard comparators.

Figure 1. Squarewave Oscillator

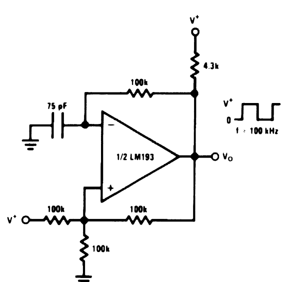
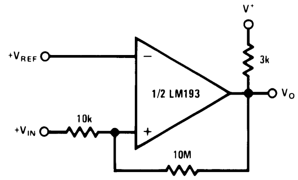


Figure 2. Non-Inverting Comparator with Hysteresis



Schematic and Connection Diagrams

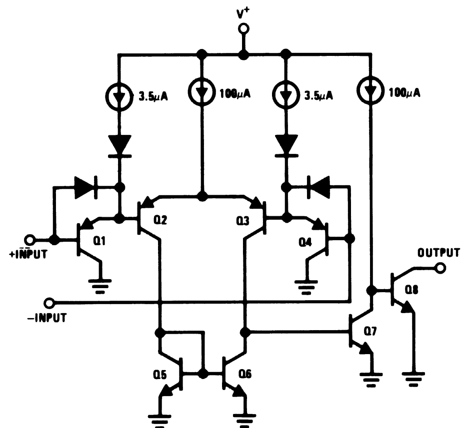


Figure 3. Metal Can Package

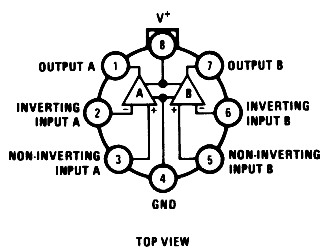
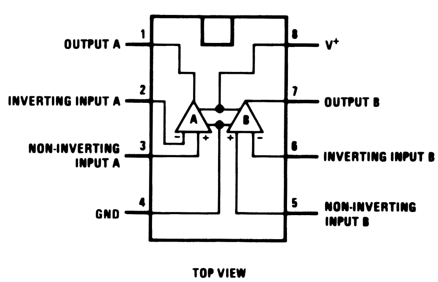


Figure 4. Dual-In-Line Package



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings [1]

Supply Voltage, V^+	$36V_{DC}$ or $\pm 18V_{DC}$
Differential Input Voltage [2]	36V
Output Voltage	36V
Input Voltage	$-0.3V_{DC}$ to $+36V_{DC}$
Input Current ($V_{IN}< -0.3V_{DC}$) [3]	50 mA
Power Dissipation [4],	
CERDIP	400 mW @ T_A = 125°C
Metal Can	330 mW @ T_A = 125°C
Maximum Junction Temperature (T_{Jmax}	175°C
Output Short-Circuit to Ground [5]	Continuous
Operating Temperature Range	$-55°C \le T_A \le +125°C$
Storage Temperature Range	$-65°C \le T_A \le +150°C$
Thermal Resistance	
θ_{JA}	
Metal Can (Still Air)	174°C/W
Metal Can (500LF/Min Air flow)	99°C/W
CERDIP (Still Air)	146°C/W
CERDIP (500LF/Min Air flow)	85°C/W
θ_{JC}	
Metal Can	44°C/W
CERDIP	33°C/W
Lead Temperature (Soldering, 10 seconds)	260°C
ESD Tolerance [6]	500V

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(2) Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than −0.3V (or 0.3V below the magnitude of the negative power supply, if used).
(3) This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the comparators to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than $-0.3V_{DC}$.
(4) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax} (maximum junction temperature), θ_{JA} (package junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is $P_{Dmax} = (T_{Jmax} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower.
(5) Short circuits from the output to V^+ can cause excessive heating and eventual destruction. When considering short circuits to ground, the maximum output current is approximately 20 mA independent of the magnitude of V^+.
(6) Human body model, 1.5KΩ in series with 100pF.

Quality Conformance Inspection

Mil-Std-883, Method 5005 - Group A

Subgroup	Description	Temp°C
1	Static tests at	25
2	Static tests at	125
3	Static tests at	-55
4	Dynamic tests at	25
5	Dynamic tests at	125
6	Dynamic tests at	-55
7	Functional tests at	25
8A	Functional tests at	125

Subgroup	Description	Temp°C
8B	Functional tests at	-55
9	Switching tests at	25
10	Switching tests at	125
11	Switching tests at	-55
12	Settling time at	25
13	Settling time at	125
14	Settling time at	-55

LM193 JAN Electrical Characteristics DC Parameters

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
V_{IO}	Input Offset Voltage	$+V_{CC}$ = 30V, $-V_{CC}$ = 0V, V_O = 15V		-5.0	5.0	mV	1
				-7.0	7.0	mV	2, 3
		$+V_{CC}$ = 2V, $-V_{CC}$ = -28V, V_O = -13V		-5.0	5.0	mV	1
				-7.0	7.0	mV	2, 3
		$+V_{CC}$ = 5V, $-V_{CC}$ = 0V, V_O = 1.4V		-5.0	5.0	mV	1
				-7.0	7.0	mV	2, 3
		$+V_{CC}$ = 2V, $-V_{CC}$ = -3V, V_O = -1.6V		-5.0	5.0	mV	1
				-7.0	7.0	mV	2, 3
I_{IO}	Input offset Current	$+V_{CC}$ = 30V, $-V_{CC}$ = 0V, V_O = 15V, R_S = 20KΩ	(1)	-25	25	nA	1, 2
			(1)	-75	75	nA	3
		$+V_{CC}$ = 2V, $-V_{CC}$ = -28V, V_O = -13V, R_S = 20KΩ	(1)	-25	25	nA	1, 2
			(1)	-75	75	nA	3
		$+V_{CC}$ = 5V, $-V_{CC}$ = 0V, V_O = 1.4V, R_S = 20KΩ	(1)	-25	25	nA	1, 2
			(1)	-75	75	nA	3
		$+V_{CC}$ = 2V, $-V_{CC}$ = -3V, V_O = -1.6V, R_S = 20KΩ	(1)	-25	25	nA	1, 2
			(1)	-75	75	nA	3
$\pm I_{IB}$	Input Bias Current	$+V_{CC}$ = 30V, $-V_{CC}$ = 0V, V_O = 15V, R_S = 20KΩ	(1)	-100	+0.1	nA	1, 2
			(1)	-200	+0.1	nA	3
		$+V_{CC}$ = 2V, $-V_{CC}$ = -28V, V_O = -13V, R_S = 20KΩ	(1)	-100	+0.1	nA	1, 2
			(1)	-200	+0.1	nA	3
		$+V_{CC}$ = 5V, $-V_{CC}$ = 0V, V_O = 1.4V, R_S = 20KΩ	(1)	-100	+0.1	nA	1, 2
			(1)	-200	+0.1	nA	3
		$+V_{CC}$ = 2V, $-V_{CC}$ = -3V, V_O = -1.6V, R_S = 20KΩ	(1)	-100	+0.1	nA	1, 2
			(1)	-200	+0.1	nA	3
CMRR	Input Voltage Common Mode Rejection	2V ≤ $+V_{CC}$ ≤ 30V, -28V ≤ $-V_{CC}$ ≤ 0V, -13V ≤ V_O ≤ 15V		76		dB	1, 2, 3
		2V ≤ $+V_{CC}$ ≤ 5V, -3V ≤ $-V_{CC}$ ≤ 0V, -1.6V ≤ V_O ≤ 1.4V		70		dB	1, 2, 3
I_{CEX}	Output Leakage Current	$+V_{CC}$ = 30V, $-V_{CC}$ = 0V, V_O = +30V			1.0	µA	1, 2, 3
$+I_{IL}$	Input Leakage Current	$+V_{CC}$ = 36V, $-V_{CC}$ = 0V, $+V_I$ = 34V, $-V_I$ = 0V		-500	500	nA	1, 2, 3
$-I_{IL}$	Input Leakage Current	$+V_{CC}$ = 36V, $-V_{CC}$ = 0V, $+V_I$ = 0V, $-V_I$ = 34V		-500	500	nA	1, 2, 3
V_{OL}	Logical "0" Output Voltage	$+V_{CC}$ = 4.5V, $-V_{CC}$ = 0V, I_O = 4mA			0.4	V	1
					0.7	V	2, 3
		$+V_{CC}$ = 4.5V, $-V_{CC}$ = 0V, I_O = 8mA			1.5	V	1
					2.0	V	2, 3
I_{CC}	Power Supply Current	$+V_{CC}$ = 5V, $-V_{CC}$ = 0V, V_{ID} = 15mV			2.0	mA	1, 2
					3.0	mA	3
		$+V_{CC}$ = 30V, $-V_{CC}$ = 0V, V_{ID} = 15mV			3.0	mA	1, 2
					4.0	mA	3
Δ_{IO} / ΔT	Temperature Coefficient of Input Offset Voltage	25°C ≤ T_A ≤ +125°C	(2)	-25	25	µV/°C	2
		-55°C ≤ T_A ≤ 25°C	(2)	-25	25	µV/°C	3

(1) S/S R_S = 20KΩ, tested with R_S = 100KΩ for better resolution
(2) Calculated parameter for ΔV_{IO} / ΔT and ΔI_{IO} / ΔT.

LM193 JAN Electrical Characteristics DC Parameters (continued)

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
ΔI_{IO} / ΔT	Temperature Coefficient of Input Offset Current	25°C ≤ T_A ≤ +125°C	(2)	-300	300	pA/°C	2
		-55°C ≤ T_A ≤ 25°C	(2)	-400	400	pA/°C	3
A_{VS}	Open Loop Voltage Gain	$+V_{CC}$ = 15V, $-V_{CC}$ = 0V, R_L = 15KΩ, 1V ≤ V_O ≤ 11V	(3)	50		V/mV	4
			(3)	25		V/mV	5, 6
V_{Lat}	Voltage Latch (Logical "1" Input)	$+V_{CC}$ = 5V, $-V_{CC}$ = 0V, V_I = 10V, I_O = 4mA			0.4	V	9

(3) K in datalog is equivalent to V/mV.

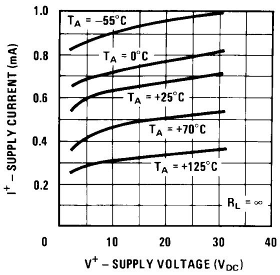
LM193 JAN Electrical Characteristics AC Parameters

The following conditions apply, unless otherwise specified. $+V_{CC}$ = 5V, $-V_{CC}$ = 0V

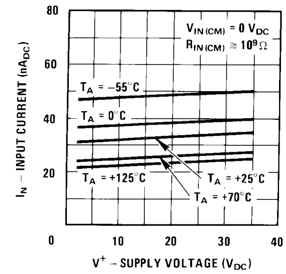
Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
t_{RLH}	Response Time	V_I = 100mV, R_L = 5.1KΩ, V_{OD} = 5mV			5.0	µS	7, 8B
					7.0	µS	8A
		V_I = 100mV, R_L = 5.1KΩ, V_{OD} = 50mV			0.8	µS	7, 8B
					1.2	µS	8A
t_{RHL}	Response Time	V_I = 100mV, R_L = 5.1KΩ, V_{OD} = 5mV			2.5	µS	7, 8B
					3.0	µS	8A
		V_I = 100mV, R_L = 5.1KΩ, V_{OD} = 50mV			0.8	µS	7, 8B
					1.0	µS	8A
CS	Channel Separation	$+V_{CC}$ = 20V, $-V_{CC}$ = -10V, A to B		80		dB	7
		$+V_{CC}$ = 20V, $-V_{CC}$ = -10V, B to A		80		dB	7

Typical Performance Characteristics

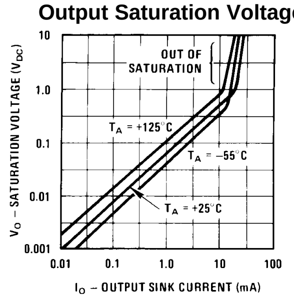
Supply Current



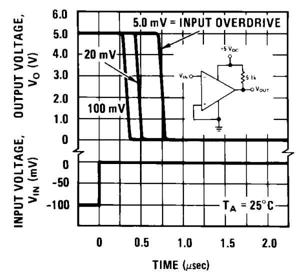
Input Current



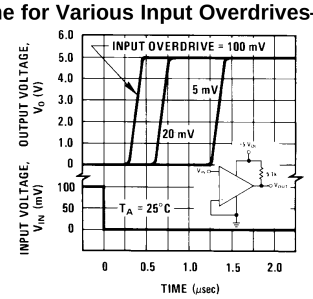
Output Saturation Voltage



Response Time for Various Input Overdrives—Negative Transition



Response Time for Various Input Overdrives—Positive Transition



Application Hints

The LM193 series are high gain, wide bandwidth devices which, like most comparators, can easily oscillate if the output lead is inadvertently allowed to capacitively couple to the inputs via stray capacitance. This shows up only during the output voltage transition intervals as the comparator change states. Power supply bypassing is not required to solve this problem. Standard PC board layout is helpful as it reduces stray input-output coupling. Reducing the input resistors to < 10 kΩ reduces the feedback signal levels and finally, adding even a small amount (1.0 to 10 mV) of positive feedback (hysteresis) causes such a rapid transition that oscillations due to stray feedback are not possible. Simply socketing the IC and attaching resistors to the pins will cause input-output oscillations during the small transition intervals unless hysteresis is used. If the input signal is a pulse waveform, with relatively fast rise and fall times, hysteresis is not required.

All input pins of any unused comparators should be tied to the negative supply.

The bias network of the LM193 series establishes a drain current which is independent of the magnitude of the power supply voltage over the range of from 2.0 V_{DC} to 30 V_{DC}.

It is usually unnecessary to use a bypass capacitor across the power supply line.

The differential input voltage may be larger than V^+ without damaging the device [1]. Protection should be provided to prevent the input voltages from going negative more than −0.3 V_{DC} (at 25°C). An input clamp diode can be used as shown in the applications section.

(1) Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than −0.3V (or 0.3V below the magnitude of the negative power supply, if used).

The output of the LM193 series is the uncommitted collector of a grounded-emitter NPN output transistor. Many collectors can be tied together to provide an output OR'ing function. An output pull-up resistor can be connected to any available power supply voltage within the permitted supply voltage range and there is no restriction on this voltage due to the magnitude of the voltage which is applied to the V^+ terminal of the LM193 package. The output can also be used as a simple SPST switch to ground (when a pull-up resistor is not used). The amount of current which the output device can sink is limited by the drive available (which is independent of V^+) and the β of this device. When the maximum current limit is reached (approximately 16mA), the output transistor will come out of saturation and the output voltage will rise very rapidly. The output saturation voltage is limited by the approximately 60Ω r_{SAT} of the output transistor. The low offset voltage of the output transistor (1.0mV) allows the output to clamp essentially to ground level for small load currents.

Typical Applications

(V^+=5.0 V_{DC})

Figure 5. Basic Comparator

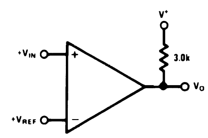


Figure 6. Driving CMOS

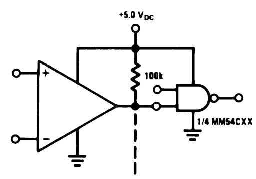


Figure 7. Driving TTL

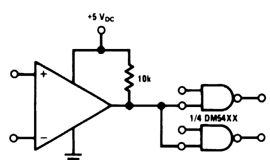
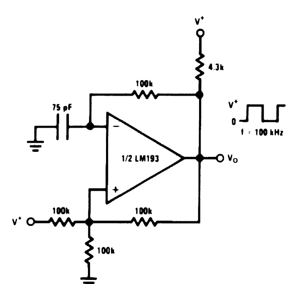
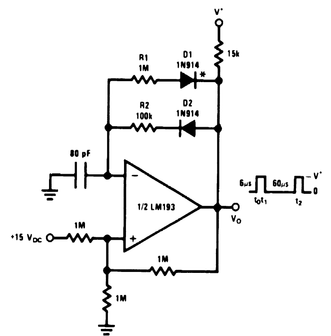


Figure 8. Squarewave Oscillator



(V^{+}=5.0 V_{DC})

Figure 9. Pulse Generator



* For large ratios of R1/R2,
D1 can be omitted.

Figure 10. Crystal Controlled Oscillator

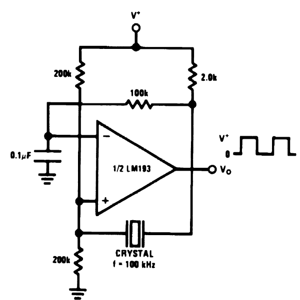
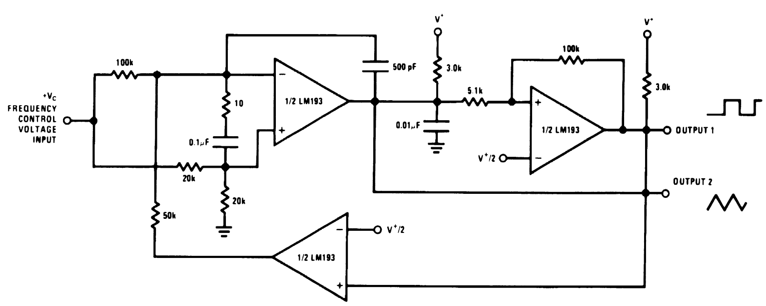
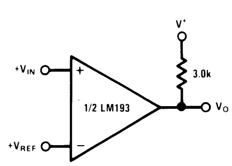


Figure 11. Two-Decade High Frequency VCO



$V^{*} = +30\ V_{DC}$
$+250\ mV_{DC} \le V_C \le +50\ V_{DC}$
$700Hz \le f_o \le 100kHz$

Figure 12. Basic Comparator



(V^+=5.0 V_{DC})

Figure 13. Non-Inverting Comparator with Hysteresis

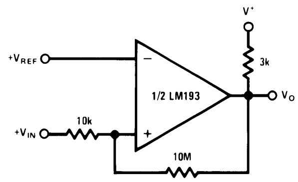


Figure 14. Inverting Comparator with Hysteresis

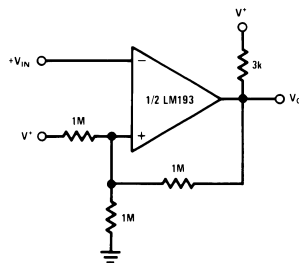


Figure 15. Output Strobing

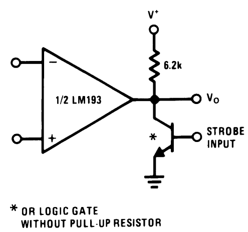


Figure 16. AND Gate

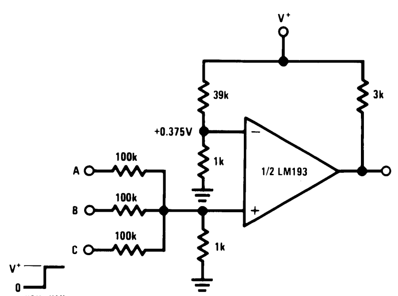
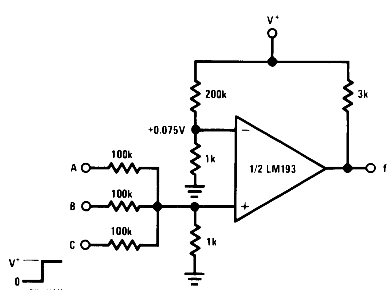


Figure 17. OR Gate



(V^{+}=5.0 V_{DC})

Figure 18. Large Fan-in AND Gate

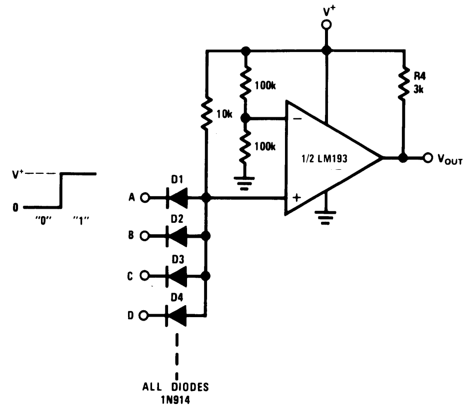


Figure 19. Limit Comparator

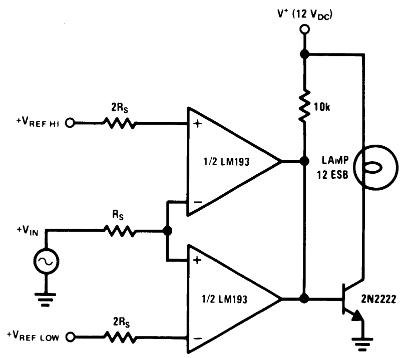


Figure 20. Comparing Input Voltages of Opposite Polarity

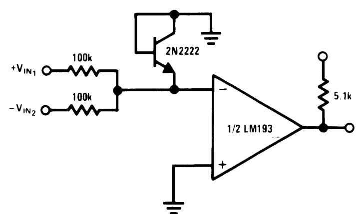
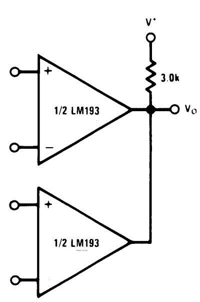


Figure 21. ORing the Outputs



(V^{+}=5.0 V_{DC})

Figure 22. Zero Crossing Detector (Single Power Supply)

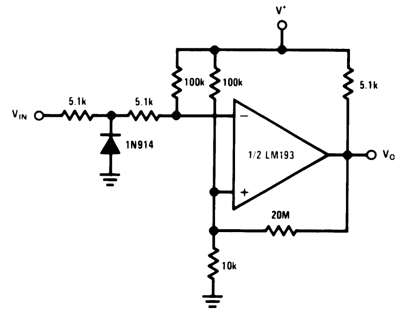


Figure 23. One-Shot Multivibrator

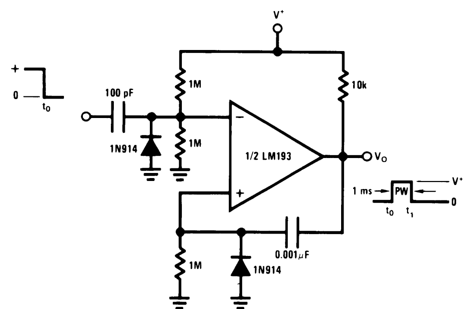


Figure 24. Bi-Stable Multivibrator

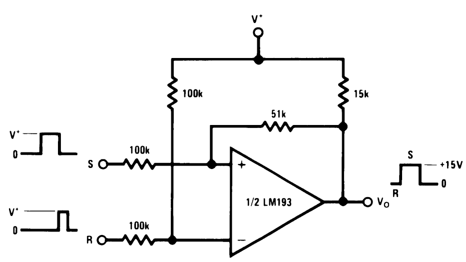
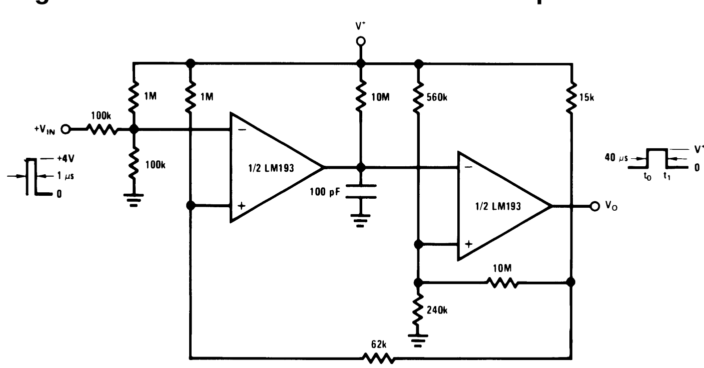


Figure 25. One-Shot Multivibrator with Input Lock Out



(V^+=5.0 V_{DC})

Figure 26. Zero Crossing Detector

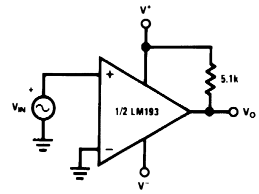


Figure 27. Comparator With a Negative Reference

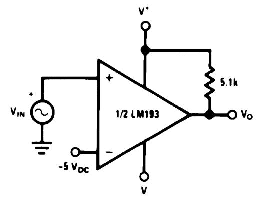
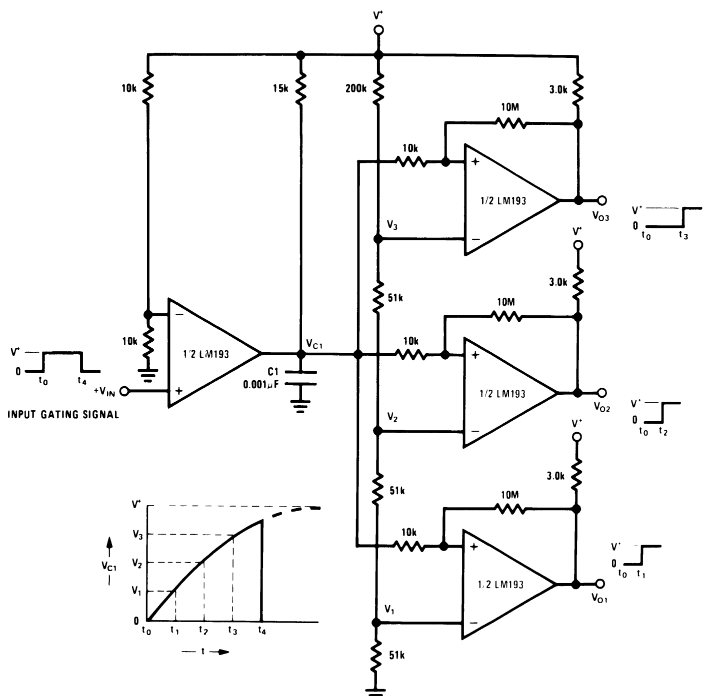


Figure 28. Time Delay Generator

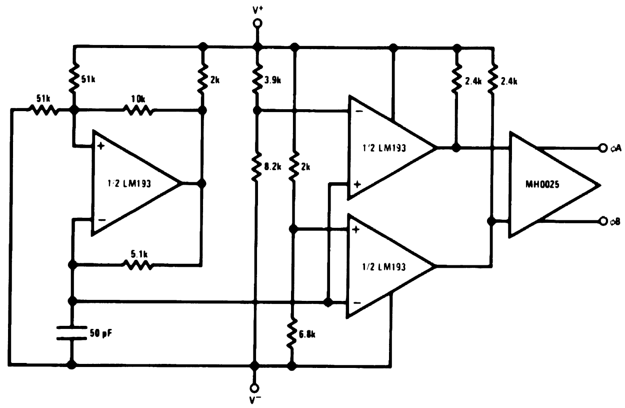


Split-Supply Applications

(V^+=+15 V_{DC} and V^-=−15 V_{DC})

(V^{+}=+15 V_{DC} and V^{-}=−15 V_{DC})

Figure 29. MOS Clock Driver



REVISION HISTORY SECTION

Date Released	Revision	Section	Originator	Changes
05/09/05	A	New Release. Corporate format	L. Lytle	1 MDS datasheets converted into one Corp. datasheet format. DC Drift table was deleted due to no JANS product offerings. MJLM193-X Rev 1A1 MDS will be archived.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
JL193BGA	ACTIVE	TO-99	LMC	8	20	TBD	POST-PLATE	Level-1-NA-UNLIM	-55 to 125	JL193BGA JM38510/11202BGA Q ACO JM38510/11202BGA Q >T	Samples
JM38510/11202BGA	ACTIVE	TO-99	LMC	8	20	TBD	POST-PLATE	Level-1-NA-UNLIM	-55 to 125	JL193BGA JM38510/11202BGA Q ACO JM38510/11202BGA Q >T	Samples
M38510/11202BGA	ACTIVE	TO-99	LMC	8	20	TBD	POST-PLATE	Level-1-NA-UNLIM	-55 to 125	JL193BGA JM38510/11202BGA Q ACO JM38510/11202BGA Q >T	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] Only one of markings shown within the brackets will appear on the physical device.

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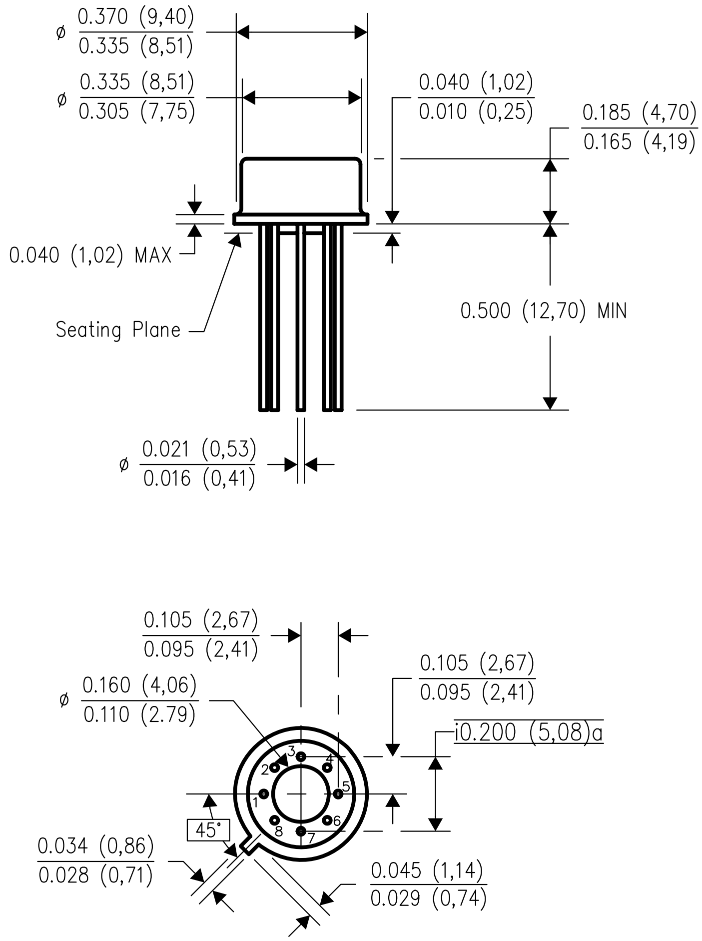
LMC (O-MBCY-W8) METAL CYLINDRICAL PACKAGE



4202483/B 09/07

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Leads in true position within 0.010 (0,25) R @ MMC at seating plane.
D. Pin numbers shown for reference only. Numbers may not be marked on package.
E. Falls within JEDEC MO-002/TO-99.

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