LM148QML Quad 741 Op Amps

Check for Samples: LM148QML

FEATURES

- **741 op amp operating characteristics**
- **Class AB output stage—no crossover distortion**
- **Pin compatible with the LM124**
- **Overload protection for inputs and outputs**
- **Low supply current drain: 0.6 mA/Amplifier**
- **Low input offset voltage: 1 mV**
- **Low input offset current: 4 nA**
- **Low input bias current 30 nA**
- **High degree of isolation between amplifiers: 120 dB**
- **Gain bandwidth product (unity gain): 1.0 MHz**

DESCRIPTION

The LM148 is a true quad LM741. It consists of four independent, high gain, internally compensated, low power operational amplifiers which have been designed to provide functional characteristics identical to those of the familiar LM741 operational amplifier. In addition the total supply current for all four amplifiers is comparable to the supply current of a single LM741 type op amp. Other features include input offset currents and input bias current which are much less than those of a standard LM741. Also, excellent isolation between amplifiers has been achieved by independently biasing each amplifier and using layout techniques which minimize thermal coupling.

The LM148 can be used anywhere multiple LM741 or LM1558 type amplifiers are being used and in applications where amplifier matching or high packing density is required.

Connection Diagram

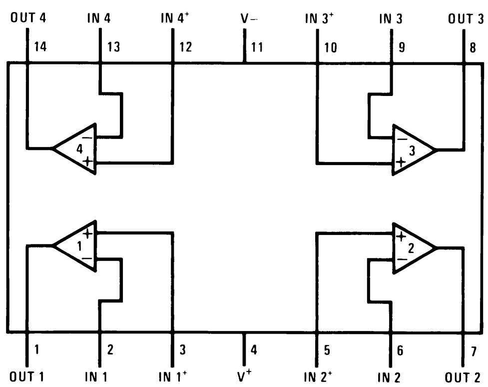

Figure 1. Top View
See NS Package Number J14A

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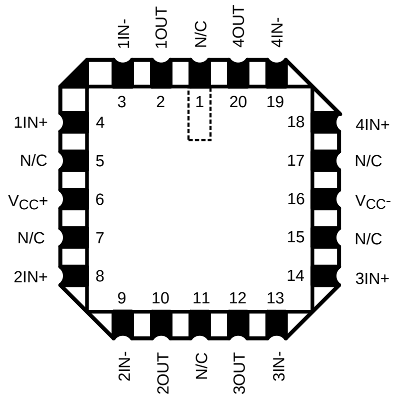
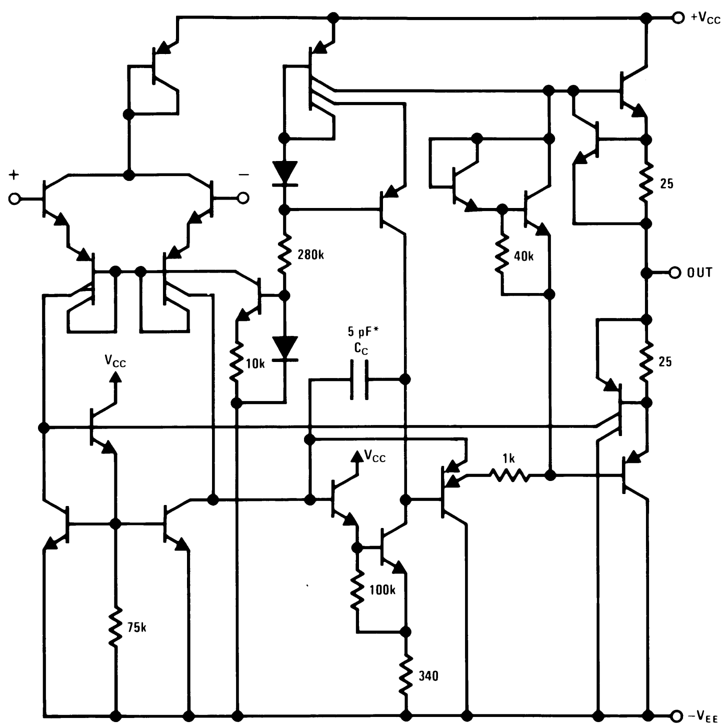


Figure 2. Top View
See NS Package Number E20A

Schematic Diagram



* 1 pF in the LM149

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

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Absolute Maximum Ratings [1]

Supply Voltage	±22V
Differential Input Voltage	±44V
Output Short Circuit Duration[2]	Continuous
Power Dissipation (P_d at 25°C) [3]	1100mW
Thermal Resistance	
θ_{JA}	
CERDIP (Still Air) CERDIP (500LF/ Min Air flow) LCC (Still Air) LCC (500LF/ Min Air flow)	103°C/W 52°C/W 90°C/W 66°C/W
θ_{JC}	
CERDIP LCC	19°C/W 21°C/W
Maximum Junction Temperature (T_{jMAX})	150°C
Operating Temperature Range	−55°C ≤ T_A ≤ +125°C
Storage Temperature Range	−65°C ≤ T_A ≤ +150°C
Lead Temperature (Soldering, 10 sec.) Ceramic	300°C
ESD tolerance [4]	500V

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(2) Any of the amplifier outputs can be shorted to ground indefinitely; however, more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.
(3) The maximum power dissipation for these devices must be derated at elevated temperatures and is dicated by T_{JMAX}, θ_{JA}, and the ambient temperature, T_A. The maximum available power dissipation at any temperature is $P_d = (T_{JMAX} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is less.
(4) Human body model, 1.5 kΩ in series with 100 pF

Quality Conformance Inspection

MIL-STD-883, Method 5005 — Group A

Subgroup	Description	Temp (°C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

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Electrical Characteristics

DC PARAMETERS (The following conditions apply to all parameters, unless otherwise specified.)
V_{CC} = ±15V, R_S = 0Ω

Symbol	Parameter	Conditions	Notes	Min	Max	Units	Sub-groups
V_{IO}	Input Offset Voltage	V_{CM} = 0V, R_S = 50 Ω		−5	+5	mV	1
				−6	+6	mV	2,3
I_{IO}	Input Offset Current	V_{CM} = 0V		−25	+25	nA	1
				−75	+75	nA	2,3
$\pm I_{IB}$	Input Bias Current	V_{CM} = 0V		1	100	nA	1
				1	325	nA	2,3
R_{in}	Input Resistance		(1)	0.8		MΩ	1
PSRR+	Power Supply Rejection Ratio	$+V_{CC}$ = +15V and +5V, $-V_{CC}$ = −15V, R_S = 50Ω		77		dB	1, 2, 3
PSRR−	Power Supply Rejection Ratio	$+V_{CC}$ = +15V, $-V_{CC}$ = −15V and −5V, R_S = 50Ω		77		dB	1, 2, 3
CMRR	Common Mode Rejection Ratio	$+V_{CM}$ = ±12V, R_S = 50Ω		70		dB	1, 2, 3
I_{OS}+	Short Circuit Current			−55	−14	mA	1
I_{OS}−	Short Circuit Current			14	55	mA	1
I_{CC}	Power Supply Current			0.4	3.6	mA	1
				0.4	4.5	mA	2, 3
A_{VS}+	Large Signal Voltage Gain	V_{OUT} = 0V to +10V, R_L > 2 kΩ		50		V/mV	4
				25		V/mV	5, 6
A_{VS}−	Large Signal Voltage Gain	V_{OUT} = 0V to −10V, R_L > 2 kΩ		50		V/mV	4
				25		V/mV	5, 6
V_{out}+	Output Voltage Swing	R_L = 10 kΩ		+12		V	4, 5, 6
		R_L = 2kΩ		+10		V	4, 5, 6
V_{out}−	Output Voltage Swing	R_L = 10 kΩ			−12	V	4, 5, 6
		R_L = 2kΩ			−10	V	4, 5, 6

(1) Parameter Guaranteed, Not Tested.

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Electrical Characteristics

AC PARAMETERS (The following conditions apply to all parameters, unless otherwise specified.)
V_{CC} = ±15V, A_V = 1, R_S = 0Ω

Symbol	Parameter	Conditions	Notes	Min	Max	Units	Sub-groups
±SR	Slew Rate			0.2		V/μs	7, 8A, 8B
G_{BW}	Gain Bandwidth Product			0.4	1.4	MHz	7, 8A, 8B

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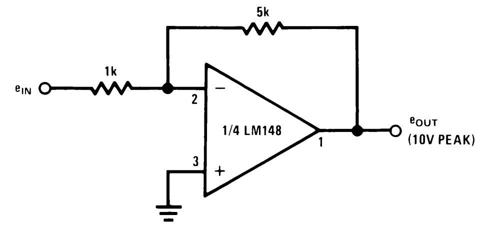
Cross Talk Test Circuit

V_S = ±15V



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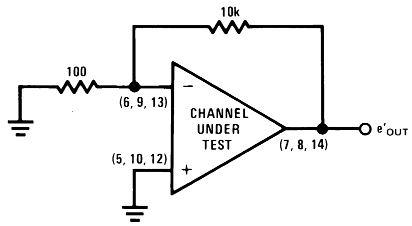

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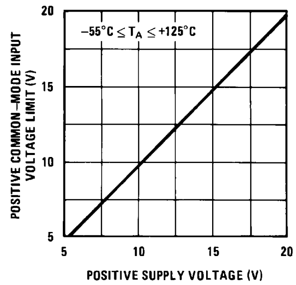

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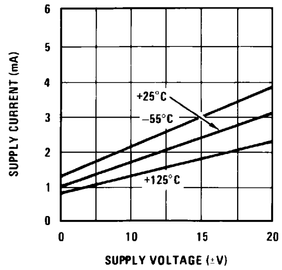
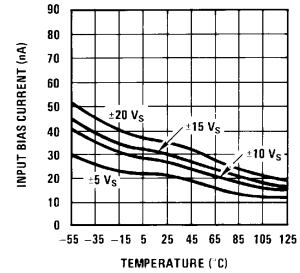
Typical Performance Characteristics

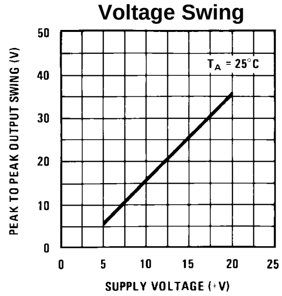
Supply Current



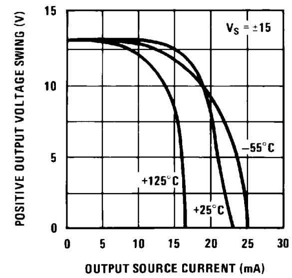
Input Bias Current



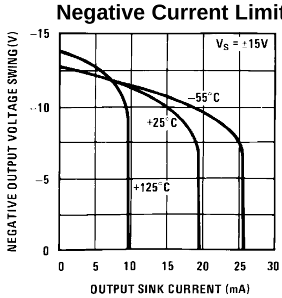
Voltage Swing



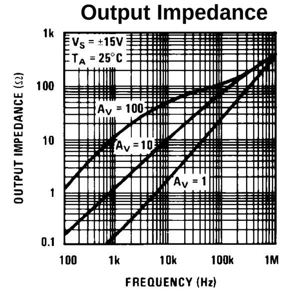
Positive Current Limit



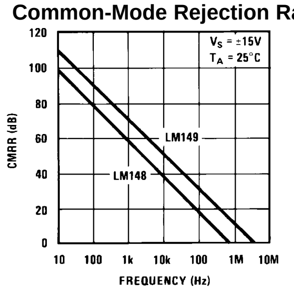
Negative Current Limit



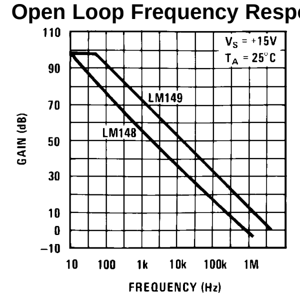
Output Impedance



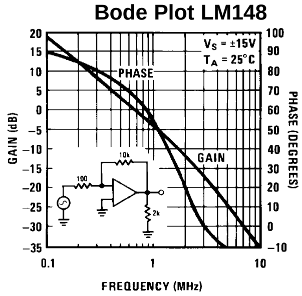
Common-Mode Rejection Ratio



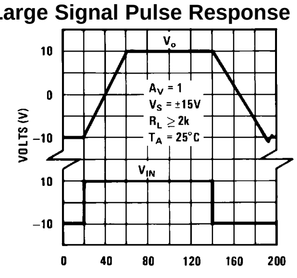
Open Loop Frequency Response



Bode Plot LM148

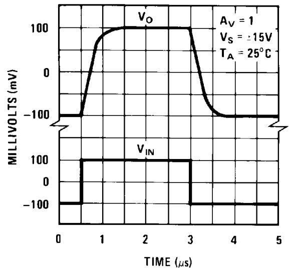


Large Signal Pulse Response (LM148)

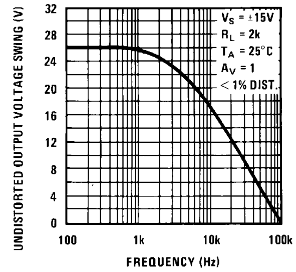


Typical Performance Characteristics (continued)

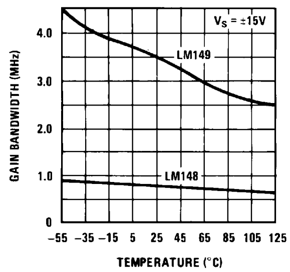
Small Signal Pulse Response (LM148)



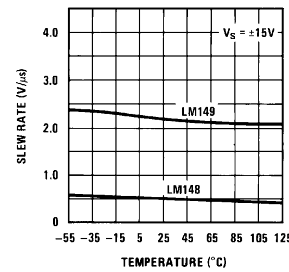
Undistorted Output Voltage Swing



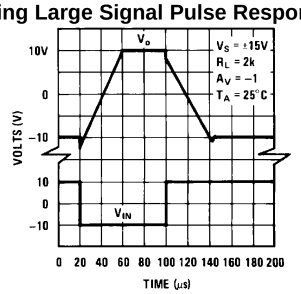
Gain Bandwidth



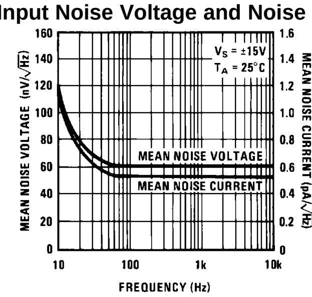
Slew Rate



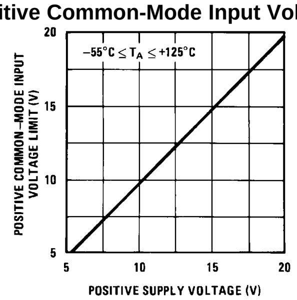
Inverting Large Signal Pulse Response (LM148)



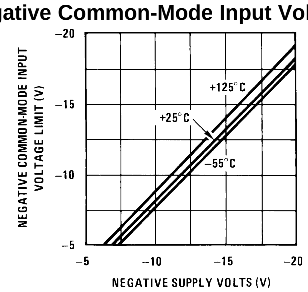
Input Noise Voltage and Noise Current



Positive Common-Mode Input Voltage Limit



Negative Common-Mode Input Voltage Limit



Application Hints

The LM148 series are quad low power LM741 op amps. In the proliferation of quad op amps, these are the first to offer the convenience of familiar, easy to use operating characteristics of the LM741 op amp. In those applications where LM741 op amps have been employed, the LM148 series op amps can be employed directly with no change in circuit performance.

The package pin-outs are such that the inverting input of each amplifier is adjacent to its output. In addition, the amplifier outputs are located in the corners of the package which simplifies PC board layout and minimizes package related capacitive coupling between amplifiers.

The input characteristics of these amplifiers allow differential input voltages which can exceed the supply voltages. In addition, if either of the input voltages is within the operating common-mode range, the phase of the output remains correct. If the negative limit of the operating common-mode range is exceeded at both inputs, the output voltage will be positive. For input voltages which greatly exceed the maximum supply voltages, either differentially or common-mode, resistors should be placed in series with the inputs to limit the current.

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Like the LM741, these amplifiers can easily drive a 100 pF capacitive load throughout the entire dynamic output voltage and current range. However, if very large capacitive loads must be driven by a non-inverting unity gain amplifier, a resistor should be placed between the output (and feedback connection) and the capacitance to reduce the phase shift resulting from the capacitive loading.

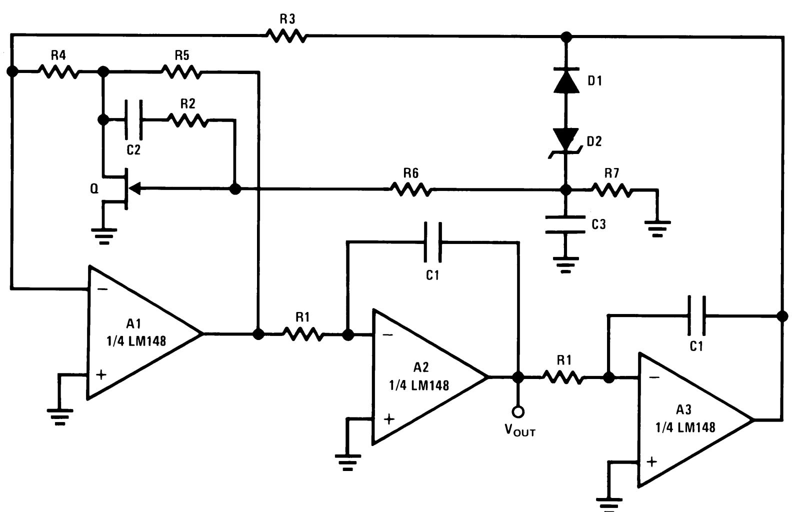
The output current of each amplifier in the package is limited. Short circuits from an output to either ground or the power supplies will not destroy the unit. However, if multiple output shorts occur simultaneously, the time duration should be short to prevent the unit from being destroyed as a result of excessive power dissipation in the IC chip.

As with most amplifiers, care should be taken lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize “pickup” and maximize the frequency of the feedback pole which capacitance from the input to ground creates.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately six times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

Typical Applications—LM148

Figure 3. One Decade Low Distortion Sinewave Generator



$$f = \frac{1}{2\pi R1C1} \times \sqrt{K},\ K = \frac{R4R5}{R3}\left(\frac{1}{r_{DS}} + \frac{1}{R4} + \frac{1}{R5}\right),\quad r_{DS} \approx \frac{R_{ON}}{\left(1 - \frac{V_{GS}}{V_P}\right)^{1/2}}$$

f_{MAX} = 5 kHz, THD ≤ 0.03%
R1 = 100k pot. C1 = 0.0047 μF, C2 = 0.01 μF, C3 = 0.1 μF, R2 = R6 = R7 = 1M,
R3 = 5.1k, R4 = 12Ω, R5 = 240Ω, Q = NS5102, D1 = 1N914, D2 = 3.6V avalanche
diode (ex. LM103), V_S = ±15V
A simpler version with some distortion degradation at high frequencies can be made by using A1 as a simple inverting amplifier, and by putting back to back zeners in the feedback loop of A3.

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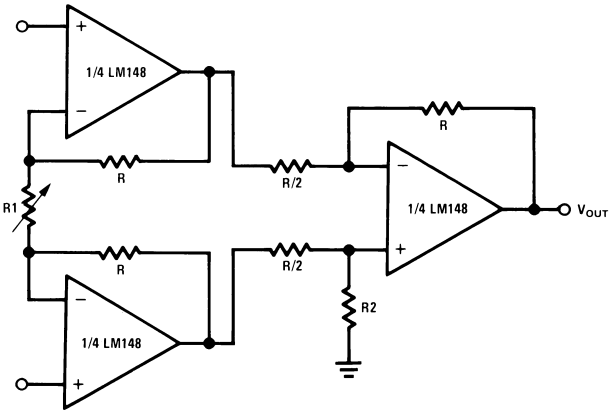
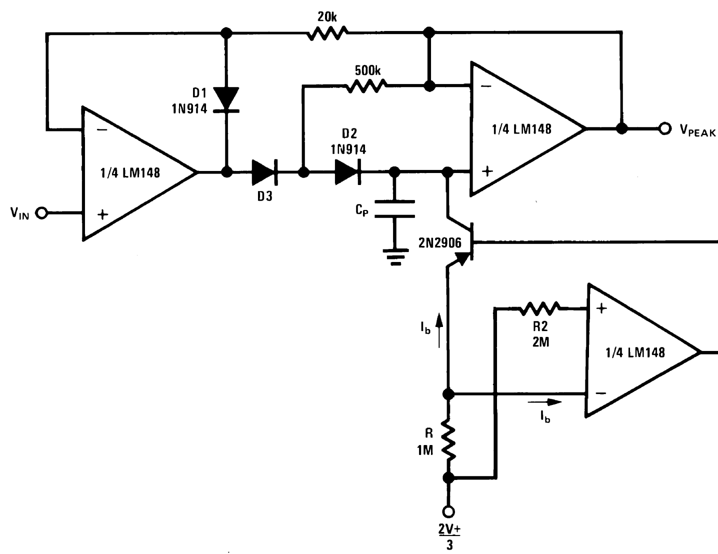
Figure 4. Low Cost Instrumentation Amplifier



$$V_{OUT} = 2\left(\frac{2R}{R1} + 1\right),\ V_S^- - 3V \le V_{IN\,CM} \le V_S^+ - 3V,$$

$V_S = \pm 15V$
R = R2, trim R2 to boost CMRR

Figure 5. Low Drift Peak Detector with Bias Current Compensation



Adjust R for minimum drift
D3 low leakage diode
D1 added to improve speed
$V_S = \pm 15V$

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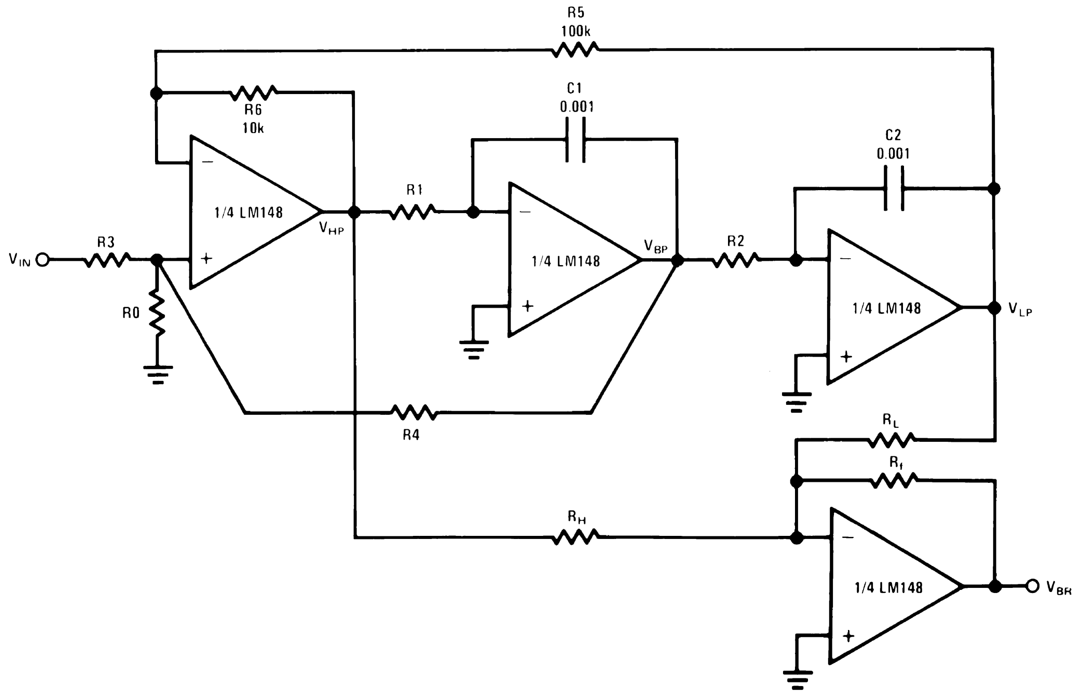
Figure 6. Universal State-Variable Filter



Tune Q through R0,
For predictable results: $f_O\ Q \le 4 \times 10^4$
Use Band Pass output to tune for Q

$$\frac{V_{(s)}}{V_{IN(s)}} = \frac{N_{(s)}}{D_{(s)}},\ D(s) = S^2 + \frac{S\omega_o}{Q} + \omega_o^2$$

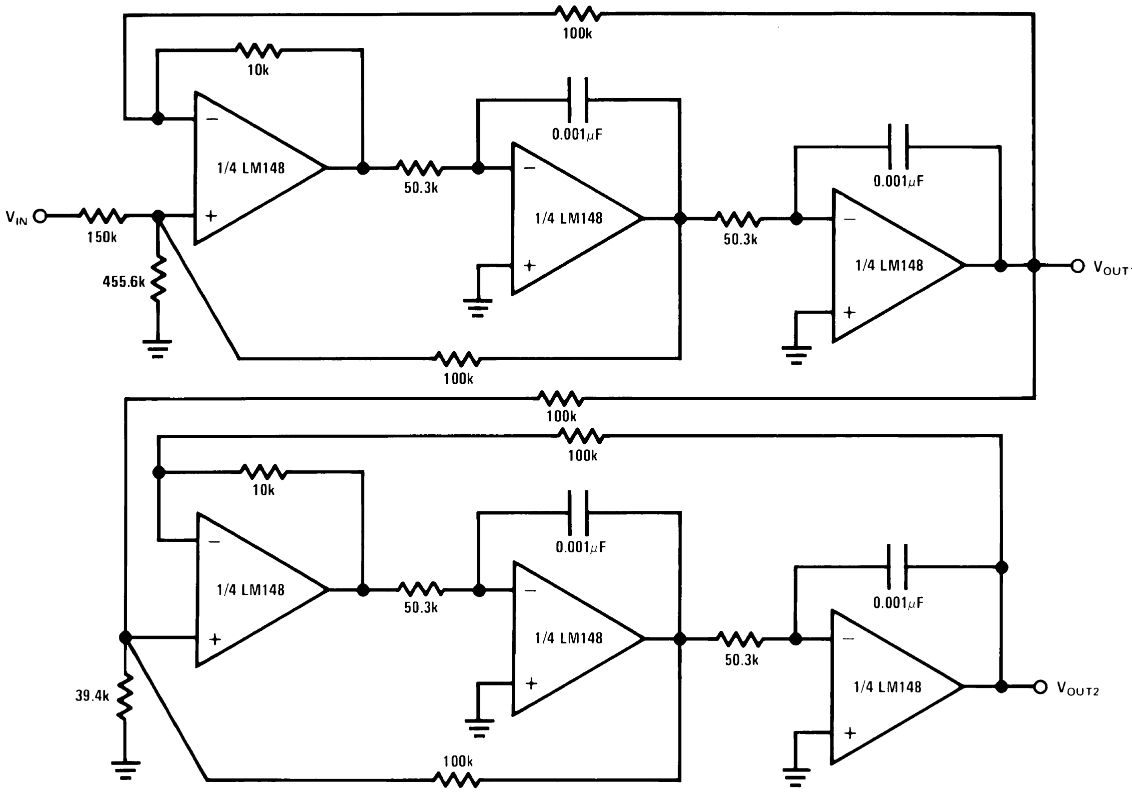
$$N_{HP(s)} = S^2 H_{OHP},\ N_{BP(s)} = \frac{-s\omega_O H_{OBP}}{Q}\quad N_{LP} = \omega_o^2 H_{OLP}.$$

$$f_o = \frac{1}{2\pi}\sqrt{\frac{R6}{R5}}\sqrt{\frac{1}{t1t2}},\ t_i = R_iC_i,\ Q = \left(\frac{1 + R4|R3 + R4|R0}{1 + R6|R5}\right)\left(\frac{R6}{R5}\frac{t_1}{t_2}\right)^{1/2}$$

$$f_{NOTCH} = \frac{1}{2\pi}\left(\frac{R_H}{R_L\ t_1\ t_2}\right)^{1/2},\ H_{OHP} = \frac{1 + R6|R5}{1 + R3|R0 + R3|R4},\ H_{OBP} = \frac{1 + R4|R3 + R4|R0}{1 + R3|R0 + R3|R4}$$

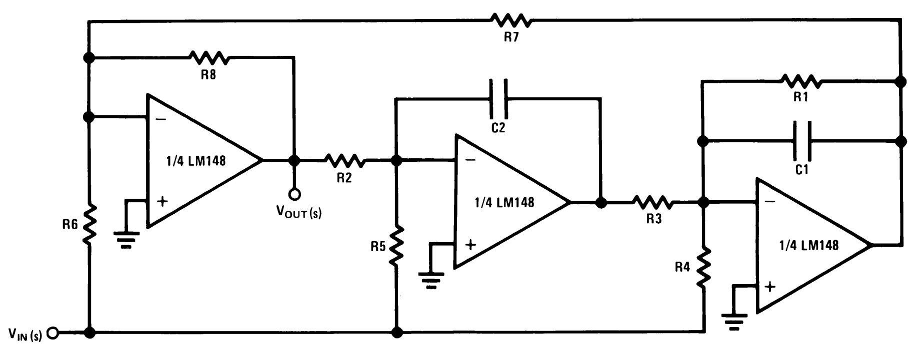
$$H_{OLP} = \frac{1 + R5|R6}{1 + R3|R0 + R3|R4}$$

Figure 7. A 1 kHz 4 Pole Butterworth



Use general equations, and tune each section separately
$Q_{1stSECTION} = 0.541$, $Q_{2ndSECTION} = 1.306$
The response should have 0 dB peaking

Figure 8. A 3 Amplifier Bi-Quad Notch Filter



$$Q = \sqrt{\frac{R8}{R7}} \times \frac{R1C1}{\sqrt{R3C2R2C1}},\ f_o = \frac{1}{2\pi}\sqrt{\frac{R8}{R7}} \times \frac{1}{\sqrt{R2R3C1C2}},\ f_{NOTCH} = \frac{1}{2\pi}\sqrt{\frac{R6}{R3R5R7C1C2}}$$

Necessary condition for notch: $\frac{1}{R6} = \frac{R1}{R4R7}$

Ex: f_{NOTCH} = 3 kHz, Q = 5, R1 = 270k, R2 = R3 = 20k, R4 = 27k, R5 = 20k, R6 = R8 = 10k, R7 = 100k, C1 = C2 = 0.001 µF
Better noise performance than the state-space approach.

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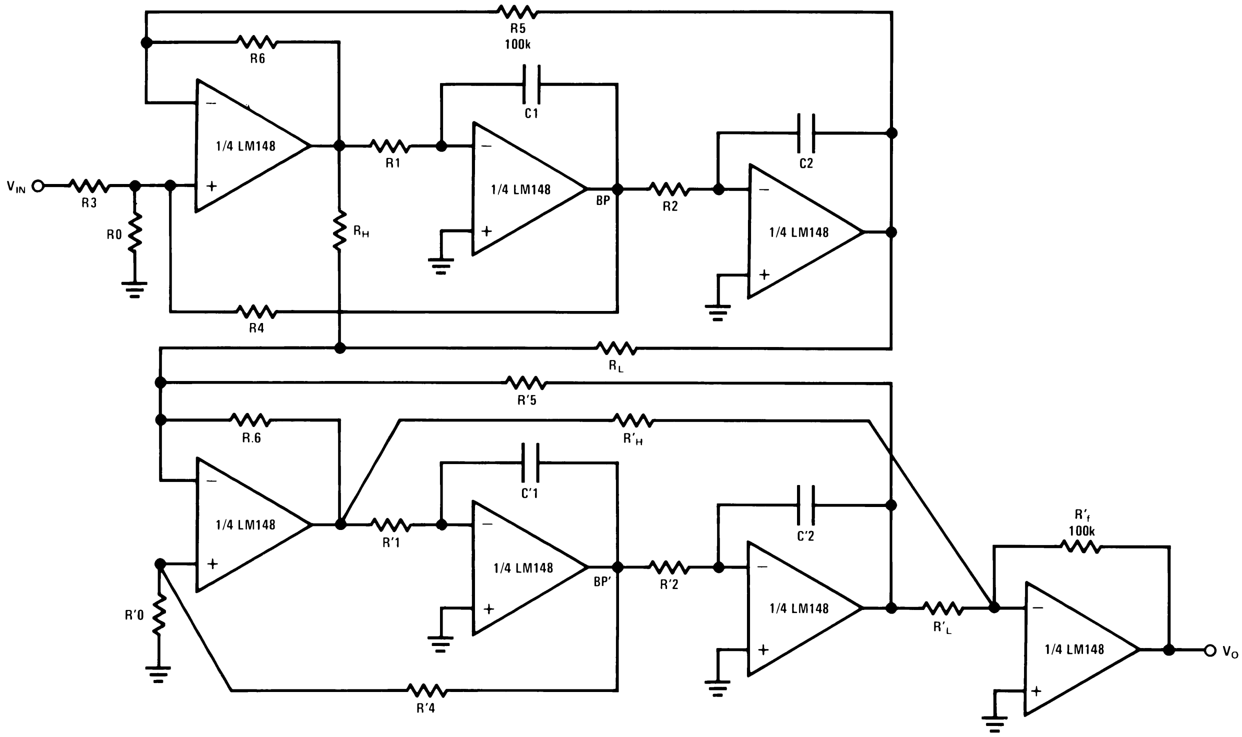
Figure 9. A 4th Order 1 kHz Elliptic Filter (4 Poles, 4 Zeros)



R1C1 = R2C2 = t

R′1C′1 = R′2C′2 = t′

f_C = 1 kHz, f_S = 2 kHz, f_p = 0.543, f_Z = 2.14, Q = 0.841, f'_P = 0.987, f'_Z = 4.92, Q′ = 4.403, normalized to ripple BW

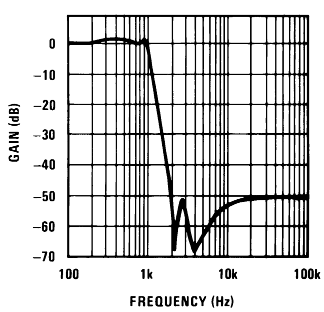
$$f = \frac{1}{2\pi R1C1} \times \sqrt{K},\ K = \frac{R4R5}{R3}\left(\frac{1}{r_{DS}} + \frac{1}{R4} + \frac{1}{R5}\right),\quad r_{DS} \approx \frac{R_{ON}}{\left(1 - \frac{V_{GS}}{V_P}\right)^{1/2}}$$

Use the BP outputs to tune Q, Q′, tune the 2 sections separately

R1 = R2 = 92.6k, R3 = R4 = R5 = 100k, R6 = 10k, R0 = 107.8k, R_L = 100k, R_H = 155.1k,

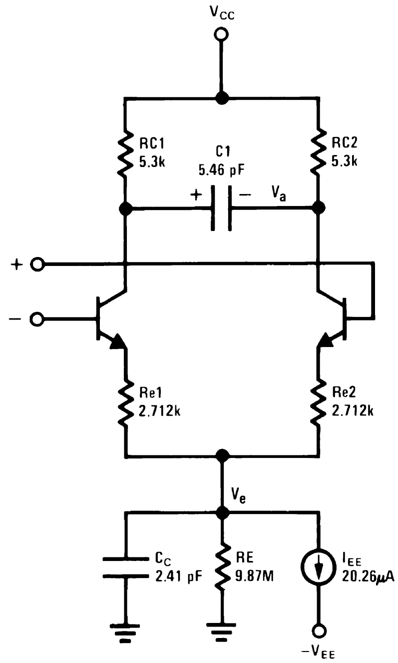
R′1 = R′2 = 50.9k, R′4 = R′5 = 100k, R′6 = 10k, R′0 = 5.78k, R'_L = 100k, R'_H = 248.12k, R′f = 100k. All capacitors are 0.001 μF.

Figure 10. Lowpass Response



Typical Simulation

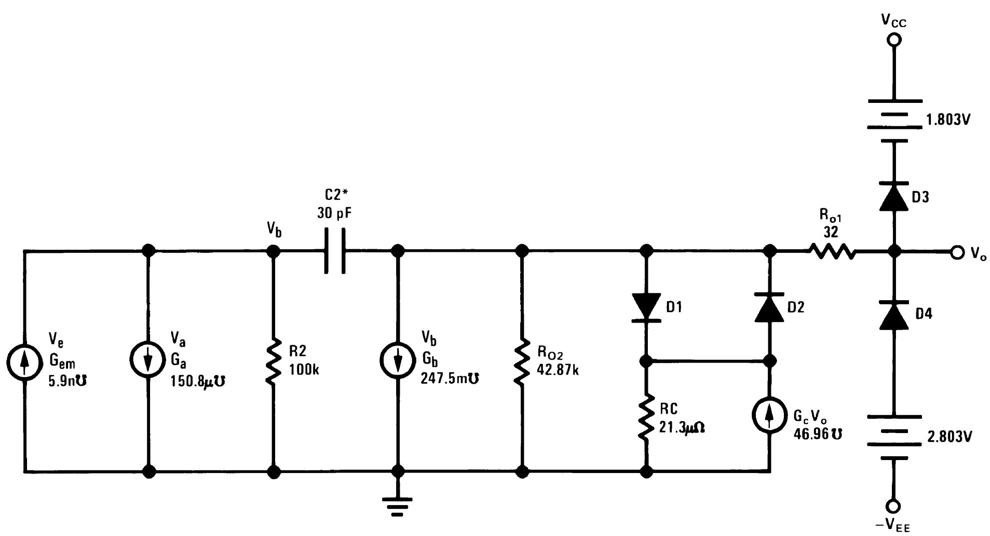
Figure 11. LM148, LM741 Macromodel for Computer Simulation



For more details, see IEEE Journal of Solid-State Circuits, Vol. SC-9, No. 6, December 1974

$_{o1}$ = $112I_S = 8 \times 10^{-16}$

$_{o2}$ = 144*C2 = 6 pF for LM149



Revision History Section

Date Released	Revision	Section	Originator	Changes
02/08/05	A	New Release, Corporate format	L. Lytle	1 MDS data sheet converted into one Corp. data sheet format. MNLM148-X, Rev. 2A2. MDS data sheet will be archived.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
LM148J/883	ACTIVE	CDIP	J	14	25	TBD	A42 SNPB	Level-1-NA-UNLIM	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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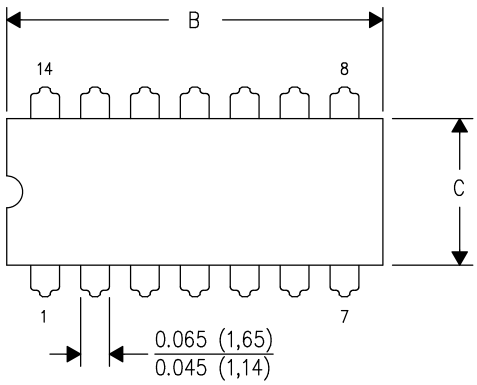
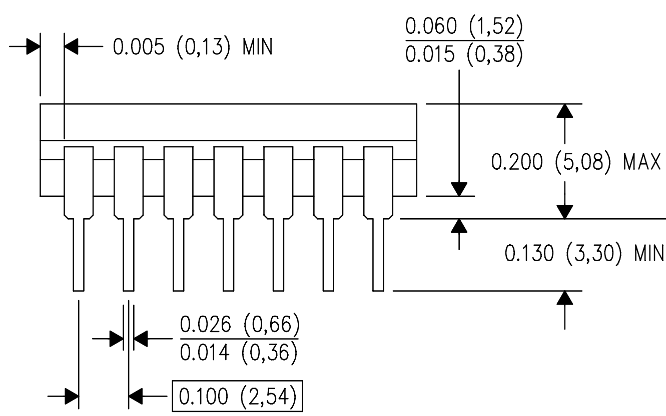
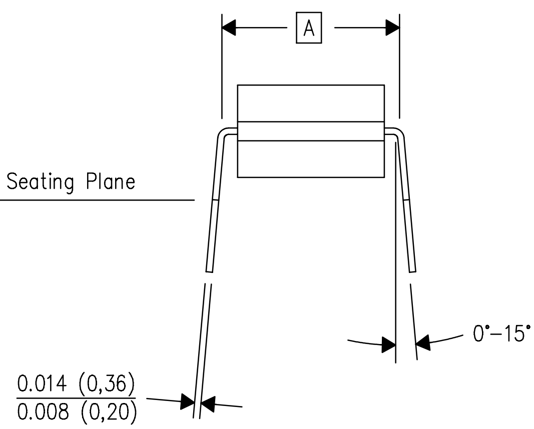
J (R–GDIP–T**) CERAMIC DUAL IN–LINE PACKAGE

14 LEADS SHOWN



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)





4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

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