

LM118QML Operational Amplifier

Check for Samples: [LM118QML](#)

FEATURES

- 15 MHz small signal bandwidth
- Guaranteed 50V/ μ s slew rate
- Maximum bias current of 250 nA
- Operates from supplies of ± 5 V to ± 20 V
- Internal frequency compensation
- Input and output overload protected
- Pin compatible with general purpose op amps

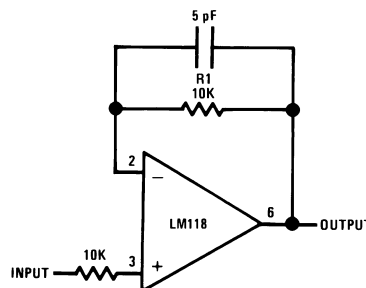
DESCRIPTION

The LM118 is a precision high speed operational amplifier designed for applications requiring wide bandwidth and high slew rate. It features a factor of ten increase in speed over general purpose devices without sacrificing DC performance.

The LM118 has internal unity gain frequency compensation. This considerably simplifies its application since no external components are necessary for operation. However, unlike most internally compensated amplifiers, external frequency compensation may be added for optimum performance. For inverting applications, feed forward compensation will boost the slew rate to over 150V/ μ s and almost double the bandwidth. Overcompensation can be used with the amplifier for greater stability when maximum bandwidth is not needed. Further, a single capacitor can be added to reduce the 0.1% settling time to under 1 μ s.

The high speed and fast settling time of this op amp makes it useful in A/D converters, oscillators, active filters, sample and hold circuits, or general purpose amplifiers. This device is easy to apply and offers an order of magnitude better AC performance than industry standards such as the LM709.

Fast Voltage Follower



Do not hard-wire as voltage follower ($R1 \geq 5 \text{ k}\Omega$)



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Connection Diagram

Dual-In-Line Package

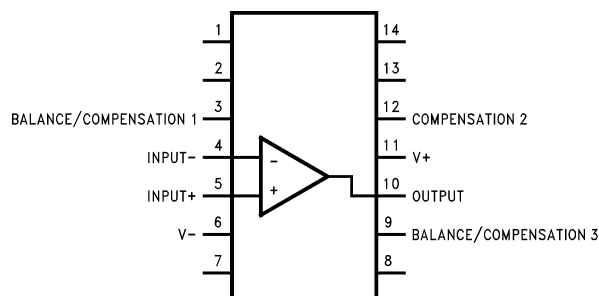


Figure 1. Top View

Dual-In-Line Package

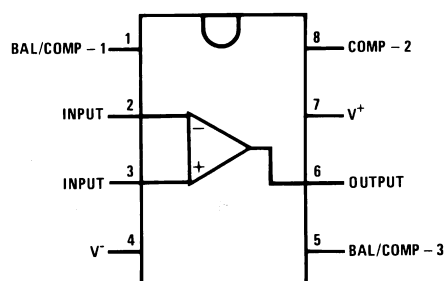
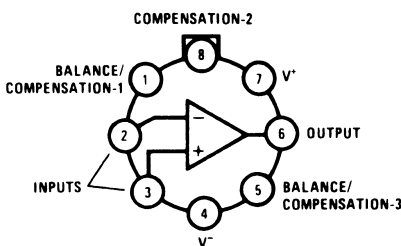


Figure 2. Top View

Metal Can Package



(1) Pin connections shown on schematic diagram and typical applications are for TO-5 package.

Figure 3. Top View

Ceramic SOIC Package

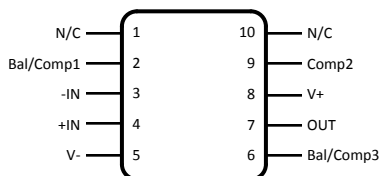
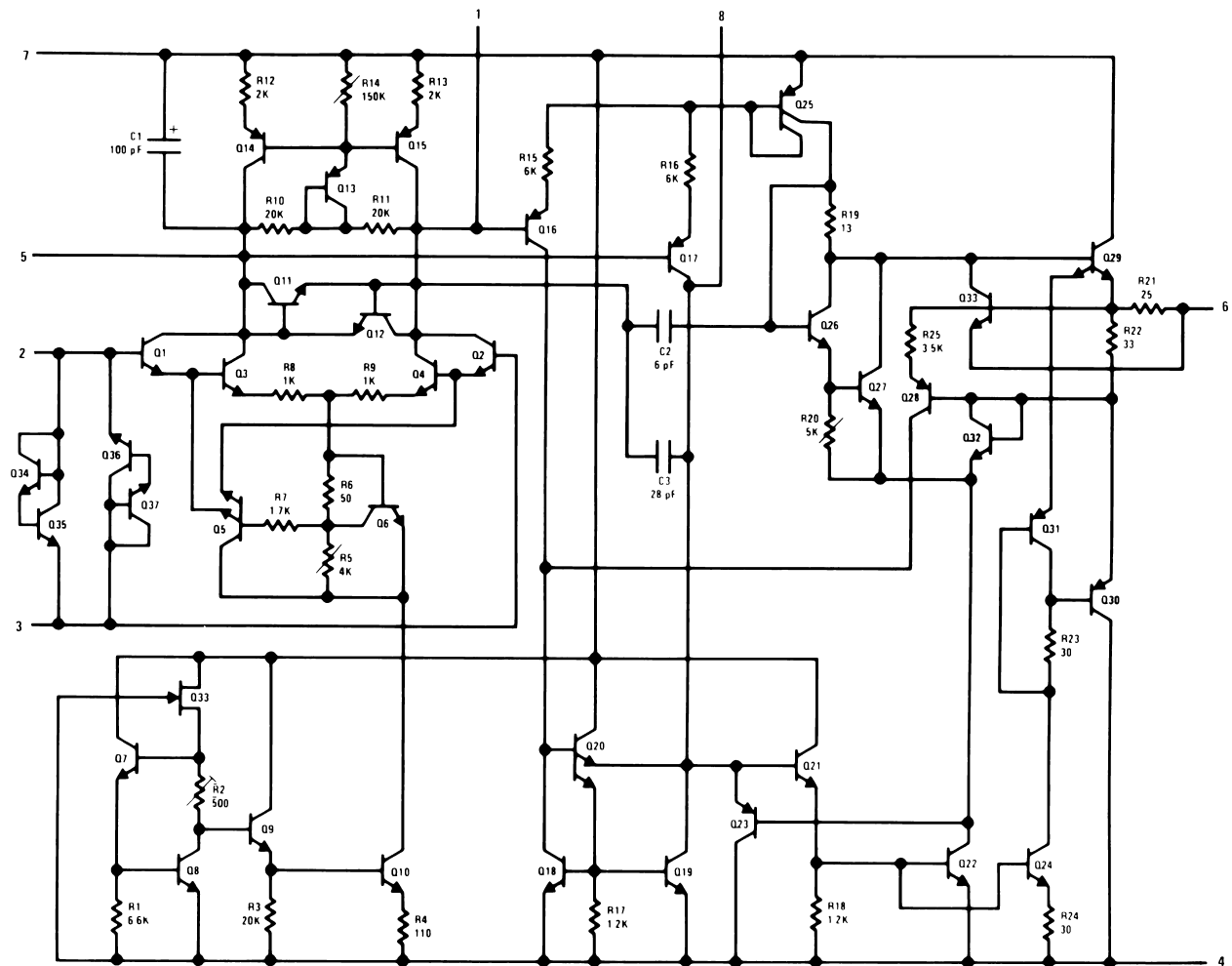


Figure 4. Top View

Schematic Diagram



Absolute Maximum Ratings ⁽¹⁾

Supply Voltage	±20V
Power Dissipation ⁽²⁾	
8 LD Metal Can	750mW
8LD CERDIP	1000mW
14LD CERDIP	1250mW
10LD Ceramic SOIC	600mW
Differential Input Current ⁽³⁾	±10 mA
Input Voltage ⁽⁴⁾	±15V
Output Short-Circuit Duration	Continuous
Operating Temperature Range	-55°C ≤ T _A ≤ +125°C
Thermal Resistance	
θ _{JA}	
8 LD Metal Can (Still Air @ 0.5W)	160°C/W
8 LD Metal Can (500LF / Min Air flow @ 0.5W)	86°C/W
8LD CERDIP (Still Air @ 0.5W)	120°C/W
8LD CERDIP (500LF / Min Air flow @ 0.5W)	66°C/W
14LD CERDIP (Still Air @ 0.5W)	87°C/W
14LD CERDIP (500LF / Min Air flow @ 0.5W)	51°C/W
10LD Ceramic SOIC (Still Air @ 0.5W)	198°C/W
10LD Ceramic SOIC (500LF / Min Air flow @ 0.5W)	124°C/W
θ _{JC}	
8 LD Metal Can	48°C/W
8LD CERDIP	17°C/W
14LD CERDIP	17°C/W
10LD Ceramic SOIC	22°C/W
Storage Temperature Range	-65°C ≤ T _A ≤ +150°C
Lead Temperature (Soldering, 10 seconds)	300°C
ESD Tolerance ⁽⁵⁾	2000V

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For specifications and test conditions, see the Electrical Characteristics. The specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
- (2) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax} (maximum junction temperature), θ_{JA} (package junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is P_{Dmax} = (T_{Jmax} - T_A)/θ_{JA} or the number given in the Absolute Maximum Ratings, whichever is lower.
- (3) The inputs are shunted with back-to-back diodes for over voltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1V is applied between the inputs unless some limiting resistance is used.
- (4) For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
- (5) Human body model, 1.5 kΩ in series with 100 pF.

Quality Conformance Inspection

Mil-Std-883, Method 5005; Group A

Subgroup	Description	Temp°C
1	Static tests at	25
2	Static tests at	125
3	Static tests at	-55
4	Dynamic tests at	25
5	Dynamic tests at	125
6	Dynamic tests at	-55
7	Functional tests at	25
8A	Functional tests at	125
8B	Functional tests at	-55
9	Switching tests at	25
10	Switching tests at	125
11	Switching tests at	-55
12	Settling time at	25
13	Settling time at	125
14	Settling time at	-55

LM118 883 Electrical Characteristics DC Parameters

The following conditions apply, unless otherwise specified.

DC $V_{CC} = \pm 15V$, $V_{CM} = 0V$

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
V_{IO}	Input Offset Voltage	$V_{CM} = \pm 11.5V$, $R_S = 50\Omega$		-4.0	+4.0	mV	1
				-6.0	+6.0	mV	2, 3
		$V_{CC} = \pm 20V$, $R_S = 50\Omega$		-4.0	+4.0	mV	1
				-6.0	+6.0	mV	2, 3
		$V_{CC} = \pm 20V$, $V_{CM} = \pm 15V$, $R_S = 50\Omega$		-4.0	+4.0	mV	1
				-6.0	+6.0	mV	2, 3
I_{IO}	Input Offset Current	$V_{CM} = \pm 11.5V$, $R_S = 10K\Omega$		-50	+50	nA	1
				-100	+100	nA	2, 3
		$V_{CC} = \pm 20V$, $R_S = 10K\Omega$		-50	+50	nA	1
				-100	+100	nA	2, 3
		$V_{CC} = \pm 5V$, $R_S = 10K\Omega$		-50	+50	nA	1
				-100	+100	nA	2, 3
I_{IB}	Input Bias Current	$V_{CM} = \pm 11.5V$, $R_S = 10K\Omega$		1.0	250	nA	1
				1.0	500	nA	2, 3
		$V_{CC} = \pm 20V$, $R_S = 10K\Omega$		1.0	250	nA	1
				1.0	500	nA	2, 3
		$V_{CC} = \pm 5V$, $R_S = 10K\Omega$		1.0	250	nA	1
				1.0	500	nA	2, 3
PSRR	Power Supply Rejection Ratio	$+V_{CC} = 20V$ to $5V$, $R_S = 50\Omega$		70		dB	1, 2, 3
		$-V_{CC} = -20V$ to $-5V$, $R_S = 50\Omega$		70		dB	1, 2, 3
CMRR	Common Mode Rejection Ratio	$V_{CC} = \pm 15V$, $V_{CM} = \pm 11.5V$, $R_S = 50\Omega$		80		dB	1, 2, 3
$+I_{OS}$	Short Circuit Current	$t < 25mS$		-65	-5.0	mA	1, 2, 3
$-I_{OS}$	Short Circuit Current	$t < 25mS$		5.0	65	mA	1, 2
				5.0	80	mA	3
I_{CC}	Power Supply Current	$V_{CC} = \pm 20V$			8.0	mA	1
					7.0	mA	2
					11	mA	3
$V_{IO\ adj.}$	Input Offset Voltage Adjust	$V_{CC} = \pm 20V$		4.0	-4.0	mV	1
R_I	Input Resistance		(1)	1.0		M Ω	1
V_I	Input Voltage Range	$V_{CC} = \pm 15V$	(2)	-11.5	+11.5	V	1, 2, 3
A_{VS}	Large Signal Voltage Gain	$R_L = 2K\Omega$, $V_O = 0$ to $-10V$	(3)	50		V/mV	4
			(3)	25		V/mV	5, 6
		$R_L = 2K\Omega$, $V_O = 0$ to $+10V$	(3)	50		V/mV	4
			(3)	25		V/mV	5, 6
V_O	Output Voltage Swing	$R_L = 2K\Omega$		+12	-12	V	4, 5, 6

(1) Specified by design not tested

(2) Specified by CMRR

(3) Datalog in K = V/mV

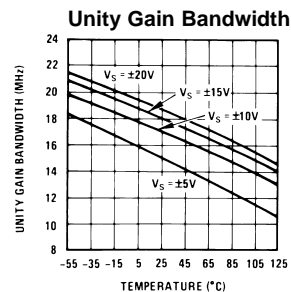
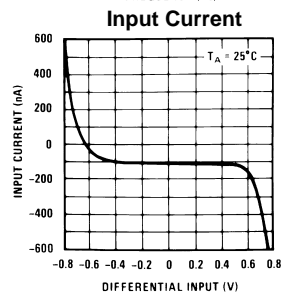
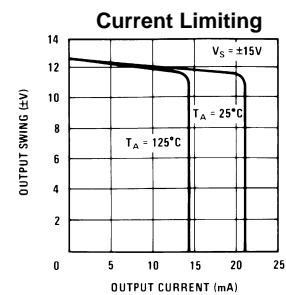
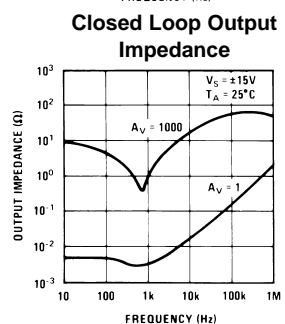
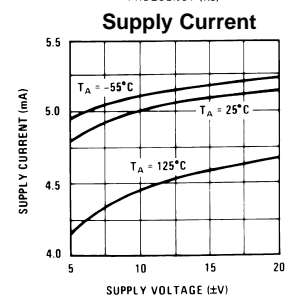
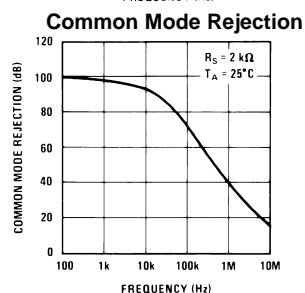
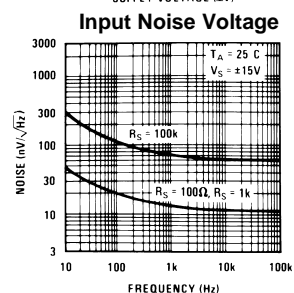
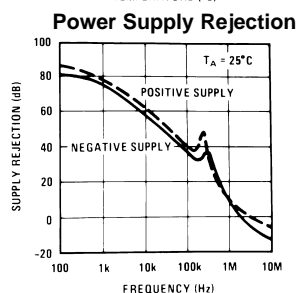
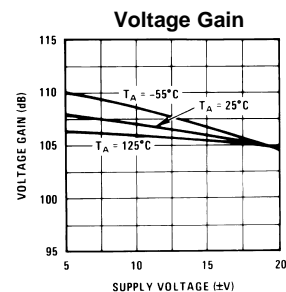
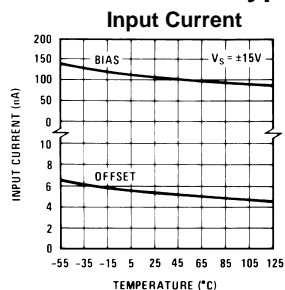
LM118 883 Electrical Characteristics AC Parameters

The following conditions apply parameters, unless otherwise specified.

AC $V_{CC} = \pm 15V$, $V_{CM} = 0V$, $R_S = 0\Omega$, $R_L = 2K\Omega$, $C_L = 33pF$

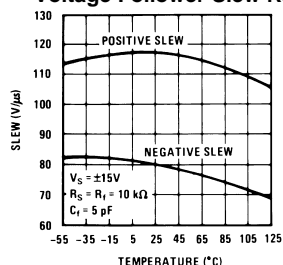
Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
S_R	Slew Rate	$V_{CC} = \pm 20V$, $V_I = -5V$ to $+5V$, $A_V=1$		50		V/ μ S	7
		$V_{CC} = \pm 20V$, $V_I = +5V$ to $-5V$, $A_V=1$		50		V/ μ S	7

Typical Performance Characteristics

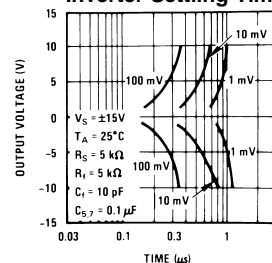


Typical Performance Characteristics (continued)

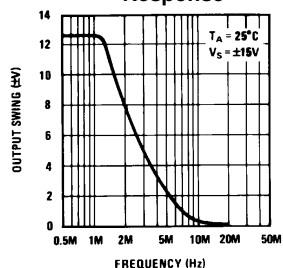
Voltage Follower Slew Rate



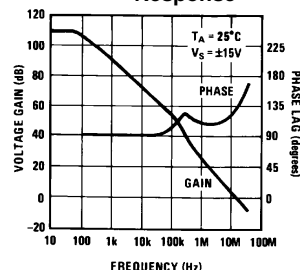
Inverter Settling Time



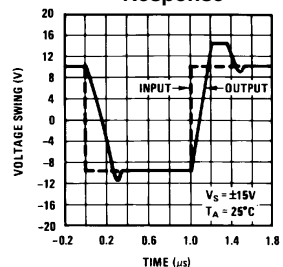
Large Signal Frequency Response



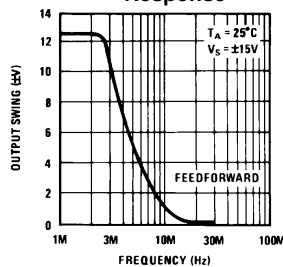
Open Loop Frequency Response



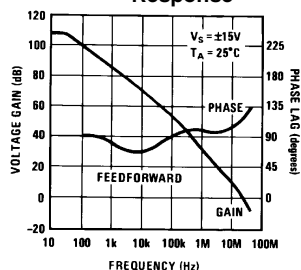
Voltage Follower Pulse Response



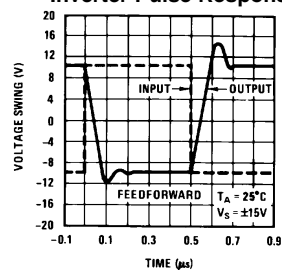
Large Signal Frequency Response



Open Loop Frequency Response

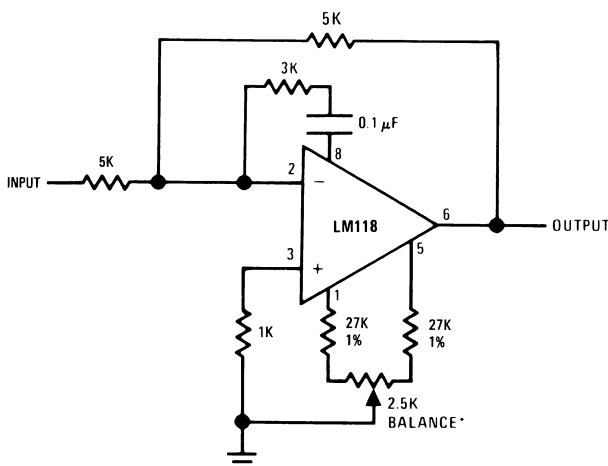


Inverter Pulse Response



Auxiliary Circuits

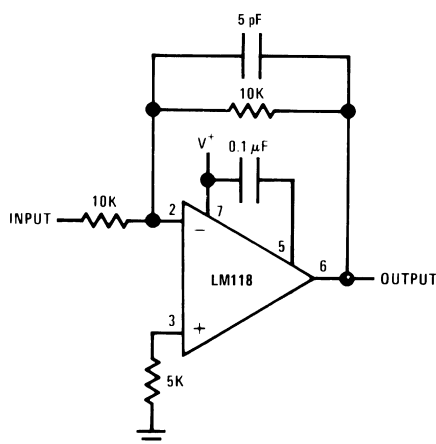
Figure 5. Feedforward Compensation for Greater Inverting Slew Rate



*Balance circuit necessary for increased slew.

Slew rate typically 150V/μs.

Figure 6. Compensation for Minimum Settling Time



- (1) Slew and settling time to 0.1% for a 10V step change is 800 ns.

Figure 7. Offset Balancing

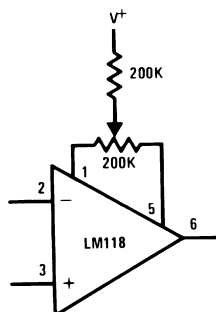


Figure 8. Isolating Large Capacitive Loads

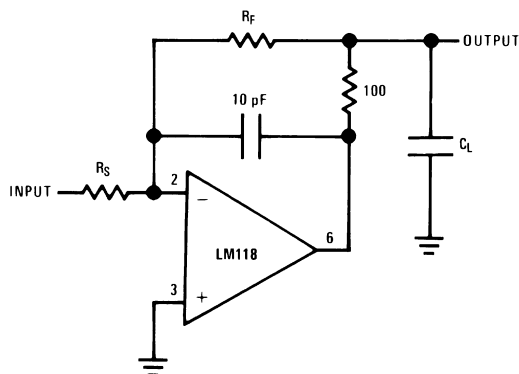
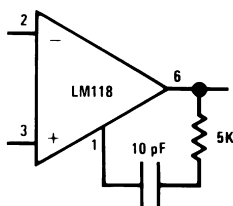


Figure 9. Overcompensation



Typical Applications

Figure 10. Fast Voltage Follower

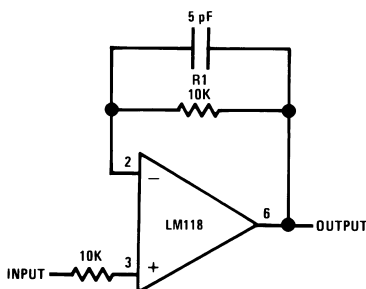
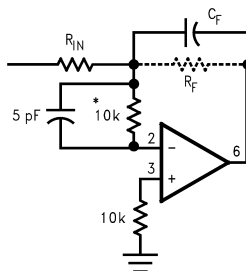


Figure 11. Integrator or Slow Inverter



$C_F = \text{Large}$

($C_F \geq 50 \text{ pF}$)

*Do not hard-wire as integrator or slow inverter; insert a 10k-5 pF network in series with the input, to prevent oscillation.

- (1) Do not hard-wire as voltage follower ($R_1 \geq 5 \text{ k}\Omega$)

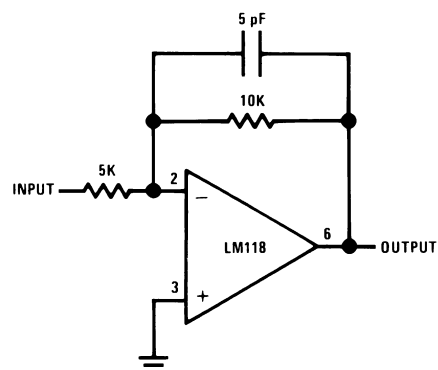
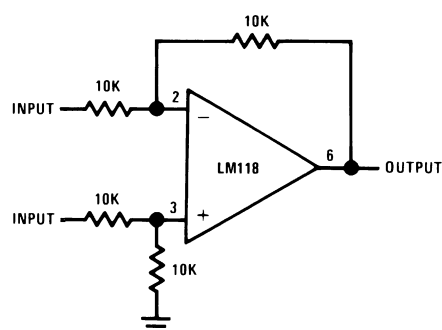
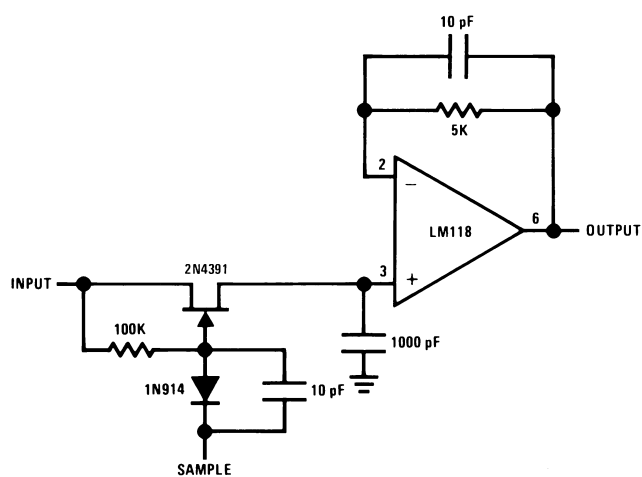
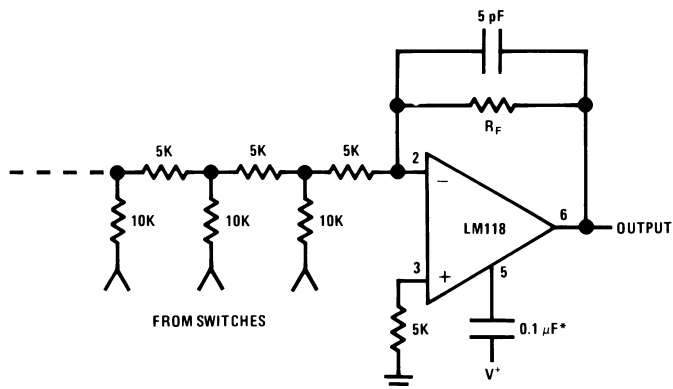
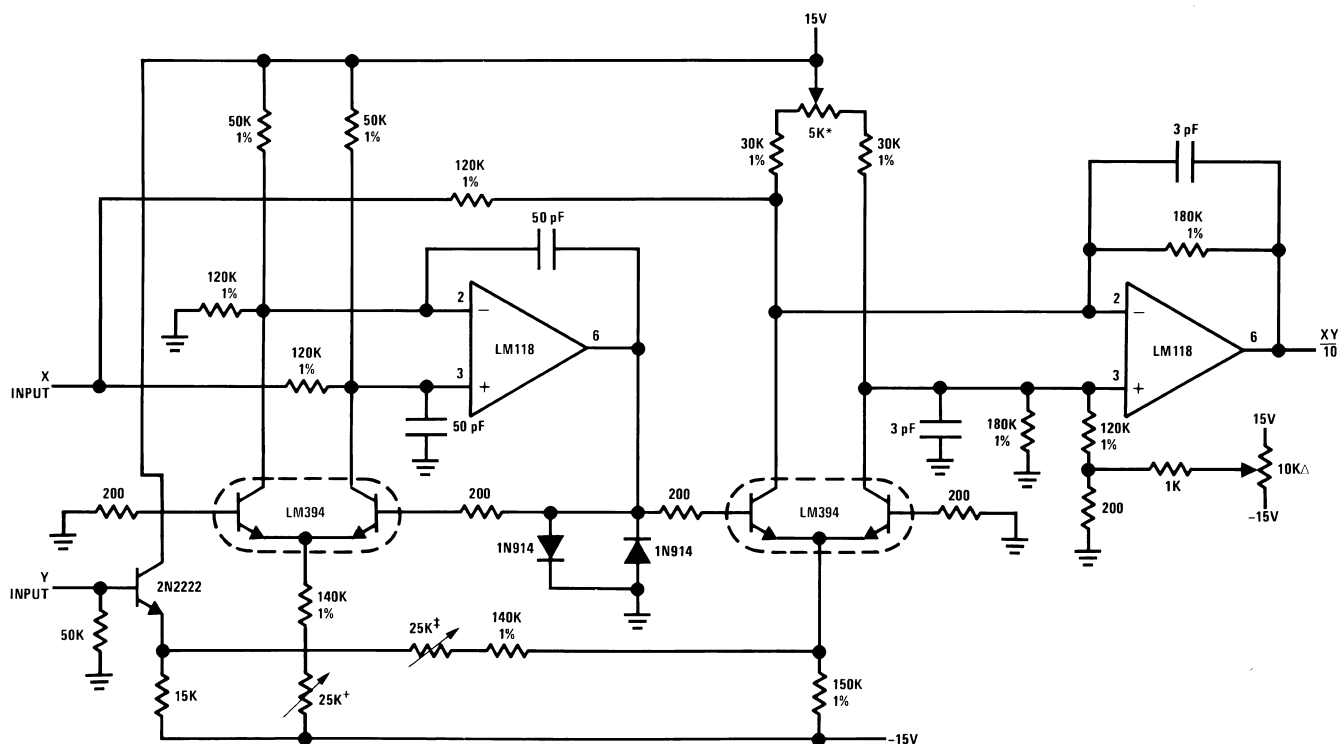
Figure 12. Fast Summing Amplifier**Figure 13. Differential Amplifier****Figure 14. Fast Sample and Hold**

Figure 15. D/A Converter Using Ladder Network



*Optional—Reduces settling time.

Figure 16. Four Quadrant Multiplier

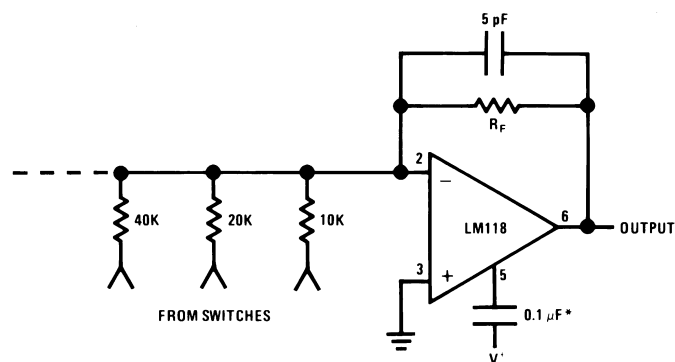


ΔOutput zero.

*"Y" zero

+ "X" zero

‡Full scale adjust.

Figure 17. D/A Converter Using Binary Weighted Network

*Optional—Reduces settling time.

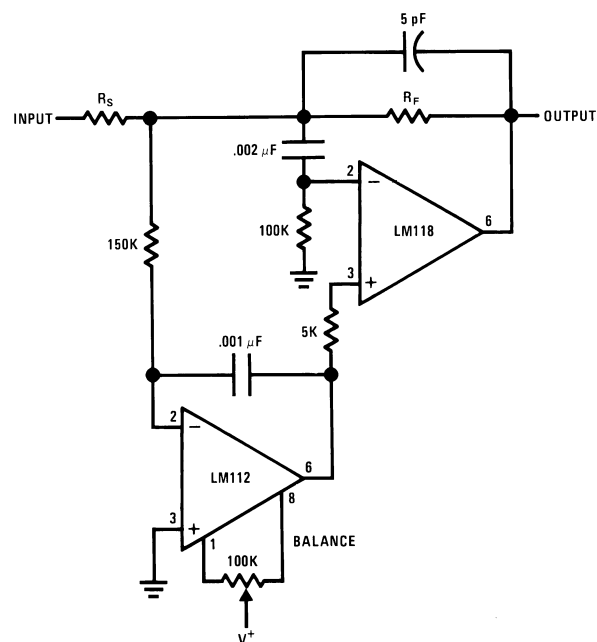
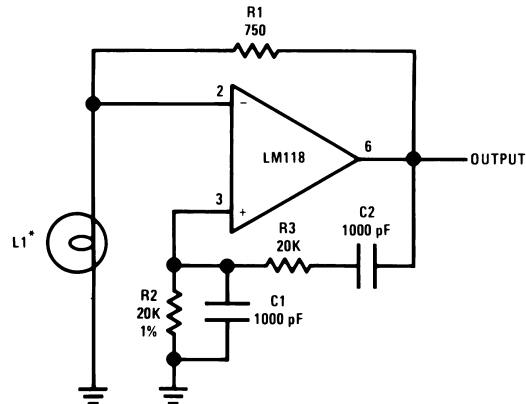
Figure 18. Fast Summing Amplifier with Low Input Current

Figure 19. Wein Bridge Sine Wave Oscillator

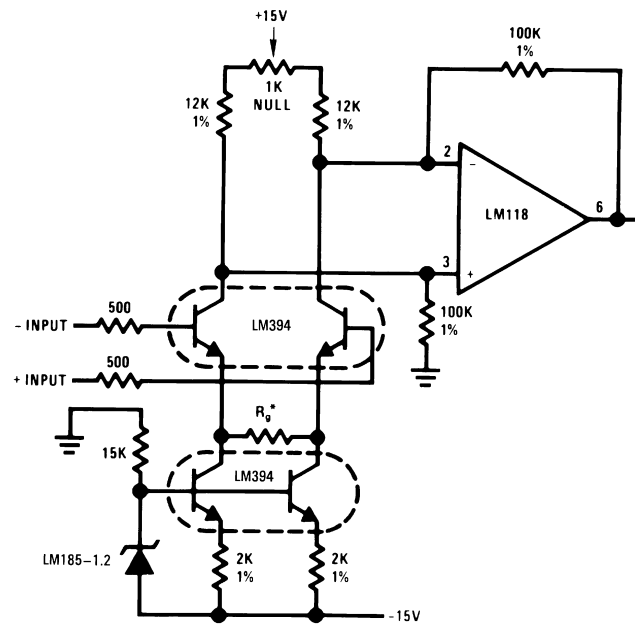


*L1—10V—14 mA bulb ELDEMA 1869

$$R1 = R2$$
$$C1 = C2$$

$$f = \frac{1}{2\pi R_2 C_1}$$

Figure 20. Instrumentation Amplifier



$$*Gain \geq \frac{200K}{R_g} \text{ for } 1.5K \leq R_g \leq 200K$$

REVISION HISTORY SECTION

Date Released	Revision	Section	Originator	Changes
07/12/05	A	New Release, Corporate format	L. Lytle	1 MDS data sheet, MNLM118–X Rev 0A0 was converted into the Corp. datasheet format. MDS datasheet will be archived.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
LM118H/883	ACTIVE	TO-99	LMC	8	20	TBD	POST-PLATE	Level-1-NA-UNLIM	
LM118J-8/883	ACTIVE	CDIP	NAB	8	40	TBD	A42 SNPB	Level-1-NA-UNLIM	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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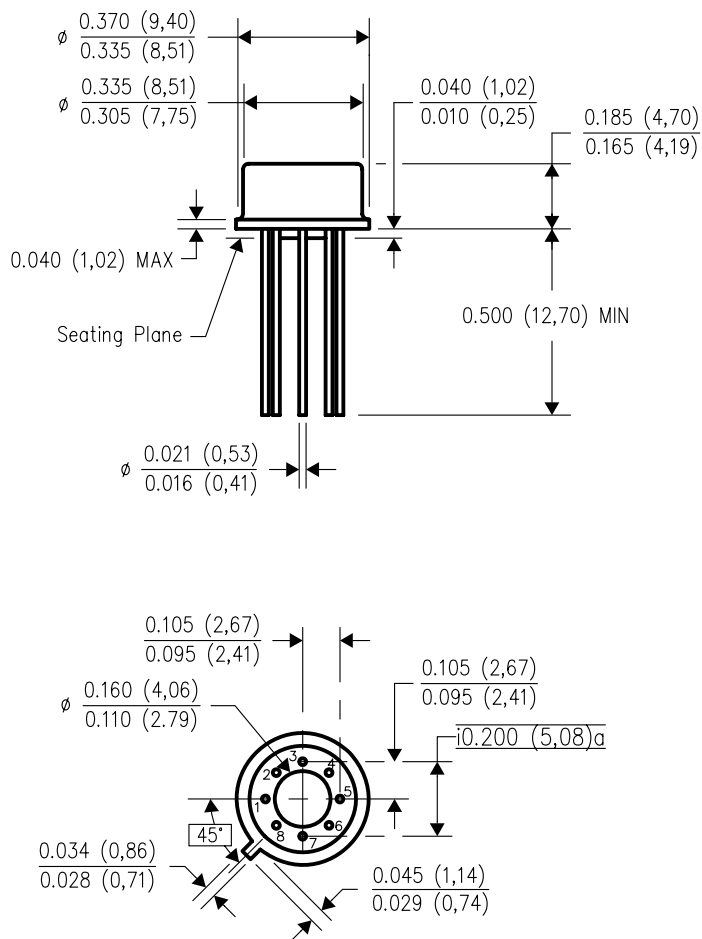
CONTROLLING DIMENSION IS INCH
VALUES IN [] ARE MILLIMETERS



J08A (Rev M)

LMC (O-MBCY-W8)

METAL CYLINDRICAL PACKAGE



4202483/B 09/07

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - Leads in true position within 0.010 (0,25) R @ MMC at seating plane.
 - Pin numbers shown for reference only. Numbers may not be marked on package.
 - Falls within JEDEC MO-002/T0-99.

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