

LM101AJAN Operational Amplifiers

Check for Samples: [LM101AJAN](#)

FEATURES

- Offset voltage 3 mV maximum over temperature
- Input current 100 nA maximum over temperature
- Offset current 20 nA maximum over temperature
- Guaranteed drift characteristics
- Offsets guaranteed over entire common mode and supply voltage ranges
- Slew rate of 10 V/ μ S as a summing amplifier

DESCRIPTION

The LM101A is a general purpose operational amplifier which features improved performance over industry standards such as the LM709. Advanced processing techniques make possible an order of magnitude reduction in input currents, and a redesign of the biasing circuitry reduces the temperature drift of input current. Improved specifications include:

- Offset voltage 3 mV maximum over temperature
- Input current 100 nA maximum over temperature
- Offset current 20 nA maximum over temperature
- Guaranteed drift characteristics
- Offsets guaranteed over entire common mode and supply voltage ranges
- Slew rate of 10V/ μ s as a summing amplifier
 - This amplifier offers many features which make its application nearly foolproof: overload protection on the input and output, no latch-up when the common mode range is exceeded, and freedom from oscillations and compensation with a single 30 pF capacitor. It has advantages over internally compensated amplifiers in that the frequency compensation can be tailored to the particular application. For example, in low frequency circuits it can be overcompensated for increased stability margin. Or the compensation can be optimized to give more than a factor of ten improvement in high frequency performance for most applications.
 - In addition, the device provides better accuracy and lower noise in high impedance circuitry. The low input currents also make it particularly well suited for long interval integrators or timers, sample and hold circuits and low frequency waveform generators. Further, replacing circuits where matched transistor pairs buffer the inputs of conventional IC op amps, it can give lower offset voltage and a drift at a lower cost.



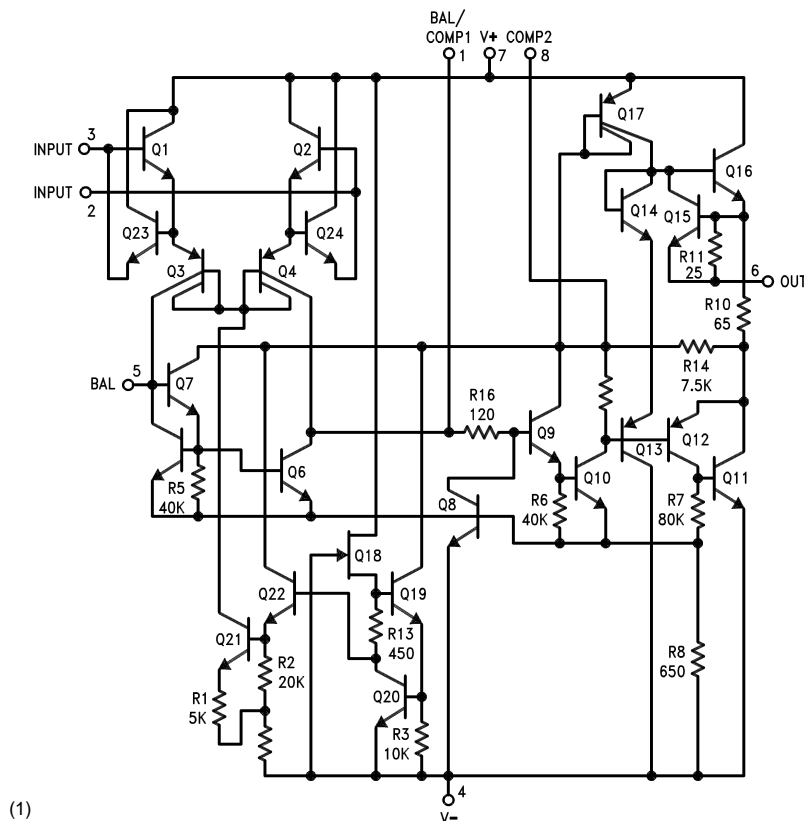
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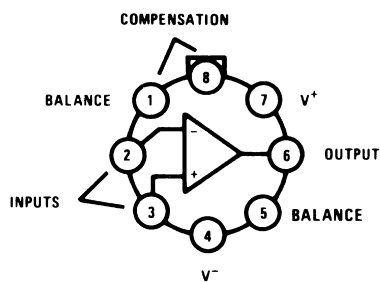
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Schematic



Connection Diagrams



Note: Pin 4 connected to case.

Figure 1. Metal Can Package – Top View

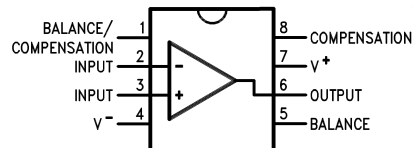


Figure 2. Dual-In-Line Package – Top View

(1) Pin connections shown are for 8-pin packages.

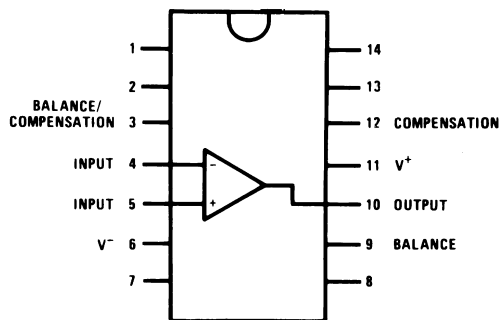


Figure 3. Dual-In-Line Package – Top View

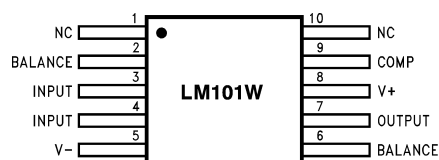
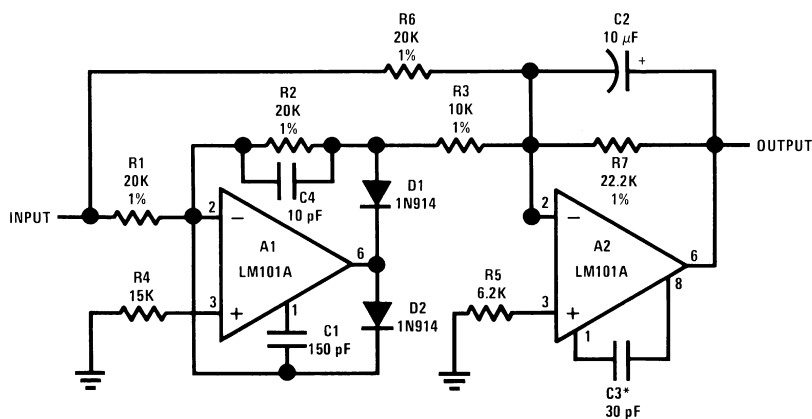


Figure 4. Ceramic Flatpack Package – Top View

Fast AC/DC Converter



Feedforward compensation can be used to make a fast full wave rectifier without a filter.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings ⁽¹⁾

Supply Voltage	±22V
Differential Input Voltage	±30V
Input Voltage ⁽²⁾	±15V
Output Short Circuit Duration	Continuous
Operating Ambient Temp. Range	-55°C ≤ T _A ≤ +125°C
T _J Max	150°C
Power Dissipation at T _A = 25°C ⁽³⁾	
H-Package	
(Still Air)	750 mW
(500 LF / Min Air Flow)	1,200 mW
J8-Package	
(Still Air)	1,000 mW
(500 LF / Min Air Flow)	1,500 mW
J14-Package	
(Still Air)	1,200mW
(500 LF / Min Air Flow)	2,000mW
W-Package	
(Still Air)	500mW
(500 LF / Min Air Flow)	800mW
Thermal Resistance	
θ _{JA}	
H-Package	
(Still Air)	165°C/W
(500 LF / Min Air Flow)	89°C/W
J8-Package	
(Still Air)	128°C/W
(500 LF / Min Air Flow)	75°C/W
J14-Package	
(Still Air)	98°C/W
(500 LF / Min Air Flow)	59°C/W
W-Package	
(Still Air)	233°C/W
(500 LF / Min Air Flow)	155°C/W
θ _{JC} (Typical)	
H-Package	39°C/W
J8-Package	26°C/W
J14-Package	24°C/W
W-Package	26°C/W
Storage Temperature Range	-65°C ≤ T _A ≤ +150°C
Lead Temperature (Soldering, 10 sec.)	300°C
ESD Tolerance ⁽⁴⁾	3000V

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating ratings indicate conditions for which the device is intended to be functional, but do no guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
- (2) For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
- (3) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax} (maximum junction temperature), θ_{JA} (package junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is P_{Dmax} = (T_{Jmax} - T_A) / θ_{JA} or the number given in the Absolute Maximum Ratings, whichever is lower.
- (4) Human body model, 100 pF discharged through 1.5 kΩ.

Quality Conformance Inspection

Mil-Std-883, Method 5005 - Group A

Subgroup	Description	Temp (°C)
1	Static tests at	25
2	Static tests at	125
3	Static tests at	-55
4	Dynamic tests at	25
5	Dynamic tests at	125
6	Dynamic tests at	-55
7	Functional tests at	25
8A	Functional tests at	125
8B	Functional tests at	-55
9	Switching tests at	25
10	Switching tests at	125
11	Switching tests at	-55

LM101A JAN Electrical Characteristics DC Parameters

The following conditions apply to all parameters, unless otherwise specified

$V_{CC} = \pm 20V$, $V_{CM} = 0V$, $R_S = 50\Omega$

Symbol	Parameters	Conditions	Notes	Min	Max	Unit	Sub-groups
V_{IO}	Input Offset Voltage	$+V_{CC} = 35V$, $-V_{CC} = -5V$, $V_{CM} = -15V$		-2.0	+2.0	mV	1
				-3.0	+3.0	mV	2, 3
		$+V_{CC} = 5V$, $-V_{CC} = -35V$, $V_{CM} = +15V$		-2.0	+2.0	mV	1
				-3.0	+3.0	mV	2, 3
		$V_{CM} = 0V$		-2.0	+2.0	mV	1
				-3.0	+3.0	mV	2, 3
		$+V_{CC} = 5V$, $-V_{CC} = -5V$, $V_{CM} = 0V$		-2.0	+2.0	mV	1
				-3.0	+3.0	mV	2, 3
I_{IO}	Input Offset Current	$+V_{CC} = 35V$, $-V_{CC} = -5V$, $V_{CM} = -15V$, $R_S = 100K\Omega$		-10	+10	nA	1, 2
				-20	+20	nA	3
		$+V_{CC} = 5V$, $-V_{CC} = -35V$, $V_{CM} = +15V$, $R_S = 100K\Omega$		-10	+10	nA	1, 2
				-20	+20	nA	3
		$V_{CM} = 0V$, $R_S = 100K\Omega$		-10	+10	nA	1, 2
				-20	+20	nA	3
		$+V_{CC} = 5V$, $-V_{CC} = -5V$, $V_{CM} = 0V$, $R_S = 100K\Omega$		-10	+10	nA	1, 2
				-20	+20	nA	3
$\pm I_B$	Input Bias Current	$+V_{CC} = 35V$, $-V_{CC} = -5V$, $V_{CM} = -15V$, $R_S = 100K\Omega$		-0.1	75	nA	1, 2
				-0.1	100	nA	3
		$+V_{CC} = 5V$, $-V_{CC} = -35V$, $V_{CM} = +15V$, $R_S = 100K\Omega$		-0.1	75	nA	1, 2
				-0.1	100	nA	3
		$V_{CM} = 0V$, $R_S = 100K\Omega$		-0.1	75	nA	1, 2
				-0.1	100	nA	3
		$+V_{CC} = 5V$, $-V_{CC} = -5V$, $V_{CM} = 0V$, $R_S = 100K\Omega$		-0.1	75	nA	1, 2
				-0.1	100	nA	3
+PSRR	Power Supply Rejection Ratio	$+V_{CC} = 10V$, $-V_{CC} = -20V$		-50	+50	$\mu V/V$	1
				-100	+100	$\mu V/V$	2, 3
-PSRR	Power Supply Rejection Ratio	$+V_{CC} = 20V$, $-V_{CC} = -10V$		-50	+50	$\mu V/V$	1
				-100	+100	$\mu V/V$	2, 3
CMRR	Common Mode Rejection Ratio	$V_{CC} = \pm 35V$ to $\pm 5V$, $V_{CM} = \pm 15V$		80		dB	1, 2, 3
$+V_{IO}$ Adj	Adjustment for Input Offset Voltage			4.0		mV	1, 2, 3
$-V_{IO}$ Adj	Adjustment for Input Offset Voltage				-4.0	mV	1, 2, 3
$+I_{OS}$	Output Short Circuit Current	$+V_{CC} = 15V$, $-V_{CC} = -15V$, $t \leq 25mS$, $V_{CM} = -15V$		-60		mA	1, 2, 3
$-I_{OS}$	Output Short Circuit Current	$+V_{CC} = 15V$, $-V_{CC} = -15V$, $t \leq 25mS$, $V_{CM} = +15V$			+60	mA	1, 2, 3
I_{CC}	Power Supply Current	$+V_{CC} = 15V$, $-V_{CC} = -15V$			3.0	mA	1
					2.32	mA	2
					3.5	mA	3
$\Delta V_{IO} / \Delta T$	Temperature Coefficient of Input Offset Voltage	$-55^\circ C \leq T_A \leq +25^\circ C$	(1)	-18	+18	$\mu V/^\circ C$	2
		$+25^\circ C \leq T_A \leq +125^\circ C$	(1)	-15	+15	$\mu V/^\circ C$	3
$\Delta I_{IO} / \Delta T$	Temperature Coefficient of Input Offset Current	$-55^\circ C \leq T_A \leq +25^\circ C$	(1)	-200	+200	pA/°C	2
		$+25^\circ C \leq T_A \leq +125^\circ C$	(1)	-100	+100	pA/°C	3

(1) Calculated parameter

LM101A JAN Electrical Characteristics DC Parameters (continued)

The following conditions apply to all parameters, unless otherwise specified

 $V_{CC} = \pm 20V$, $V_{CM} = 0V$, $R_S = 50\Omega$

Symbol	Parameters	Conditions	Notes	Min	Max	Unit	Sub-groups
$-A_{VS}$	Large Signal (Open Loop) Voltage Gain	$R_L = 2K\Omega$, $V_O = -15V$	(2)	50		V/mV	4
			(2)	25		V/mV	5, 6
		$R_L = 10K\Omega$, $V_O = -15V$	(2)	50		V/mV	4
			(2)	25		V/mV	5, 6
$+A_{VS}$	Large Signal (Open Loop) Voltage Gain	$R_L = 2K\Omega$, $V_O = +15V$	(2)	50		V/mV	4
			(2)	25		V/mV	5, 6
		$R_L = 10K\Omega$, $V_O = +15V$	(2)	50		V/mV	4
			(2)	25		V/mV	5, 6
A_{VS}	Large Signal (Open Loop) Voltage Gain	$V_{CC} = \pm 5V$, $R_L = 2K\Omega$, $V_O = \pm 2V$	(2)	10		V/mV	4, 5, 6
		$V_{CC} = \pm 5V$, $R_L = 10K\Omega$, $V_O = \pm 2V$	(2)	10		V/mV	4, 5, 6
$+V_{OP}$	Output Voltage Swing	$R_L = 10K\Omega$, $V_{CM} = -20V$		+16		V	4, 5, 6
		$R_L = 2K\Omega$, $V_{CM} = -20V$		+15		V	4, 5, 6
$-V_{OP}$	Output Voltage Swing	$R_L = 10K\Omega$, $V_{CM} = 20V$			-16	V	4, 5, 6
		$R_L = 2K\Omega$, $V_{CM} = 20V$			-15	V	4, 5, 6

(2) Datalog reading of $K = V/mV$.

LM101A JAN Electrical Characteristics AC Parameters

The following conditions apply to all parameters, unless otherwise specified

$V_{CC} = \pm 20V$, $V_{CM} = 0V$, $R_S = 50\Omega$

Symbol	Parameter	Conditions	Notes	Min	Max	Units	Sub-groups
+SR	Slew Rate	$A_V = 1$, $V_I = -5V$ to $+5V$		0.3		V/ μ S	7
-SR	Slew Rate	$A_V = 1$, $V_I = +5V$ to $-5V$		0.3		V/ μ S	7
TR _{TR}	Rise Time	$A_V = 1$, $V_I = 50mV$			800	nS	7
TR _{OS}	Overshoot	$A_V = 1$, $V_I = 50mV$			25	%	7
NI _{BB}	Noise Broadband	BW = 10Hz to 5KHz, $R_S = 0\Omega$			15	μV_{RMS}	7
NI _{PC}	Noise Popcorn	BW = 10Hz to 5KHz, $R_S = 100K\Omega$			80	μV_{PK}	7

LM101A JAN Electrical Characteristics DC Parameters: Drift Values

The following conditions apply to all parameters, unless otherwise specified

$V_{CC} = \pm 20V$, $V_{CM} = 0V$, $R_S = 50\Omega$

Delta calculations performed on JAN S devices at group B, Subgroup 5 only.

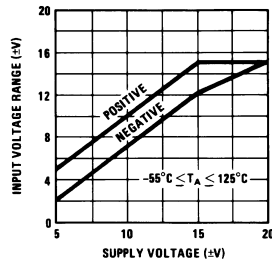
Symbol	Parameter	Conditions	Notes	Min	Max	Units	Sub-groups
V_{IO}	Input Offset Voltage	$V_{CM} = 0V$		-0.5	0.5	mV	1
$\pm I_{IB}$	Input Bias Current	$V_{CM} = 0V$, $R_S = 100K\Omega$		-7.5	7.5	nA	1

Notes

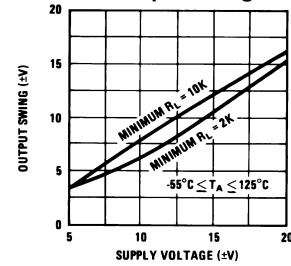
Typical Performance Characteristics

LM101A

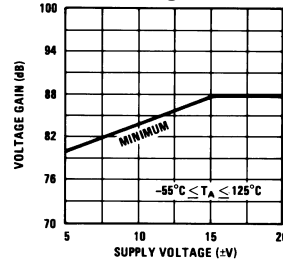
Input Voltage Range



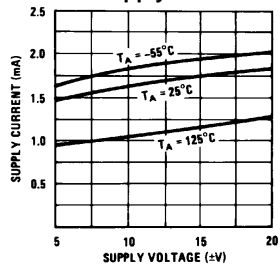
Output Swing



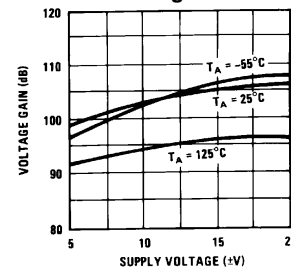
Voltage Gain



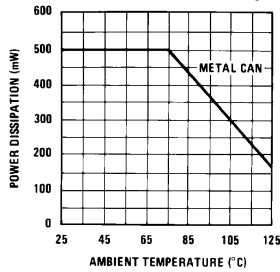
Supply Current



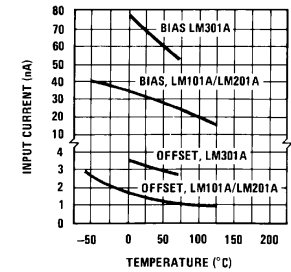
Voltage Gain



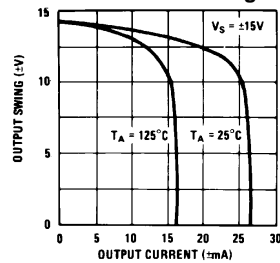
Maximum Power Dissipation



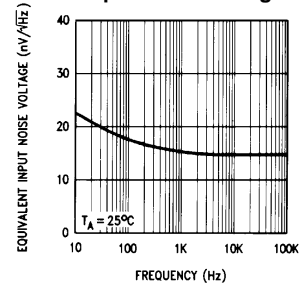
Input Current, LM101A



Current Limiting

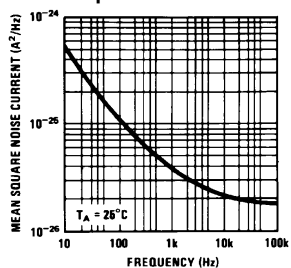


Input Noise Voltage

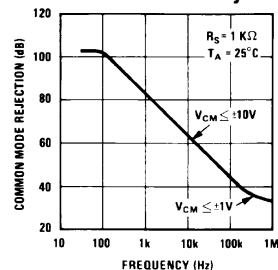


Typical Performance Characteristics LM101A (continued)

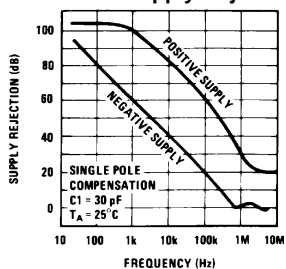
Input Noise Current



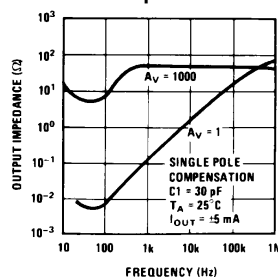
Common Mode Rejection



Power Supply Rejection

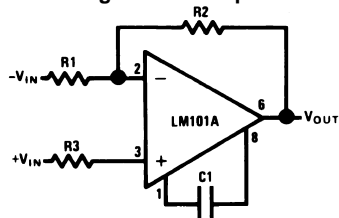


Closed Loop Output Impedance



Typical Performance Characteristics for Various Compensation Circuits

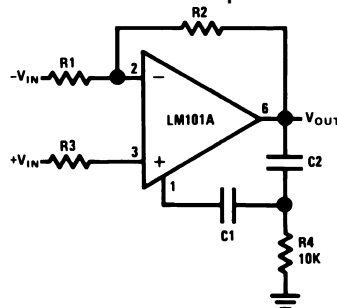
Single Pole Compensation



$$C1 \geq \frac{R1 C_S}{R1 + R2}$$

$$C_S = 30 \text{ pF}$$

Two Pole Compensation

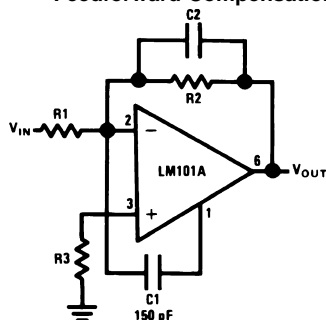


$$C1 \geq \frac{R1 C_S}{R1 + R2}$$

$$C_S = 30 \text{ pF}$$

$$C2 = 10 C1$$

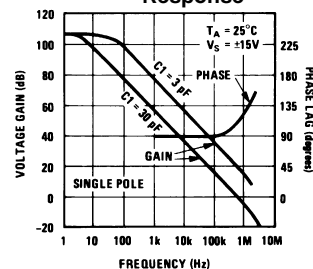
Feedforward Compensation



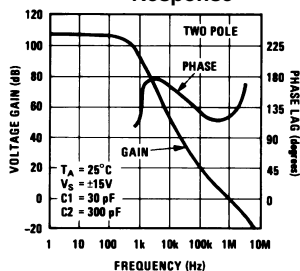
$$C2 = \frac{1}{2\pi f_o R2}$$

$$f_o = 3 \text{ MHz}$$

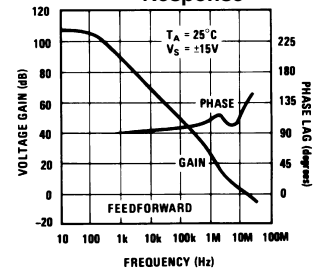
Open Loop Frequency Response



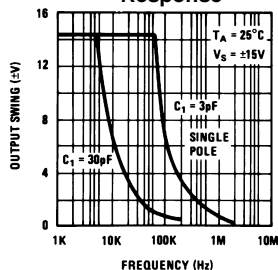
Open Loop Frequency Response



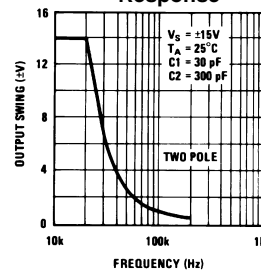
Open Loop Frequency Response



Large Signal Frequency Response



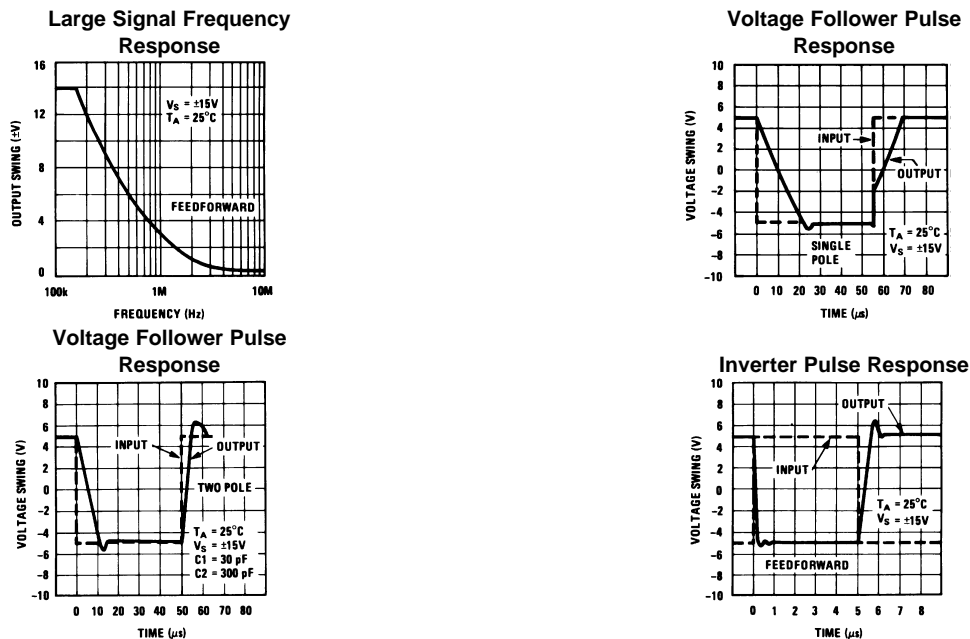
Large Signal Frequency Response



(1) Pin connections shown are for 8-pin packages.

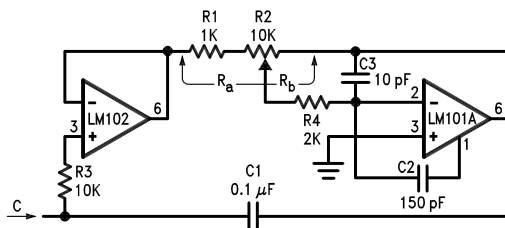
Typical Performance Characteristics for Various Compensation Circuits (continued)

(1)



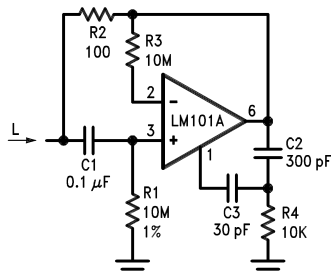
Typical Applications (2)

Figure 5. Variable Capacitance Multiplier



$$C = 1 + \frac{R_b}{R_a} C_1$$

Figure 6. Simulated Inductor



$$L \approx R_1 R_2 C_1$$

$$R_S = R_2$$

$$R_P = R_1$$

(2) Pin connections shown are for 8-pin packages.

Figure 7. Fast Inverting Amplifier with High Input Impedance

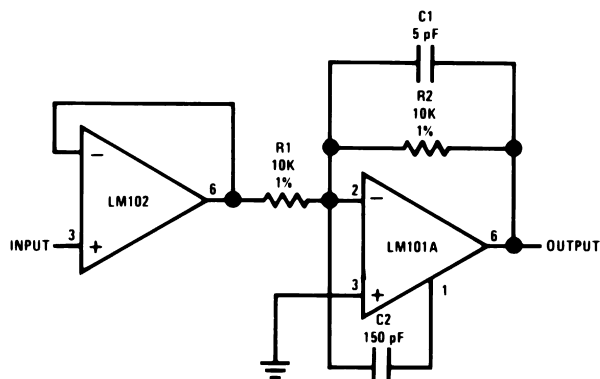
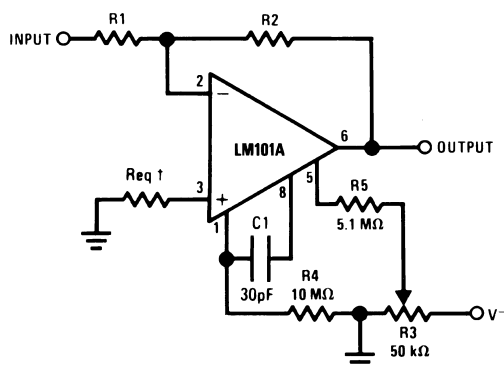
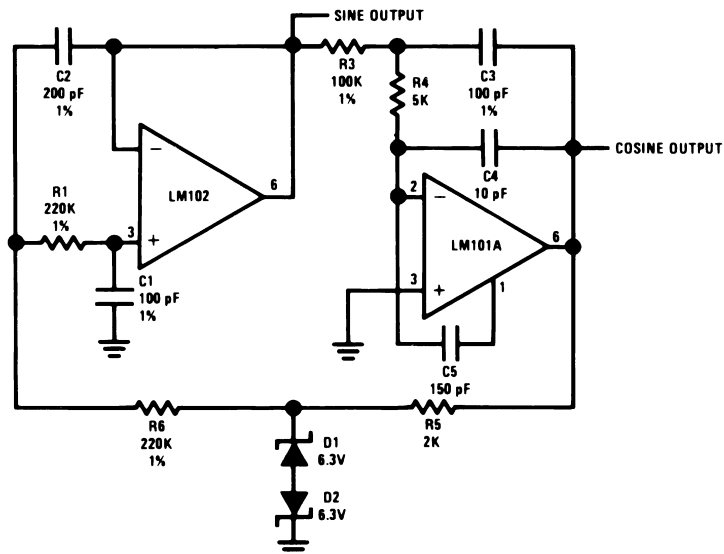


Figure 8. Inverting Amplifier with Balancing Circuit



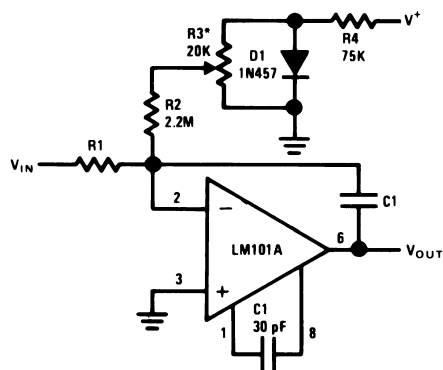
†May be zero or equal to parallel combination of R1 and R2 for minimum offset.

Figure 9. Sine Wave Oscillator



$f_o = 10 \text{ kHz}$

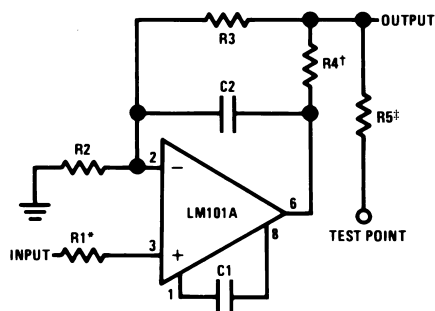
Figure 10. Integrator with Bias Current Compensation



*Adjust for zero integrator drift. Current drift typically 0.1 nA/°C over –55°C to +125°C temperature range.

Application Hints ⁽³⁾

Figure 11. Protecting Against Gross Fault Conditions

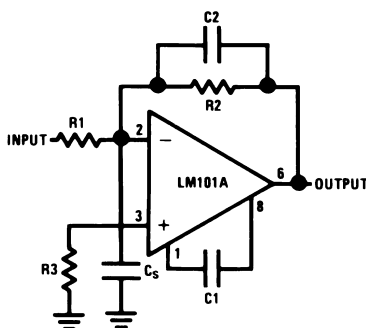


*Protects input

†Protects output

‡Protects output—not needed when R4 is used.

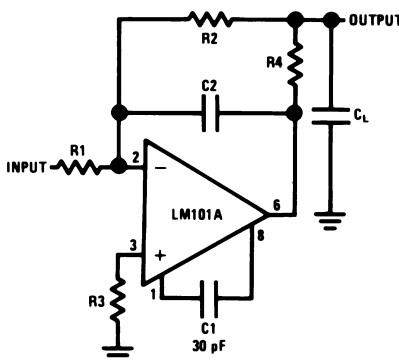
Figure 12. Compensating for Stray Input Capacitances or Large Feedback Resistor



$$C2 = \frac{R1 C_s}{R2}$$

(3) Pin connections shown are for 8-pin packages.

Figure 13. Isolating Large Capacitive Loads



Although the LM101A is designed for trouble free operation, experience has indicated that it is wise to observe certain precautions given below to protect the devices from abnormal operating conditions. It might be pointed out that the advice given here is applicable to practically any IC op amp, although the exact reason why may differ with different devices.

When driving either input from a low-impedance source, a limiting resistor should be placed in series with the input lead to limit the peak instantaneous output current of the source to something less than 100 mA. This is especially important when the inputs go outside a piece of equipment where they could accidentally be connected to high voltage sources. Large capacitors on the input (greater than 0.1 μF) should be treated as a low source impedance and isolated with a resistor. Low impedance sources do not cause a problem unless their output voltage exceeds the supply voltage. However, the supplies go to zero when they are turned off, so the isolation is usually needed.

The output circuitry is protected against damage from shorts to ground. However, when the amplifier output is connected to a test point, it should be isolated by a limiting resistor, as test points frequently get shorted to bad places. Further, when the amplifier drives a load external to the equipment, it is also advisable to use some sort of limiting resistance to preclude mishaps.

Precautions should be taken to insure that the power supplies for the integrated circuit never become reversed—even under transient conditions. With reverse voltages greater than 1V, the IC will conduct excessive current, fusing internal aluminum interconnects. If there is a possibility of this happening, clamp diodes with a high peak current rating should be installed on the supply lines. Reversal of the voltage between V^+ and V^- will always cause a problem, although reversals with respect to ground may also give difficulties in many circuits.

The minimum values given for the frequency compensation capacitor are stable only for source resistances less than 10 k Ω , stray capacitances on the summing junction less than 5 pF and capacitive loads smaller than 100 pF. If any of these conditions are not met, it becomes necessary to overcompensate the amplifier with a larger compensation capacitor. Alternately, lead capacitors can be used in the feedback network to negate the effect of stray capacitance and large feedback resistors or an RC network can be added to isolate capacitive loads.

Although the LM101A is relatively unaffected by supply bypassing, this cannot be ignored altogether. Generally it is necessary to bypass the supplies to ground at least once on every circuit card, and more bypass points may be required if more than five amplifiers are used. When feed-forward compensation is employed, however, it is advisable to bypass the supply leads of each amplifier with low inductance capacitors because of the higher frequencies involved.

Typical Applications ⁽⁴⁾

Figure 14. Standard Compensation and Offset Balancing Circuit

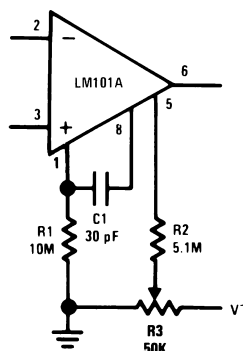
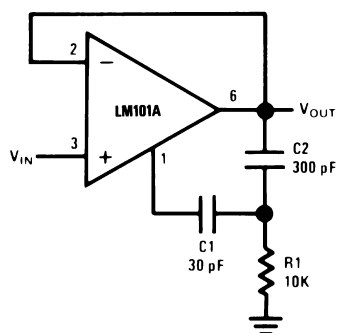
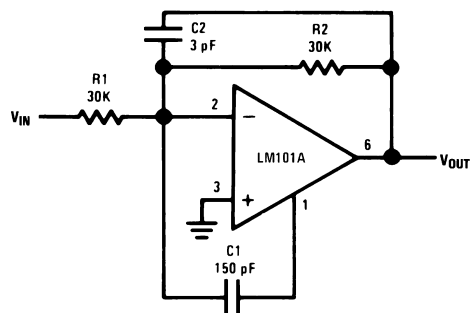


Figure 15. Fast Voltage Follower



Power Bandwidth: 15 kHz
Slew Rate: 1V/μs

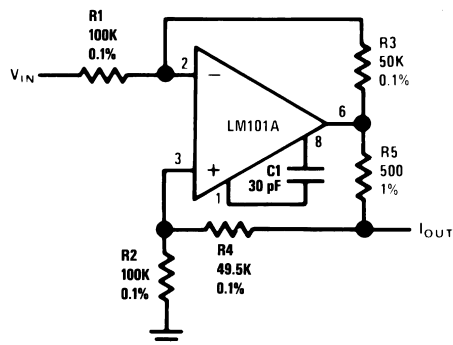
Figure 16. Fast Summing Amplifier



Power Bandwidth: 250 kHz
Small Signal Bandwidth: 3.5 MHz
Slew Rate: 10V/μs

(4) Pin connections shown are for 8-pin packages.

Figure 17. Bilateral Current Source

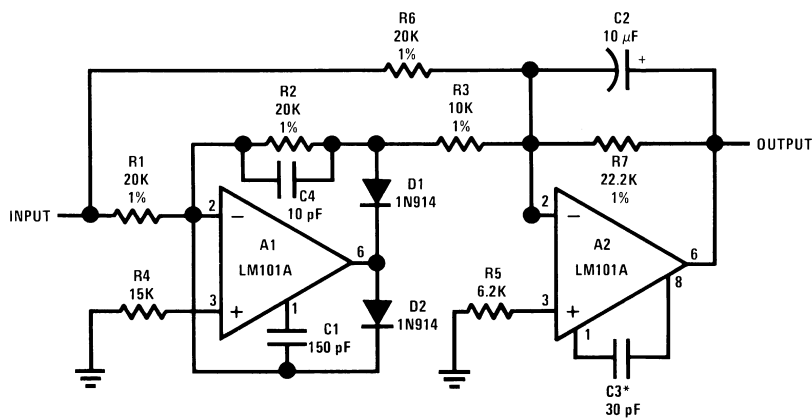


$$I_{OUT} = \frac{R_3 V_{IN}}{R_1 R_5}$$

$$R_3 = R_4 + R_5$$

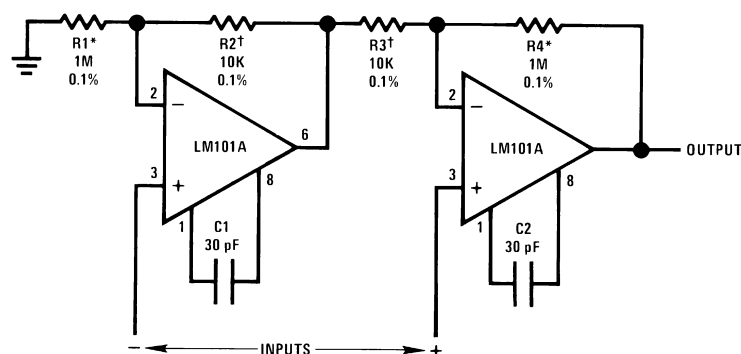
$$R_1 = R_2$$

Figure 18. Fast AC/DC Converter



Feedforward compensation can be used to make a fast full wave rectifier without a filter.

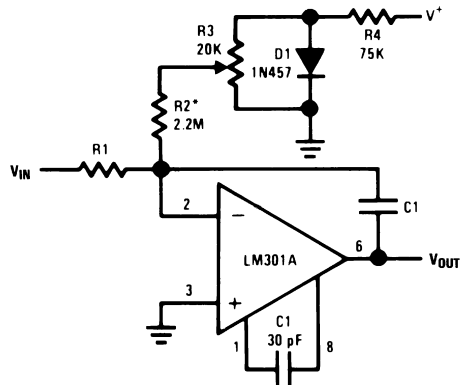
Figure 19. Instrumentation Amplifier



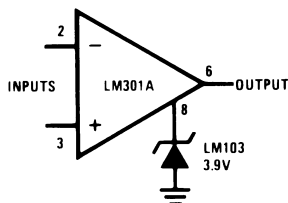
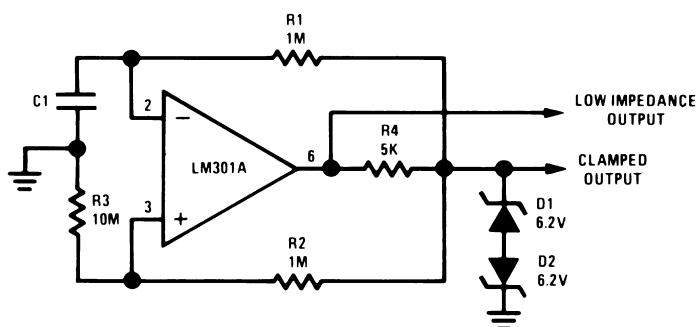
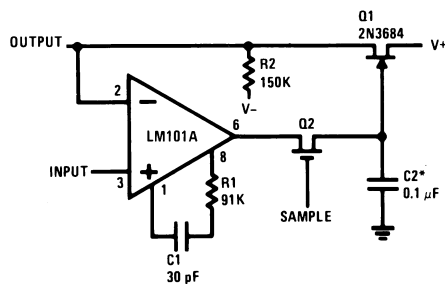
$$R_1 = R_4; R_2 = R_3$$

$$A_v = 1 + \frac{R_1}{R_2}$$

*, † Matching determines CMRR.

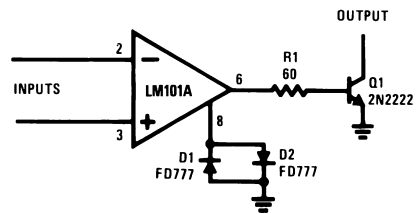
Figure 20. Integrator with Bias Current Compensation

*Adjust for zero integrator drift. Current drift typically 0.1 nA/°C over 0°C to +70°C temperature range.

Figure 21. Voltage Comparator for Driving RTL Logic or High Current Driver**Figure 22. Low Frequency Square Wave Generator****Figure 23. Low Drift Sample and Hold**

*Polycarbonate-dielectric capacitor

Figure 24. Voltage Comparator for Driving DTL or TTL Integrated Circuits



REVISION HISTORY SECTION

Date Released	Revision	Section	Originator	Changes
01/05/06	A	New Release to corporate format	L. Lytle	1 MDS datasheets converted into one Corp. datasheet format. MJLM101A-X Rev 1A0 datasheet will be archived.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
JL101ABCA	ACTIVE	CDIP	J	14	25	TBD	A42 SNPB	Level-1-NA-UNLIM	-55 to 125	JL101ABCA JM38510/10103BCA Q	Samples
JL101ABGA	ACTIVE	TO-99	LMC	8	20	TBD	POST-PLATE	Level-1-NA-UNLIM	-55 to 125	JL101ABGA JM38510/10103BGA Q ACO JM38510/10103BGA Q >T	Samples
JL101ABPA	ACTIVE	CDIP	NAB	8	40	TBD	A42 SNPB	Level-1-NA-UNLIM	-55 to 125	JL101ABPA Q JM38510/ 10103BPA ACO 10103BPA >T	Samples
JM38510/10103BCA	ACTIVE	CDIP	J	14	25	TBD	A42 SNPB	Level-1-NA-UNLIM	-55 to 125	JL101ABCA JM38510/10103BCA Q	Samples
JM38510/10103BGA	ACTIVE	TO-99	LMC	8	20	TBD	POST-PLATE	Level-1-NA-UNLIM	-55 to 125	JL101ABGA JM38510/10103BGA Q ACO JM38510/10103BGA Q >T	Samples
JM38510/10103BPA	ACTIVE	CDIP	NAB	8	40	TBD	A42 SNPB	Level-1-NA-UNLIM	-55 to 125	JL101ABPA Q JM38510/ 10103BPA ACO 10103BPA >T	Samples
M38510/10103BCA	ACTIVE	CDIP	J	14	25	TBD	A42 SNPB	Level-1-NA-UNLIM	-55 to 125	JL101ABCA JM38510/10103BCA Q	Samples
M38510/10103BGA	ACTIVE	TO-99	LMC	8	20	TBD	POST-PLATE	Level-1-NA-UNLIM	-55 to 125	JL101ABGA JM38510/10103BGA Q ACO JM38510/10103BGA Q >T	Samples
M38510/10103BPA	ACTIVE	CDIP	NAB	8	40	TBD	A42 SNPB	Level-1-NA-UNLIM	-55 to 125	JL101ABPA Q JM38510/ 10103BPA ACO 10103BPA >T	Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

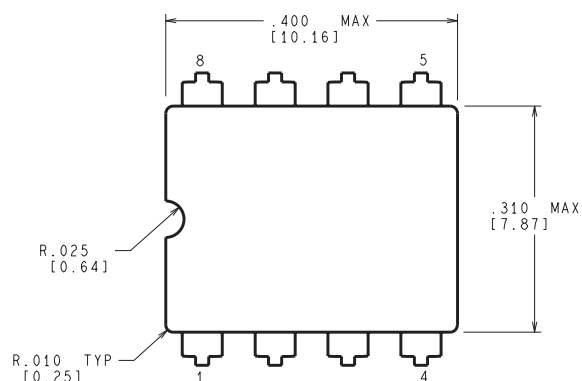
⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ Only one of markings shown within the brackets will appear on the physical device.

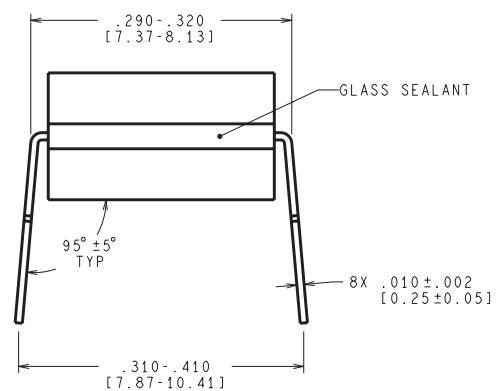
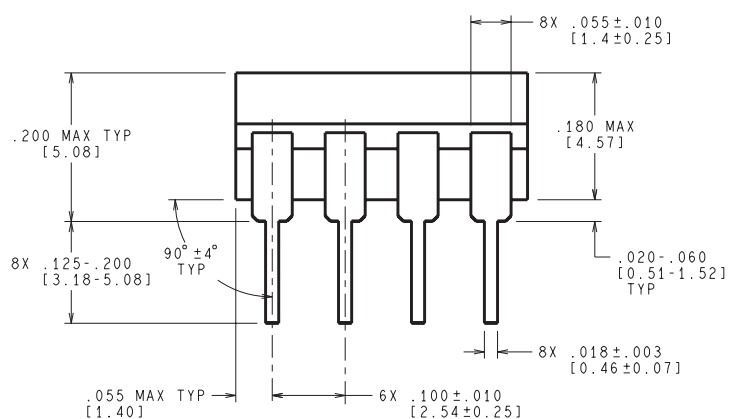
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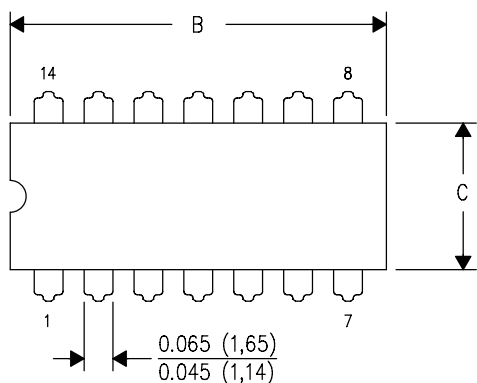


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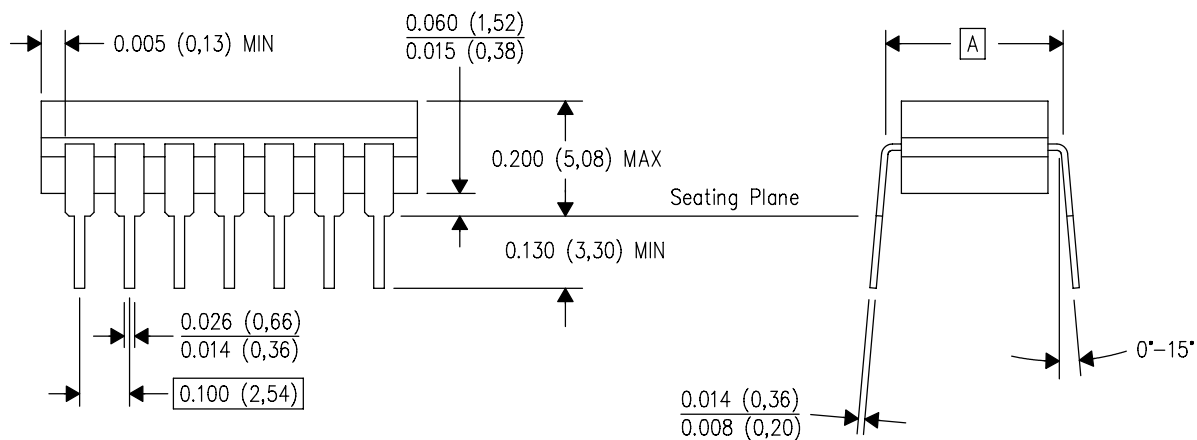
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

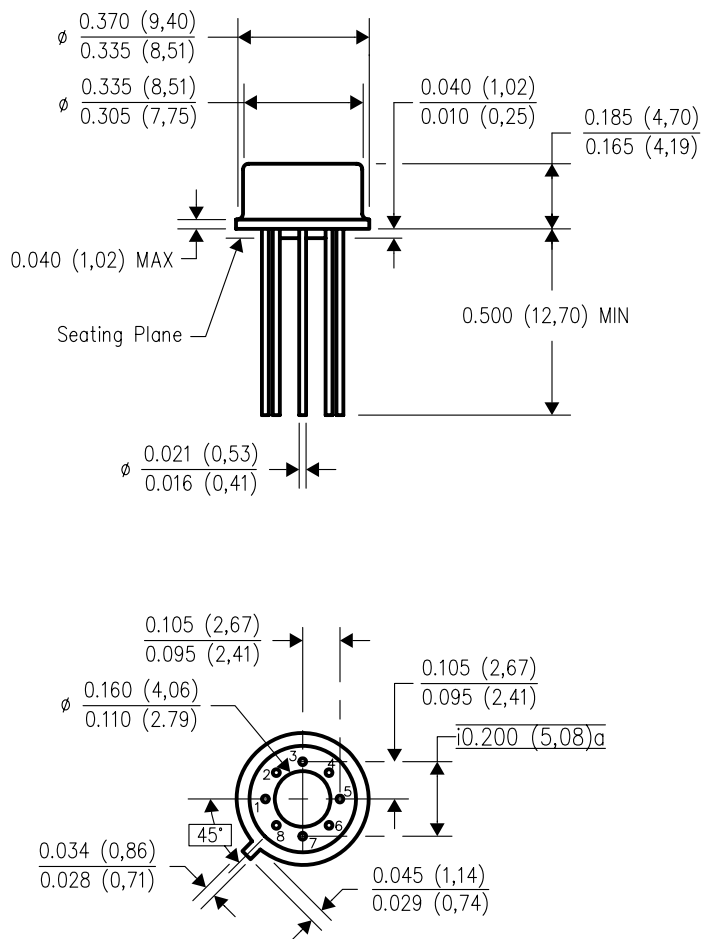


4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

LMC (O-MBCY-W8)

METAL CYLINDRICAL PACKAGE



4202483/B 09/07

NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Leads in true position within 0.010 (0,25) R @ MMC at seating plane.
- D. Pin numbers shown for reference only. Numbers may not be marked on package.
- E. Falls within JEDEC MO-002/TO-99.

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