National Semiconductor

LH4010/LH4010C Fast FET Buffer

General Description

The LH4010/LH4010C is a high speed, FET input, voltage follower/buffer designed to provide high current drive at frequencies from DC to over 100 MHz. LH4010 will provide ±100 mA into 50Ω loads (±250 mA peak) at slew rates of 2500 V/μs. In addition, both exhibit excellent phase linearity up to 20 MHz.

The LH4010 is intended to fulfill a wide range of buffer applications such as high speed line drivers, video impedance transformation, nuclear instrumentation amplifiers, op amp isolation buffer for driving reactive loads and high impedance input buffers for high speed ADCs and comparators.

These devices are constructed using specially selected junction FETs and active laser trimming to achieve guaranteed performance specifications. The LH4010 is specified for operation from −55°C to +125°C; whereas, the LH4010C is specified from −25°C to +85°C. The LH4010/LH4010C is available in a 1.5W metal TO-8 package or a 16 lead dual-in-line package, N16A.

Features

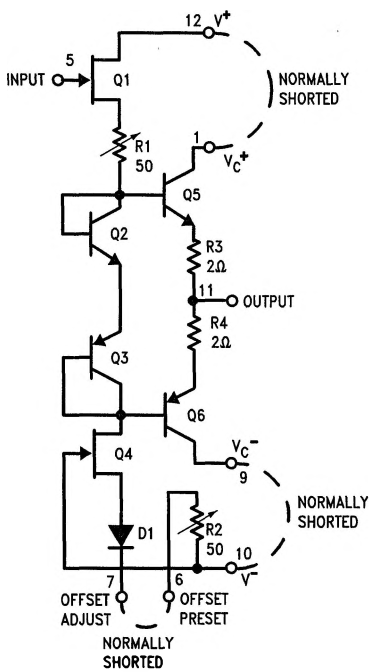
- Slew rate 2500 V/μs
- Wide range single or dual supply operation
- Power bandwidth DC to 20 MHz
- High output drive ±10V with 100Ω load
- Low phase non-linearity 2°
- Fast rise times 2 ns
- High current gain 120 dB
- High input resistance 10^{10}Ω
- Pin compatible with LH0033

Applications

- High speed cable driver
- Isolation buffer
- ADC input buffer
- Op amp current booster

Schematic and Connection Diagram

LH4010/LH4010C



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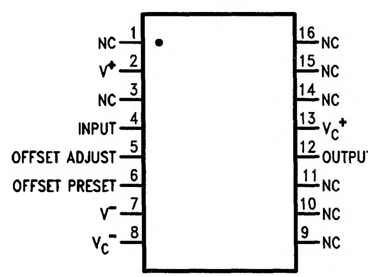
Pin numbers shown for TO-8 ("G") package.

Top View



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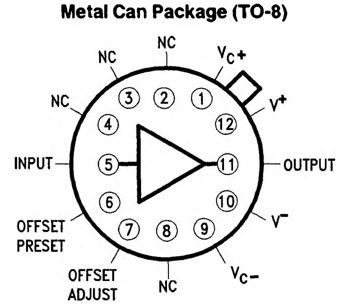
Order Number LH4010CN
See NS Package Number N16A

Metal Can Package (TO-8)



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Top View

Case is Electrically Isolated.

Order Number LH4010G or LH4010CG
See NS Package Number H12B

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ($V^+ - V^-$)	40V
Maximim Power Dissipation (See Curves)	1.5W
Maximum Junction Temperature	175°C
Input Voltage	Equal to Supplies
Output Current, Continuous	±100 mA
Pulsed	±250 mA
Operating Temperature Range	
LH4010C	−25°C to +85°C
LH4010	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics

$V_S = \pm 15V$, $V_{IN} = 0V$, $R_L = 1k$, $T_A = 25°C$ unless otherwise noted (Note 1)

Symbol	Parameter	Conditions	LH4010C			Units (Max Unless Otherwise Noted)
			Typical	Tested Limit (Note 2)	Design Limit (Note 3)	
V_{OS}	Output Offset Voltage	$V_{IN} = 0V$, $T_A = T_J = 25°C$ (Note 4)	5	10	**20**	mV
I_B	Input Bias Current	$T_J = 25°C$ (Note 1)	0.5	1	**50**	nA
V_O	Output Voltage Swing	$V_{IN} = \pm 14V$ (Note 1)		±12	**±12**	V (Min)
		$V_{IN} = \pm 10.5$, $R_L = 100\Omega$		±9		V (Min)
R_{IN}	Input Impedance	$T_J = 25°C$, $V_{IN} = \pm 1V$	10^{10}			Ω
I_S	Supply Current		22	26		mA
R_{OUT}	Output Impedance	$V_{IN} = \pm V_{DC}$, $\Delta R_L = 100\Omega$ to ∞		10		Ω
A_V	Voltage Gain	$V_{IN} = \pm 10V$		0.96	**0.96**	V/V (Min)
		$V_{IN} = \pm 10V$, $R_L = 100\Omega$		0.90	**0.90**	V/V (Min)

DC Electrical Characteristics $V_S = \pm 15V$, $V_{IN} = 0V$, $R_L = 1k$, $T_A = 25°C$ otherwise noted (Note 1)

Symbol	Parameter	Conditions	LH4010			Units (Max Unless Otherwise Noted)
			Typical	Tested Limit (Note 2)	Design Limit (Note 3)	
V_{OS}	Input Offset	$V_{IN} = 0V$, $T_A = T_J = 25°C$ (Notes 1, 4)	5	10		mV
				25		
I_B	Input Bias Current	$T_J = 25°C$ (Notes 1, 4)	200	500		pA
				10		nA
V_O	Output Voltage Swing	$V_{IN} = \pm 14V$		**±12**		V (Min)
		$V_{IN} = \pm 10.5$, $RL = 100\Omega$, $T_A = 25°C$		±9		V (Min)
R_{IN}	Input Impedance	$T_J = 25°C$, $V_{IN} = \pm 1V$	10^{10}			Ω
I_S	Supply Current		22	**26**		mA
R_{OUT}	Output Impedance	$V_{IN} = \pm V_{DC}$ (Note 4) $\Delta R_L = 100\Omega$ to ∞		**8**		Ω
A_V	Voltage Gain	$V_{IN} = \pm 10V$		**0.97**		V/V (Min)
		$V_{IN} = \pm 10V$, $RL = 100\Omega$		**0.92**		V/V (Min)

AC Electrical Characteristics $V_S = \pm 15V$, $R_L = 1\ k\Omega$, $R_S = 50\Omega$, $T_A = 25°C$ unless otherwise noted

Symbol	Parameter	Conditions	LH4010/LH4010C			Units (Max Unless Otherwise Noted)
			Typical	Tested Limit (Note 2)	Design Limit (Note 3)	
t_r	Small Signal Rise Time (Note 5)	$\Delta V_{IN} = 0.5V$	1.5			ns
		$R_L = 50\Omega$, $V_{IN} = 0.5V$		2.5		
t_p	Propagation Delay (Note 5)	$\Delta V_{IN} = 0.5V$	2.0			ns
BW	Small Signal Bandwidth (Note 7)		200			MHz (Min)
		$R_L = 50\Omega$			140	
SR	Slew Rate (Note 6)	$V_{IN} = \pm 5V$	2500	2000		V/μs (Min)

Note 1: Boldface limits are guaranteed over full temperature range. Operating ambient temperature range of LH4010C is −25°C to +85°C, and LH4010 is −55°C to +125°C.

Note 2: Tested limits are guaranteed and 100% production tested.

Note 3: Design limits are guaranteed (but not production tested) over the indicated temperature or temperature range. These limits are not used to calculate outgoing quality level.

Note 4: Specifications are at 25°C junction temperature due to requirements of high speed automatic testing. Actual values at operating temperature will exceed value at $T_J = 25°C$.

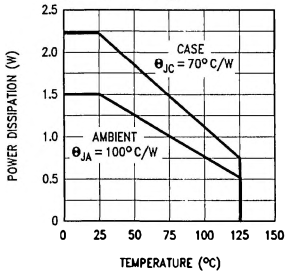
Note 5: See AC Test Circuit.

Note 6: Slew rate is measured between +2.5V and −2.5V. See AC Test Circuit.

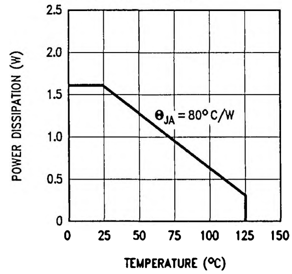
Note 7: Bandwidth is calculated from rise time with $f = t_r/\pi$.

Typical Characteristics

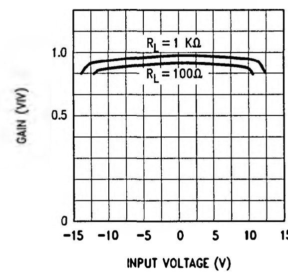
Maximum Power Dissipation for TO-8 ("G") Package



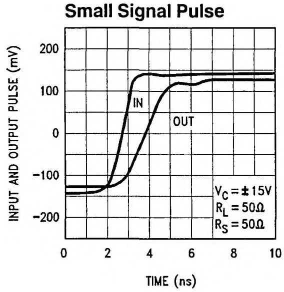
Maximum Power Dissipation for N16A Package



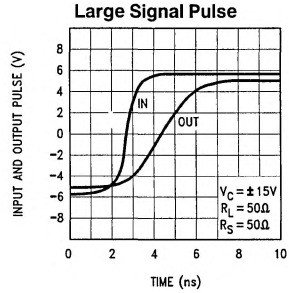
Gain vs Input Voltage



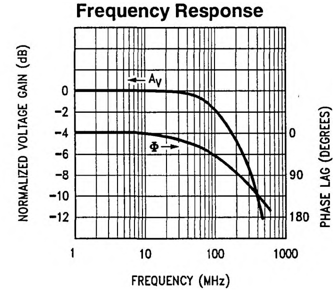
Small Signal Pulse



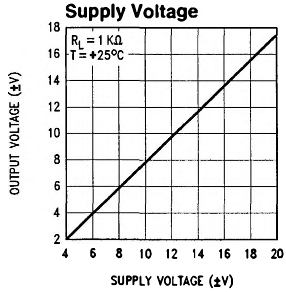
Large Signal Pulse



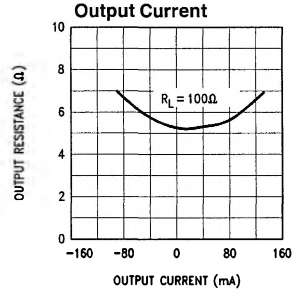
Frequency Response



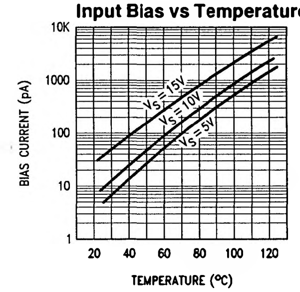
Output Voltage vs Supply Voltage



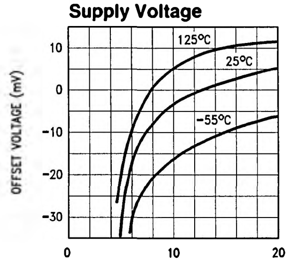
Output Resistance vs Output Current



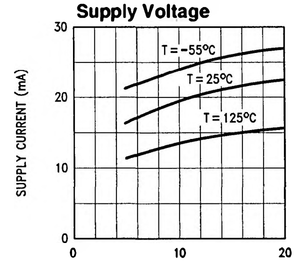
Input Bias vs Temperature



Offset Voltage vs Supply Voltage



Supply Current vs Supply Voltage



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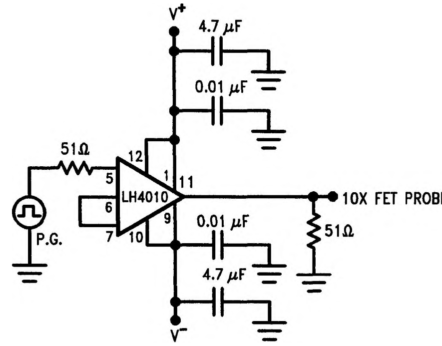
AC Test Circuit



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Application Hints

Recommended Layout Precautions: RF/video printed circuit board layout rules should be followed when using the LH4010 and LH4010C since they will provide power gain to frequencies over 100 MHz. Ground planes are recommended and power supplies should be decoupled at each device with low inductance capacitors. In addition, ground plane shielding may be extended to the metal case of the device since it is electrically isolated from internal circuitry. Alternatively the case should be connected to the output to minimize input capacitance.

Offset Voltage Adjustment: Both the LH4010 and LH4010C offset voltages have been actively trimmed by laser to meet guaranteed specifications when the offset preset pin is shorted to the offset adjust pin. This pre-calibration allows the devices to be used in most DC or AC applications without individually offset nulling each device. If offset null is desirable, it is simply obtained by leaving the offset preset pin open and connecting a trim pot of 100Ω between the offset adjust pin and V^- as illustrated in *Figure 1.*

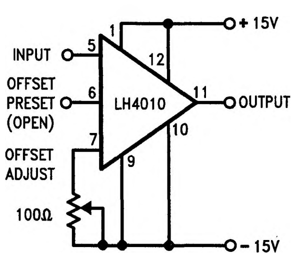

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FIGURE 1. Offset Zero Adjust for LH4010

Operation from Single or Asymmetrical Power Supplies: Both device types may be readily used in application where symmetrical supplies are unavailable or not desirable. A typical application might be an interface to a MOS shift register where $V^+ = +5V$ and $V^- = -12V$. In this case, an apparent output offset occurs due to the device's voltage gain of less than unity. This additional output offset error may be predicted by:

$$\Delta V_O \cong (1 - A_V) \frac{(V^+ - V^-)}{2} = 0.005\,(V^+ - V^-)$$

where:

A_V = No load voltage gain, typically 0.99

V^+ = Positive supply voltage

V^- = Negative supply voltage

For the above example, ΔV_O would be −35 mV. This may be adjusted to zero as discussed above. For AC coupled applications, no additional offset occurs if the DC input is properly biased as illustrated in the "typical applications" section.

Short Circuit Protection: In order to optimize transient response and output swing, output current limit has been omitted from the LH4010 and LH4010C. Short circuit protection may be added by inserting appropriate value resistors between V^+ and V_C^+ pins and V^- and V_C^- pins as illustrated in *Figure 2*. Resistor values may be predicted by:

$$R_{LIM} \cong \frac{V^+}{I_{SC}} = \frac{-V^-}{I_{SC}}$$

where:

$$I_{SC} \leq 100\ \text{mA}$$

The inclusion of limiting resistors in the collectors of the output transitors reduces output voltage swing. Decoupling V_C^+ and V_C^- pins with capacitors to ground will retain full output swing for transient pulses. An alternate active current limit technique that retains full DC output swing is shown in *Figure 3.*

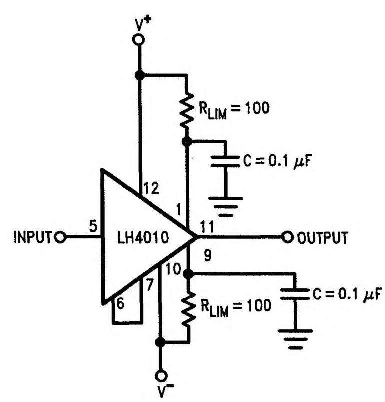

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FIGURE 2

Applications Hints (Continued)

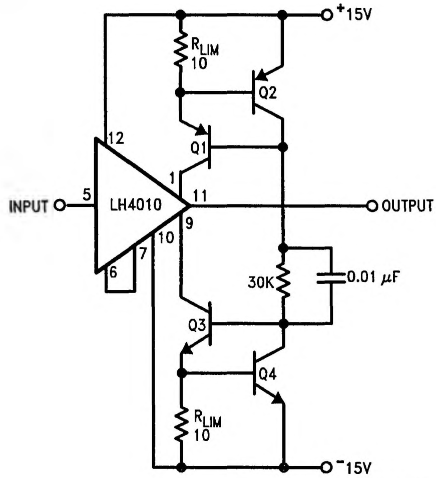

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FIGURE 3. LH4010 Current Limiting Using Current Sources

Capacitive Loading: The LH4010 is designed to drive capacitive loads such as coaxial cables in excess of several thousand picofarads without being susceptible to oscillation. However, peak current resulting from ($C \times dV/dt$) should be limited below absolute maximum peak current ratings for the devices.

Thus:

$$\left\{\frac{\Delta V_{IN}}{\Delta t}\right\} \times C_L \leq I_{OUT} \leq \pm 250 \text{ mA}$$

In addition, power dissipation resulting from driving capcitative loads plus standby power should be kept below total package power rating:

$$P_{\underset{pkg}{diss}} \geq P_{DC} + P_{AC}$$

$$P_{\underset{pkg}{diss}} \geq (V^+ - V^-) \times I_S + P_{AC}$$

$$P_{AC} \cong (V_{PP})^2 \times f \times C_L$$

where: V_{PP} = Peak-to-peak output voltage swing
f = frequency
C_L = Load Capacitance

Operation Within an Op Amp Loop: Both devices may be used as a current booster or isolation buffer within a closed loop with op amps such as LH0032, LM6361, or LM118. An isolation resistor of 47Ω should be used between the op amp output and the input of LH4010. The wide bandwidths and high slew rates of the LH4010 assure that loop has the characteristics of the op amp and that additional rolloff is not required.

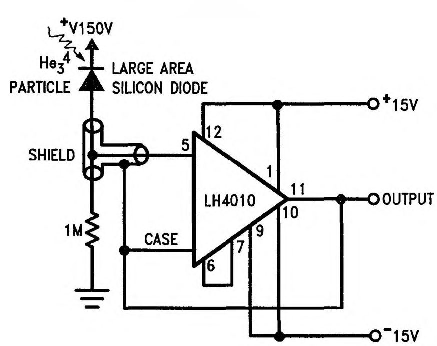
Hardware: In order to utilize the full drive capabilities of the device, it should be mounted with a heat sink particularly for extended temperature operation. The case is isolated from the circuit and may be connected to system chassis.

ATTENTION!

Power supply bypassing is necessary to prevent oscillation in all circuits. Low inductance ceramic disc capacitors with the shortest practical lead lengths must be connected from each supply lead (within < ¼″ to ½″ of the device package) to a ground plane. Capacitors should be one or two 0.1 μF in parallel; adding a 4.7 μF solid tantalum capacitor will help in troublesome instances.

Typical Applications

Nuclear Particle Detector



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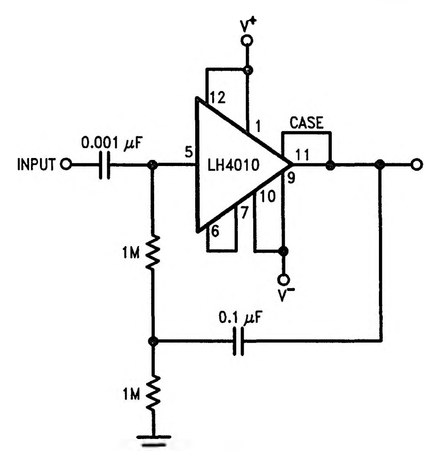
High Input Impedance AC Coupled Amplifier



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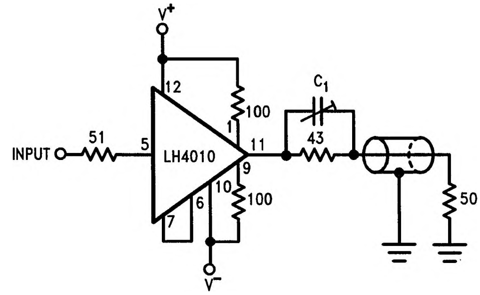
Typical Applications (Continued)

Coaxial Cable Driver



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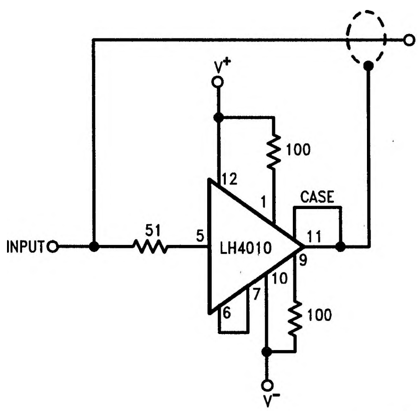
*Select C_1 for optimum pulse response.

Instrumentation Shield/Line Driver



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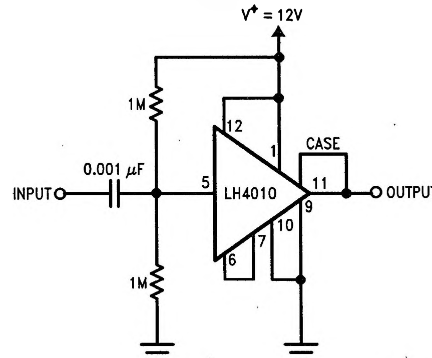
Single Supply AC Amplifier



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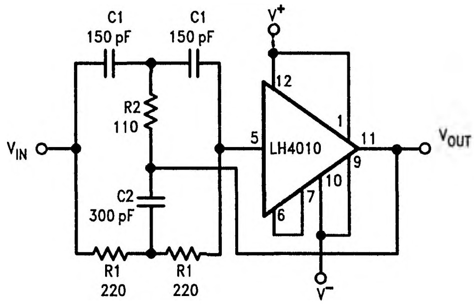
Typical Applications (Continued)

4.5 MHz Notch Filter



$$f_O = \frac{1}{2\pi R1C1}$$

$$R1 = 2\,R2$$

$$C1 = \frac{C2}{2}$$

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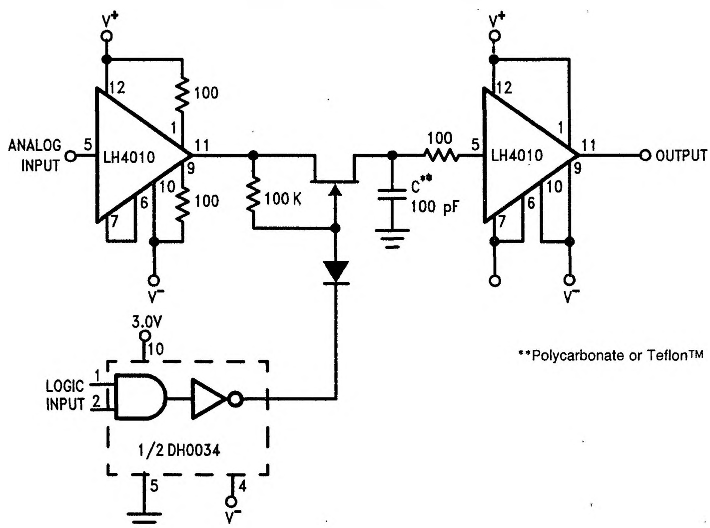
High Speed Sample and Hold



**Polycarbonate or Teflon™

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*Pin numbers shown for TO-8 ("G") package.