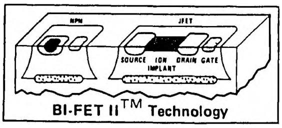
National Semiconductor



BI-FET II™ Technology

LF453 Wide-Bandwidth Dual JFET-Input Operational Amplifiers

General Description

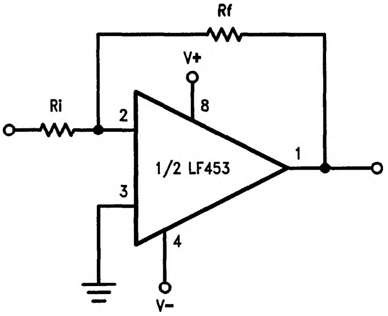
The LF453 is a low-cost, high-speed, dual JFET-input operational amplifier with an internally trimmed input offset voltage (BI-FET II technology). The device requires a low supply current and yet the amplifiers maintain a large gain bandwidth product and a fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF453 is pin compatible with the standard LM1558, allowing designers to upgrade the overall performance of existing designs.

The LF453 may be used in such applications as high-speed integrators, fast D/A converters, sample-and-hold circuits and many other circuits requiring low input bias current, high input impedance, high slew rate and wide bandwidth.

Features

■ Internally trimmed offset voltage	5.0 mV (max)
■ Low input bias current	50 pA (typ)
■ Low input noise current	0.01 pA/$\sqrt{\text{Hz}}$ (typ)
■ Wide gain bandwidth	4 MHz (typ)
■ High slew rate	13 V/μs (typ)
■ Low supply current	6.5 mA (max)
■ High input impedance	$10^{12}\Omega$ (typ)
■ Low total harmonic distortion $A_V = 10$, $R_L = 10k$, $V_O = 20\ V_{p-p}$, f = 20 Hz–20 kHz	<0.02% (typ)
■ Low 1/f noise corner	50 Hz (typ)
■ Fast settling time to 0.01%	2 μs (typ)

Typical Connection



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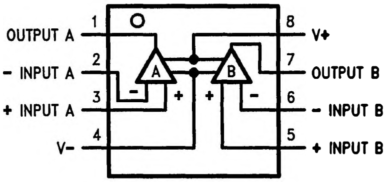
Connection Diagram

SO Package



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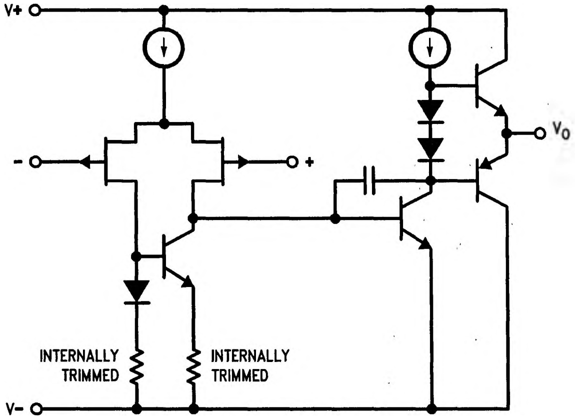
Top View

Order Number LF453CM
See NS Package Number M08A

Simplified Schematic



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ($V^+ - V^-$)	36V
Input Voltage Range	$V^- \le V_{IN} \le V^+$
Differential Input Voltage (Note 2)	±30V
Junction Temperature (T_J MAX)	150°C
Output Short Circuit Duration	Continuous
Power Dissipation (Note 3)	500 mW
ESD Susceptability (Note 4)	2000V

Soldering Information (Note 5)

SO Package: Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

Operating Ratings (Note 1)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
LF453CM	$0°C \le T_A + 70°C$
Junction Temperature ($T_{J\ max}$)	125°C
Supply Voltage ($V^+ - V^-$)	10V to 32V

DC Electrical Characteristics

The following specifications apply for $V^+ = +15V$ and $V^- = -15V$. **Boldface limits apply for T_{MIN} to T_{MAX};** all other limits $T_A = T_J = 25°C$.

Symbol	Parameter	Conditions	LF453CM			Units
			Typical (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	
V_{OS}	Maximum Input Offset Voltage	$R_S = 10\ k\Omega$, (Note 10)		5		mV
I_{OS}	Maximum Input Offset Current	(Notes 9, 10) $T_J = 25°C$ $T_J = 70°C$	25	100	 **2**	pA nA
I_B	Maximum Input Bias Current	(Notes 9, 10) $T_J = 25°C$ $T_J = 70°C$	50	200	 **4**	pA nA
R_{IN}	Input Resistance	$T_J = 25°C$	10^{12}			Ω
AVOL	Minimum Large Signal Voltage Gain	$V_O = \pm 10V$, $R_L = 2\ k\Omega$ (Note 10)	200	50	**25**	V/mV
V_O	Minimum Output Voltage Swing	$R_L = 10k$	±13.5	±12	**±12**	V
V_{CM}	Minimum Input Common Mode Voltage Range		+14.5 −11.5	+11 −11	**+11** **−11**	V V
CMRR	Minimum Common-Mode Rejection Ratio	$R_S \le 10\ k\Omega$	100	80	**80**	dB
PSRR	Minimum Supply Voltage Rejection Ratio	(Note 11)	100	80	**80**	dB
I_S	Maximum Supply Current			6.5	**6.5**	mA

AC Electrical Characteristics

The following specifications apply for $V^+ = +15V$ and $V^- = -15V$. Limits apply for $T_A = T_J = 25°C$.

Symbol	Parameter	Conditions	LF453CM			Units
			Typical (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	
SR	Slew Rate	$A_V = +1$	13	8		V/μs
GBW	Minimum Gain-Bandwidth Product	f = 100 kHz	4	2.7		MHz
e_n	Equivalent Input Noise Voltage	$R_S = 100\Omega$, f = 1 kHz	25			$nV/\sqrt{Hz}$
i_n	Equivalent Input Noise Current	$R_S = 100\Omega$, f = 1 kHz	0.01			$pA/\sqrt{Hz}$

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating ratings.

Note 2: When the input voltage exceeds the power supplies, the current should be limited to 1 mA.

Note 3: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_J MAX, Θ_{JA} and the ambient temperature, T_A. The maximum allowable power dissipation at any temperature is $P_D = (T_J\ MAX - T_A)/\Theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For guaranteed operation $T_{J\ max} = 125°C$. The typical thermal resistance (Θ_{JA}) of the LF453CM when board-mounted is 160°C/W.

Note 4: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 5: See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" (section titled "Surface Mount") for other methods of soldering surface mount devices.

Note 6: Typicals are at $T_J = 25°C$ and represent most likely parametric norm.

Note 7: Tested limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

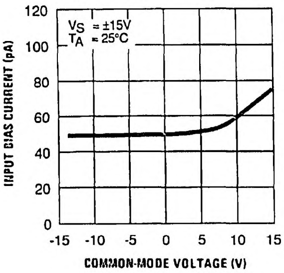
Note 8: Design limits are guaranteed to National's AOQL, but not 100% tested.

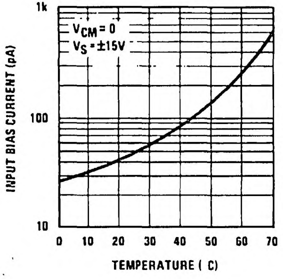
Note 9: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature T_J. Due to limited production test time, the input bias currents are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. $T_J = T_A + \Theta_{JA} P_D$ where Θ_{JA} is the thermal resistance from junction to ambient.

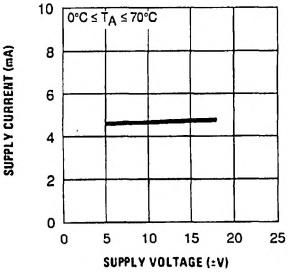
Note 10: V_{OS}, I_B, AVOL and I_{OS} are measured at $V_{CM} = 0V$.

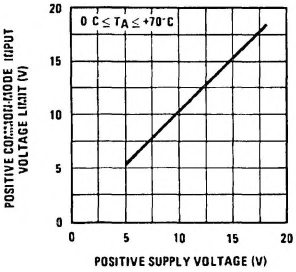
Note 11: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice.

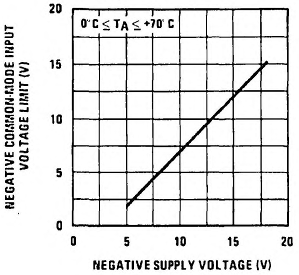
Typical Performance Characteristics

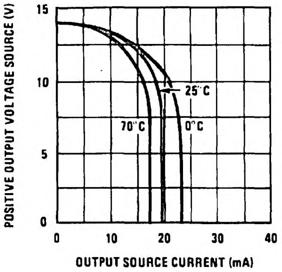

Input Bias Current

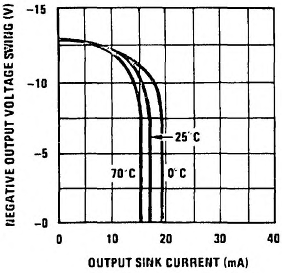

Input Bias Current

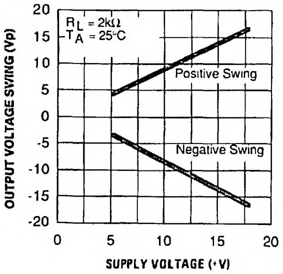

Supply Current

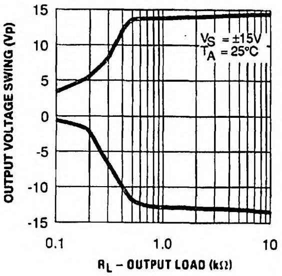

Positive Common-Mode Input Voltage Limit

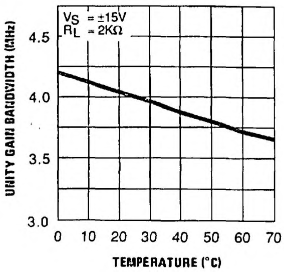

Negative Common-Mode Input Voltage Limit

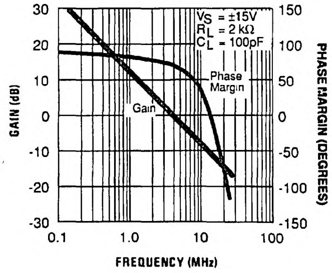

Positive Current Limit

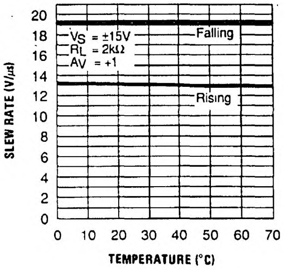

Negative Current Limit


Voltage Swing


Output Voltage Swing


Gain Bandwidth


Bode Plot


Slew Rate

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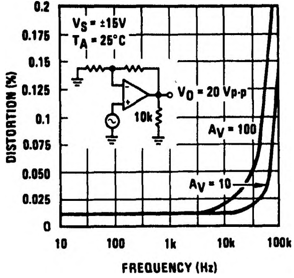
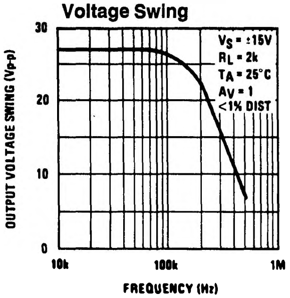
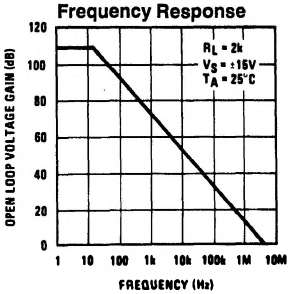
Typical Performance Characteristics (Continued)



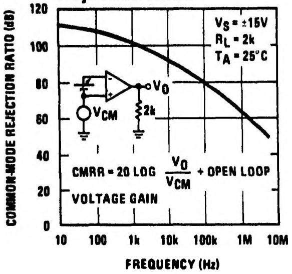
Distortion vs Frequency



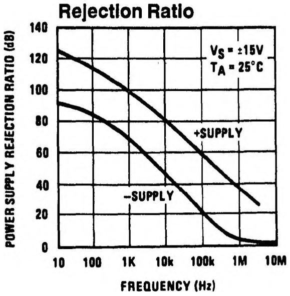
Undistorted Output Voltage Swing



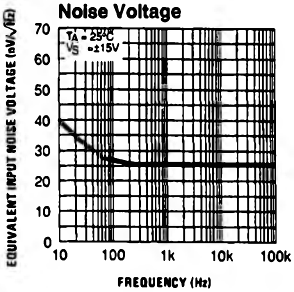
Open Loop Frequency Response



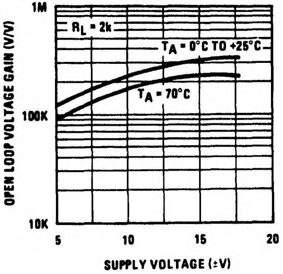
Common-Mode Rejection Ratio



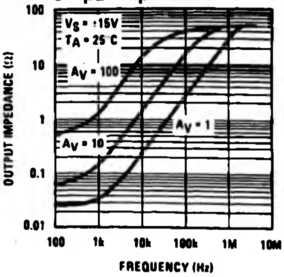
Power Supply Rejection Ratio



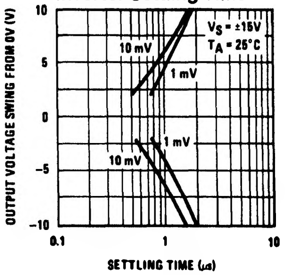
Equivalent Input Noise Voltage



Open Loop Voltage Gain (V/V)



Output Impedance



Inverter Settling Time

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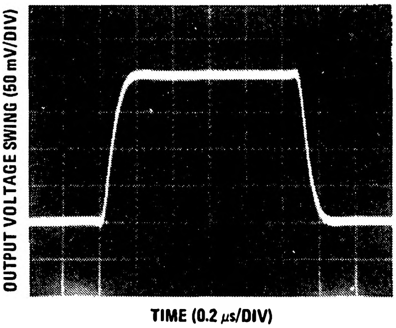
Pulse Response


Small Signal Inverting

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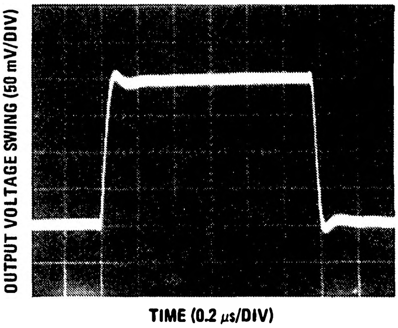
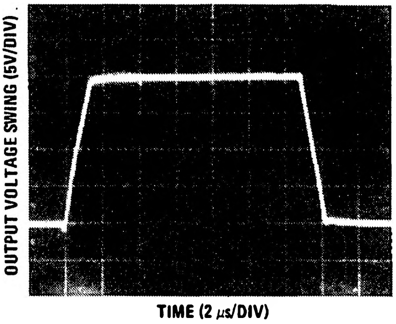
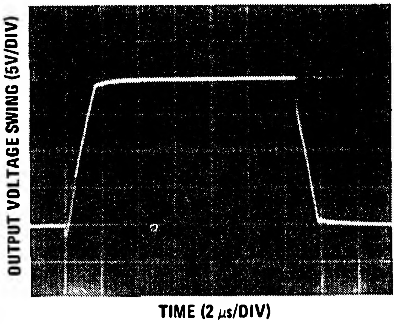

Small Signal Non-Inverting

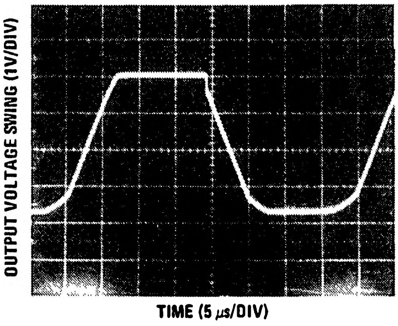
TL/H/9710-7


Large Signal Inverting

TL/H/9710-8


Large Signal Non-Inverting

TL/H/9710-9


Current Limit (R_L = 100 Ω)

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Application Hints

These devices are op amps with an internally trimmed input offset voltage and JFET input devices (BI-FET II). These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit with the non-inverting input, or with both inputs, will force the output to a high state, potentially causing a reversal of phase to the output. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

The amplifiers will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

Each amplifier is individually biased by a zener reference which allows normal circuit operation on ±5V power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate.

The amplifiers will drive a 2 kΩ load resistance to ±10V over the full temperature range of 0°C to +70°C. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

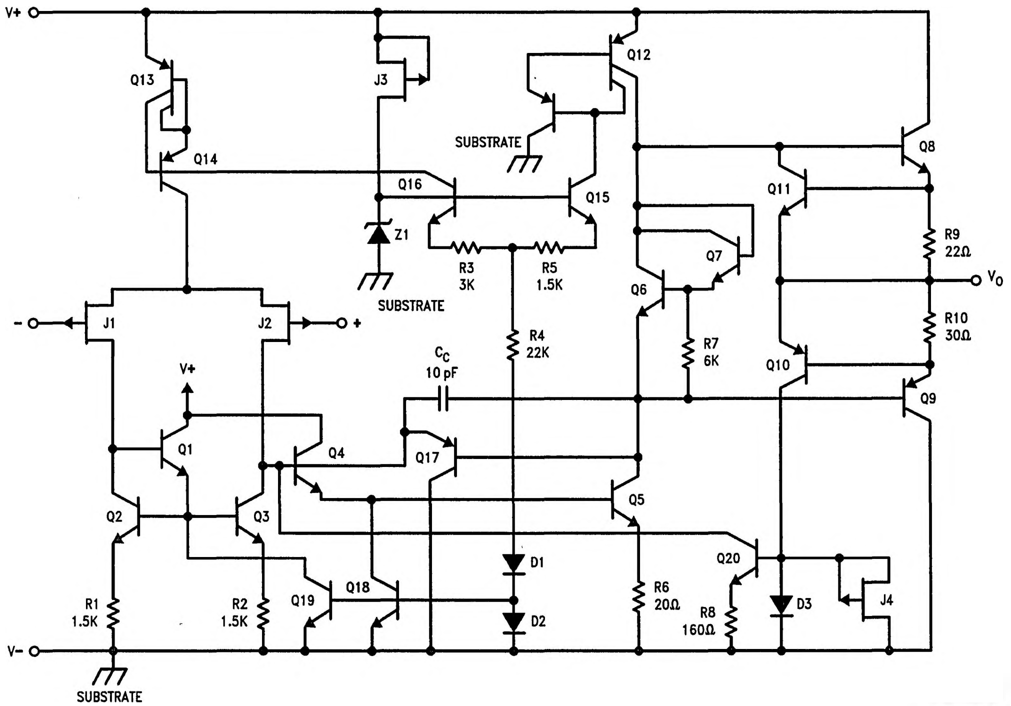
Because these amplifiers are JFET rather than MOSFET input op amps they are more resistant to ESD (see Absolute Maximum Ratings).

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive.The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

The benefit of the SO package results from its very small size. It follows, however, that the die inside the SO package is less protected from external physical forces than a die in a standard DIP would be, because there is so much less plastic in the SO. Therefore, not following certain precautions when board mounting the LF453CM can put mechanical stress on the die, lead frame, and/or bond wires. This can cause shifts in the LF453CM's parameters, even causing them to exceed limits specified in the Electrical Characteristics. For recommended practices in LF453CM surface mounting refer to Application Note AN450 "Surface Mounting Methods and Their Effect on Product Reliability" and to the section titled "Surface Mount" found in any Rev 1. Linear Databook volume.

Detailed Schematic



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