# MONOLITHIC SAMPLE AND HOLD CIRCUITS — LF198/LF298/LF398

## DESCRIPTION

The Signetics LF198/LF298/LF398 are monolithic sample and hold circuits which utilize high-voltage Ion Implant JFET technology to obtain ultra-high DC accuracy with fast acquisition of signal and low droop rate. Operating as a unity gain follower, DC gain accuracy is 0.002% typical and acquisition time is as low as 6μs to 0.01%. A bipolar input stage is used to achieve low offset voltage and wide bandwidth. Input offset adjust is accomplished with a single pin and does not degrade input offset drift. The wide bandwidth allows the LF198 to be included inside the feedback loop of 1MHz op amps without having stability problems. Input impedance of $10^{10}\Omega$ allows high source impedances to be used without degrading accuracy.

P-channel junction FET's are combined with bipolar devices in the output amplifier to give droop rates as low as 5mV/min with a 1μF hold capacitor. The JFET's have much lower noise than MOS devices used in previous designs and do not exhibit high temperature instabilities. The overall design guarantees no feed-through from input to output in the hold mode even for input signals equal to the supply voltages.

Logic inputs are fully differential with low input current, allowing direct connection to TTL, PMOS, and CMOS. Differential threshold is 1.4V. The LF198/LF298/LF398 will operate from ±5V to ±18V supplies. They are available in an 8-lead TO-5 package, or an 8-pin plastic DIP.

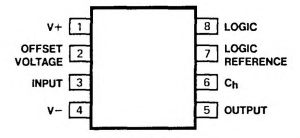
## FEATURES

- **Operates from ±5V to ±18V supplies**
- **Less than 10μs acquisition time**
- **TTL, PMOS, CMOS compatible logic input**
- **0.5mV typical hold step at $C_h$ = 0.01μF**
- **Low input offset**
- **0.002% gain accuracy**
- **Low output noise in hold mode**
- **Input characteristics do not change during hold mode**
- **High supply rejection ratio in sample or hold**
- **Wide bandwidth**

## APPLICATIONS

- **The LF198/LF298/LF398 are ideally suited for a wide variety of sample and hold applications including data acquisition, analog-to-digital conversion, synchronous demodulation, and automatic test setup.**

**F,N PACKAGE**

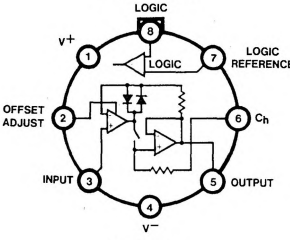



TOP VIEW

**ORDER NUMBERS**

LF198F, LF298F, LF398F
LF198N, LF298N, LF398N

**H PACKAGE**

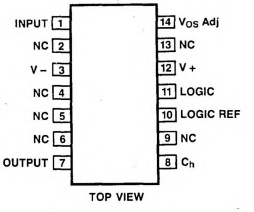



TOP VIEW

**ORDER NUMBERS**

LF198H, LF298H, LF398H

**D³ PACKAGE**



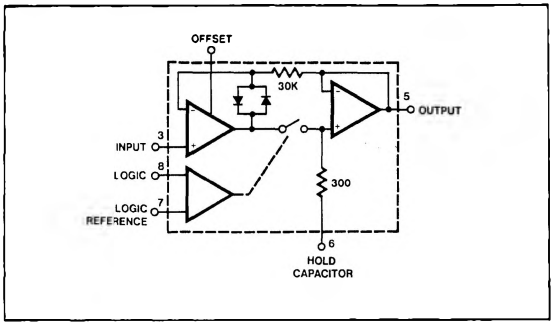

TOP VIEW

**ORDER NUMBER**

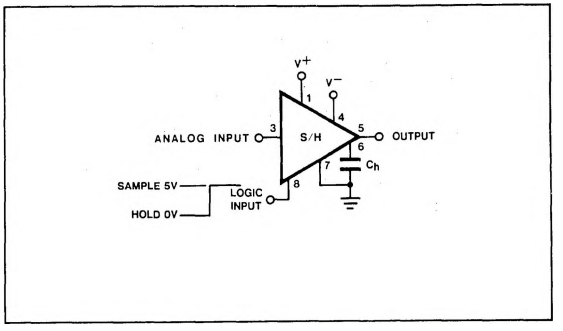
LF398D

NOTES:
1. SOL - Released in Large SO package only.
2. SOL and non-standard pinout.
3. SO and non-standard pinouts.

## FUNCTIONAL DIAGRAM




## TYPICAL APPLICATIONS



# MONOLITHIC SAMPLE AND HOLD CIRCUITS — LF198/LF298/LF398

## ABSOLUTE MAXIMUM RATINGS

| PARAMETER | RATING | UNIT |
|---|---|---|
| Supply voltage | ± 18 | V |
| Power dissipation (package limitation)[1] | 500 | mW |
| Operating ambient temperature range | | |
| LF198 | −55 to +125 | °C |
| LF298 | −25 to +85 | °C |
| LF398 | 0 to +70 | °C |
| Storage temperature range | −65 to +150 | °C |
| Input voltage | Equal to supply voltage | |
| Logic to logic reference differential voltage[2] | +7, −30 | V |
| Output short circuit duration | Indefinite | |
| Hold capacitor short circuit duration | 10 | sec |
| Lead temperature (soldering, 10sec) | 300 | °C |

## DC ELECTRICAL CHARACTERISTICS

Unless otherwise specified, the following conditions apply. Unit is in "sample" mode, $V_S = \pm 15V$, $T_j = 25°C$, $-11.5V \leq V_{IN} \leq +11.5V$, $C_h = 0.01\mu F$, and $R_L = 10k\Omega$. Logic reference voltage = OV and logic voltage = 2.5V.

| PARAMETER | TEST CONDITIONS | LF198/LF298 | | | LF398 | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Input offset voltage[6] | $T_j = 25°C$ | | 1 | 3<br>5 | | 2 | 7<br>10 | mV<br>mV |
| Input bias current[6] | $T_j = 25°C$<br>Full temperature range | | 5 | 25<br>75 | | 10 | 50<br>100 | nA<br>nA |
| Input impedance | $T_j = 25°C$ | | $10^{10}$ | | | $10^{10}$ | | Ω |
| Gain error | $T_j = 25°C$, $R_L = 10K$<br>Full temperature range | | 0.002 | 0.005<br>0.02 | | 0.004 | 0.01<br>0.02 | %<br>% |
| Feedthrough attenuation ratio at 1kHz | $T_j = 25°C$, $C_h = 0.01\mu F$ | 86 | 96 | | 80 | 90 | | dB |
| Output impedance | $T_j = 25°C$, "HOLD" mode<br>Full temperature range | | 0.5 | 2<br>4 | | 0.5 | 4<br>6 | Ω<br>Ω |
| "HOLD" step[4] | $T_j = 25°C$, $C_h = 0.01\mu F$, $V_{OUT} = 0$ | | 0.5 | 2.0 | | 1.0 | 2.5 | mV |
| Supply current[6] | $T_j \leq 25°C$ | | 4.5 | 5.5 | | 4.5 | 6.5 | mA |
| Logic and logic reference input current | $T_j = 25°C$ | | 2 | 10 | | 2 | 10 | μA |
| Leakage current into hold capacitor[6] | $T_j = 25°C$[5], Hold mode | | 30 | 100 | | 30 | 200 | pA |
| Acquisition time to 0.1% | $\Delta V_{OUT} = 10V$, $C_h = 1000pF$<br>$C_h = 0.01\mu F$ | | 4<br>20 | | | 4<br>20 | | μs<br>μs |
| Hold capacitor charging current | $V_{IN} - V_{OUT} = 2V$ | | 5 | | | 5 | | mA |
| Supply voltage rejection ratio | $V_{OUT} = 0$ | 80 | 110 | | 80 | 110 | | dB |
| Differential logic threshold | $T_j = 25°C$ | 0.8 | 1.4 | 2.4 | 0.8 | 1.4 | 2.4 | V |

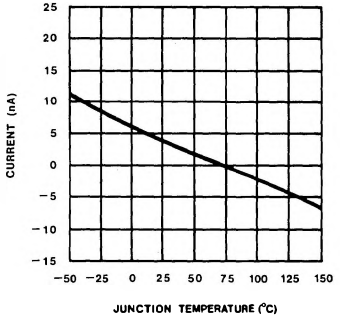
NOTES

1. The maximum junction temperature of the LF398 is 150°C. When operating at elevated ambient temperature, the TO-5 and plastic DIP packages must be derated based on a thermal resistance (θjA) of 150°C/W.
2. Although the differential voltage may not exceed the limits given, the common-mode voltage on the logic pins may be equal to the supply voltages without causing damage to the circuit. For proper logic operation, however, one of the logic pins must always be at least 2V below the positive supply and 3V above the negative supply.
3. Unless otherwise specified, the following conditions apply. Unit is in "sample" mode, $V_S = \pm 15V$, $T_j = 25°C$, $-11.5V \leq V_{IN} \leq +11.5V$, $C_h = 0.01\mu F$, and $R_L = 10k$. Logic reference voltage = OV and logic voltage = 2.5V.
4. Hold step is sensitive to stray capacitive coupling between input logic signals and the hold capacitor. 1pF, for instance, will create an additional 0.5mV step with a 5V logic swing and a 0.01μF hold capacitor. Magnitude of the hold step is inversely proportional to hold capacitor value.
5. Leakage current is measured at a junction temperature of 25°C. The effects of junction temperature rise due to power dissipation or elevated ambient can be calculated by doubling the 25°C value for each 11°C increase in chip temperature. Leakage is guaranteed over full input signal range.
6. The parameters guaranteed over a supply voltage of ±5 to ± 18V.

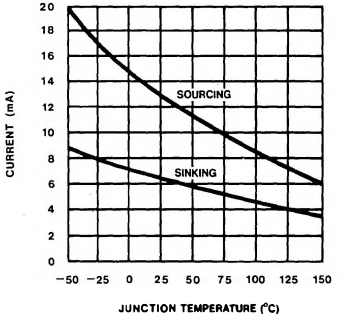
# MONOLITHIC SAMPLE AND HOLD CIRCUITS — LF198/LF298/LF398

## TYPICAL DC PERFORMANCE CHARACTERISTICS

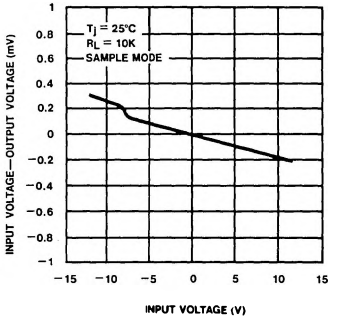
### INPUT BIAS CURRENT



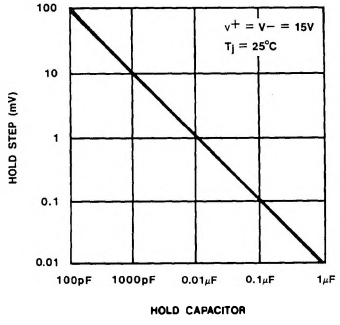

### OUTPUT SHORT CIRCUIT CURRENT



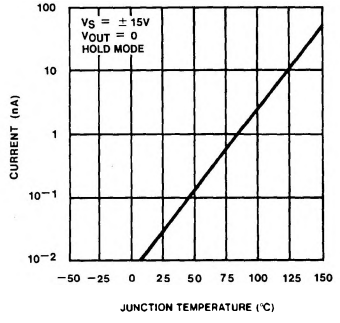

### GAIN ERROR



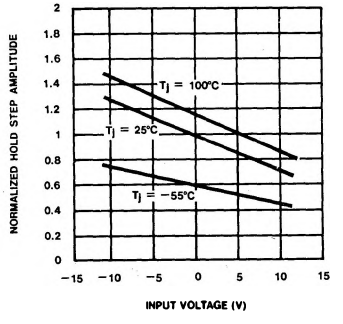

### HOLD STEP




### LEAKAGE CURRENT INTO HOLD CAPACITOR

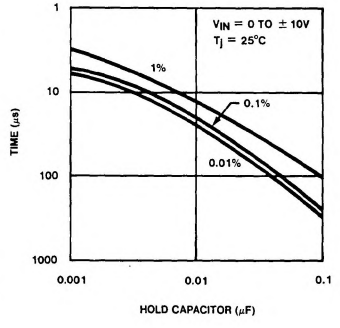



### HOLD STEP INPUT VOLTAGE

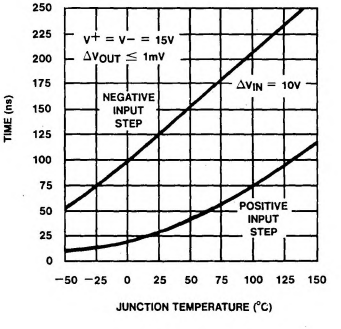



## TYPICAL AC PERFORMANCE CHARACTERISTICS

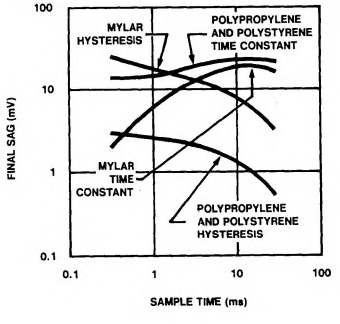
### ACQUISITION TIME




### APERTURE TIME

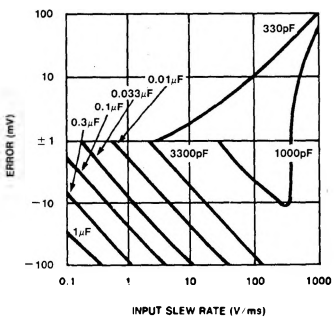



### CAPACITOR HYSTERESIS

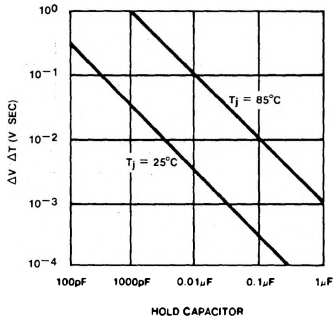


## TYPICAL AC PERFORMANCE CHARACTERISTICS (cont'd)

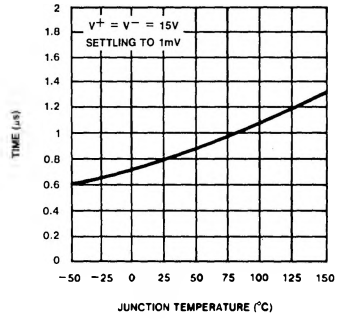
### DYNAMIC SAMPLING ERROR



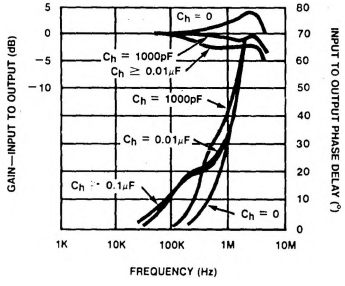

### OUTPUT DROOP RATE



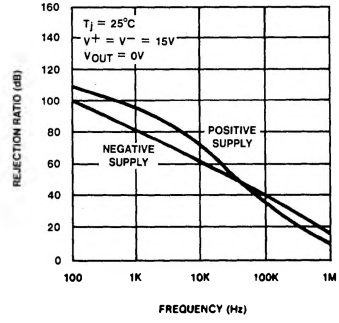

### "HOLD" SETTLING TIME



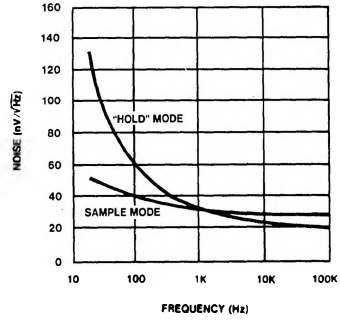

### PHASE AND GAIN (INPUT TO OUTPUT, SMALL SIGNAL)




### POWER SUPPLY REJECTION




### OUTPUT NOISE




### FEEDTHROUGH REJECTION RATIO (HOLD MODE)