Ordering number: EN2577B

CMOS LSI

No.2577B

LC6538D

SINGLE-CHIP 4-BIT MICROCOMPUTER FOR LARGE-SCALE CONTROL-ORIENTED APPLICATIONS

(with FLT Controller/Drivers, Comparator, PWM Output, 8K Byte-ROM)

The LC6538D is a single-chip 4-bit microcomputer placed in a 64-pin package. It contains a high-speed CPU (minimum cycle time: 0.92μs) which is the heart of the LC6538D, an 8K-byte ROM, a 448-word RAM, an automatic FLT display controller/drivers, a dual 8-bit serial I/O port, an 8-bit timer, an interval timer capable of delivering 14-bit PWM output signal or 8-bit + 6-bit PWM output signal, a 14-bit time-keeping time base timer which can be also used as an event counter or watchdog timer, a 4-channel comparator input port, a horizontal sync detection counter, and provides 8 interrupt sources with 4 vector addresses. The LC6358D has 2 crystal oscillators (4.19MHz and 32.768kHz) which make it possible to select either clock signal for system clock or time-keeping as required and also make it possible to use either clock signal to continue time-keeping in the standby mode. The LC6538D is especially suited for use in VCR, CD, ECR applications. In particular, the LC6538D is so designed as to facilitate processing of the time-keeping/timer function, voltage/frequency synthesizer tuner control, remote control signal reception, tape counter, etc. on a single chip. Since the FLT display controller has the static output mode and structure capable of being also used as a general-purpose output port, the LC6538D is also especially suited for use in VCR, CD system/servo controller applications.

Features

- 78 instructions
- On-chip 8192-byte ROM, 448x4-bit RAM (64x4 bits of the 448x4-bit RAM are used both for data memory and display, KEY Return Data memory.)
- Minimum instruction cycle time: 0.92μs (4.33MHz, $V_{DD} \geqq 4.5V$)
  61μs (32.768kHz, $V_{DD} \geqq 2.7V$)
- Power-down function available when a system clock signal is selected (program-selectable)
  - When 4.19MHz clock signal is selected: 0.95μs, 1.9μs, 30.6μs
  - When 32.768kHz clock signal is selected: 61μs
- Working register/flag function
  - (16 flags + 8 working registers) x 4 banks
- Stack level: 16 levels
- I/O port: 55 pins in all
  - Input-only port 4 pins (common with comparator input)
  - Input/output common port 27 pins (high-current port for LED drive: 8 pins)
  - Output-only port 24 pins (FLT direct drive capability, high-current output for digits: 16 pins)
- On-chip FLT display controller
  - Number of segments: 8 to 12 Program-selectable
  - Number of digits: 16 to 8 Program-selectable
- On-chip automatic KEY Return Data input function
  - 4x15-bit
- Timer: 3 channels
  - 6-bit prescaler + 8-bit programmable timer
  - Interval timer: Common with PWM DAC, capable of frequency division for melody generation
  - Time-keeping time base timer: On-chip 14-stage frequency divider
- PWM DAC output: Common with Timer 1 (Interval Timer)
  - 6-bit PWM DAC + 8-bit PWM DAC or 14-bit PWM DAC
- Serial input/output interface (LSB first)
  - 8-bit input/output x 2 channels or 16-bit input/output x 1 channel
- Interrupt function: 8 sources, 4 vector addresses
  - External interrupt 2 lines
  - Timer interrupt 3 lines
  - Serial I/O interrupt 2 lines
  - Digit interrupt 1 line
- On-chip comparator for AFC signal detection (4 channels)

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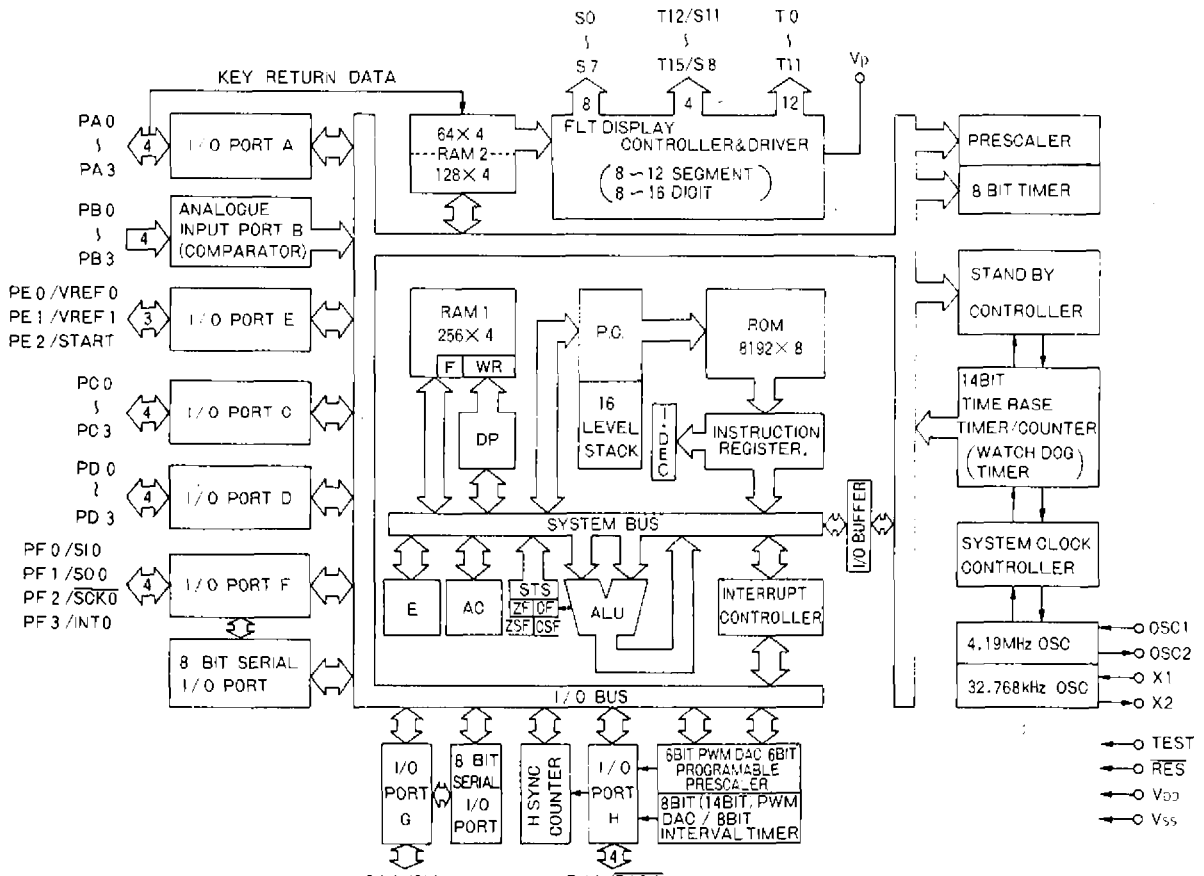
- On-chip watchdog timer: Common with time-keeping time base timer (Option)
- On-chip 9-bit counter for horizontal sync detection
- On-chip OSC stabilizing time wait function in the reset mode
- OSC curcuit: 2 channels
  - Main clock: 4.19MHz crystal OSC or 4.0MHz ceramic resonator OSC
  - Subclock: 32.768kHz crystal OSC
- Standby function: 2 modes of HALT and HOLD
- Supply voltage: 2.7 to 6.0V
- Package: DIP-64S
- Evaluation LSI: LC6593 (evaluation chip) + EVA800-TB6593 (evaluation chip board)
  LC65PG38D (piggyback)

System Block Diagram



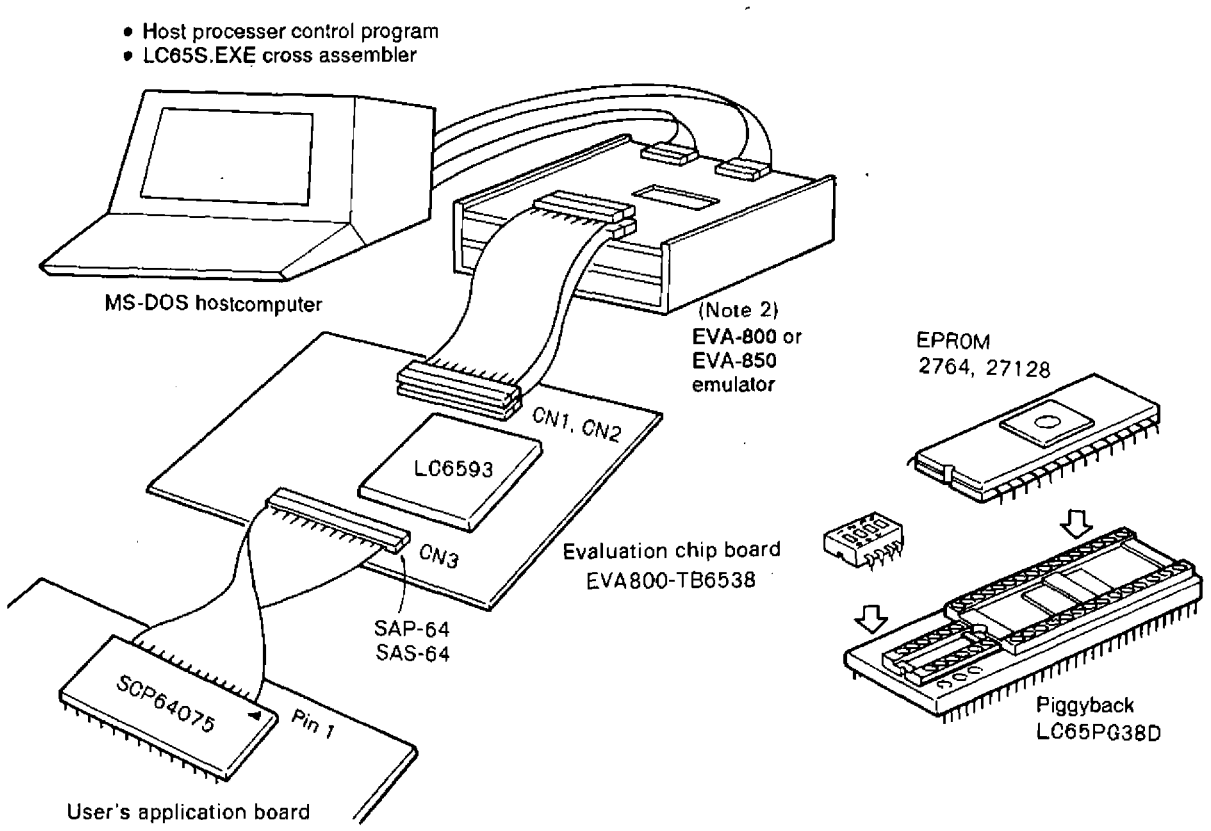
PG0/SI1	PH0/$\overline{DAC0}$
PG1/SO1	PH1/$\overline{DAC1}$
PG2/$\overline{SCK1}$	PH2/SQR
PG3/$\overline{INT1}$	PH3/HCNT

Development Support Tools

The follwoing tools are provided to support the program development for the LC6538D microcomputer.

(1) User's Manual
"LC6538D User's Manual" (Issued in February, 1988)
(2) Developement Tool Manual
This contains the basic information on the EVA-800. For more detailed information on the LC6538D, refer to the description of Developement Support Tools in "LC6538D User's Manual".
(3) Development Tools
① For program development (Note 1)
i. MS-DOS-based host system and cross-assembler
ii. Cross assembler ..... MS-DOS base cross assembler: (LC65S.EXE)
② For program evaluation
i. Evaluation chip : LC6593
ii. Piggyback microcomputer: LC65PG38D
iii. Emulator : The EVA-800 controller board and evaluation chip board, or the EVA-850 emulator and evaluation chip board

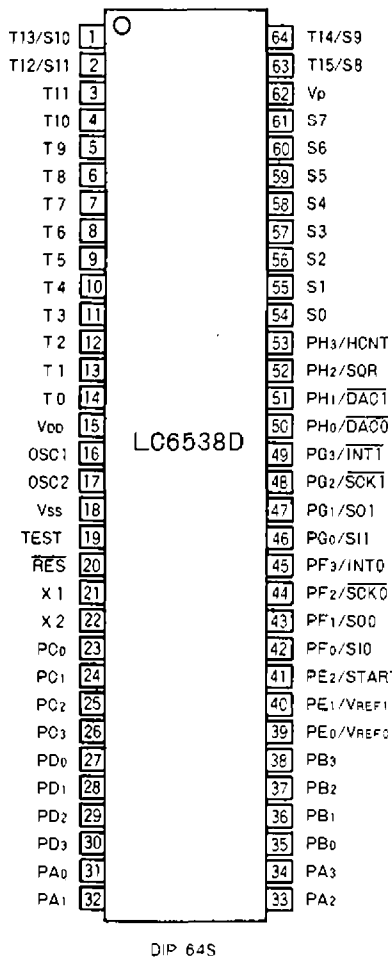
Appearance of Development Support System



(Note 1) MS-DOS: Trademark of MicroSoft Corporation

(Note 2) The EVA-800, EVA-850 is a general term for emulator. A suffix (A, B, ---) is added at the end of EVA-800, EVA-850 as the EVA-800, EVA-850 is improved to be a newer version. Do not use the EVA-800, EVA-850 with no suffix added.

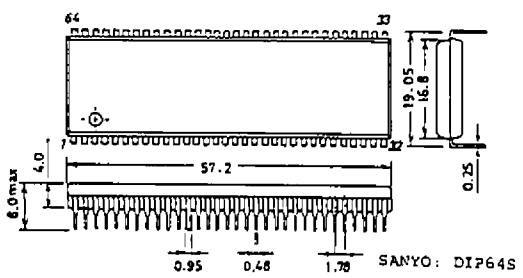
Pin Assignment



DIP 64S

OSC1, OSC2 : Crystal or ceramic resonator OSC circuit for main OSC
X1, X2 : Crystal OSC circuit for sub-OSC
PA_{0-3} : Input/output common port A_{0-3}, +15V breakdown voltage
PB_{0-3} : Reference voltage variable input-only port B_{0-3}
PC_{0-3} : Input/output common port C_{0-3}, +15V breakdown voltage
PD_{0-3} : Input/output common port D_{0-3}, +15V breakdown voltage
PE_{0-2} : Input/output common port E_{0-2}, PE_2 only has +15V breakdown voltage.
PF_{0-3} : Input/output common port F_{0-3}, +15V breakdown voltage
PG_{0-3} : Input/output common port G_{0-3}, +15V breakdown voltage
PH_{0-3} : Input/output common port H_{0-3}, +15V breakdown voltage
T0-T11 : Output port for digit only
T12/S11-T15/S8 : Output port for both digit/segment } P-channel high-voltage output
S0-S7 : Output port for segment only
Vp : Power supply pin for P-channel high-voltage output port
$\overline{RES}$: Reset
TEST : Test
V_{DD}, V_{SS} : Power supply pin
V_{REF0} : Comparator 0 reference voltage input pin
V_{REF1} : Comparator 1 reference voltage input pin
START : HALT control pin
SI0 : 8-bit/16-bit serial input port
SO0 : 8-bit/16-bit serial output port
$\overline{SCK0}$: Input/output for serial clock 0
INT0 : Interrupt 0 request input
SI1 : 8-bit serial input port
SO1 : 8-bit serial output port
$\overline{SCK1}$: Input/output for serial clock 1
$\overline{INT1}$: Interrupt 1 request input
$\overline{DAC0}$: 6-bit PWM output
$\overline{DAC1}$: 6-bit/14-bit PWM output
SQR : Burst pulse output
HCNT : Horizontal sync detection input

Package Dimensions 3071-D64IC
(unit: mm)



Pin Description

PU: Output with pull-up MOS
OD: Open drain output

Pin Name	Pins	I/O	Functions	Output Driver	Option	During Reset
V_{DD}	1	—	Power supply pin	—	—	—
V_{SS}	1	—				
TEST	1	I	LSI test pin. Must be connected to V_{SS}.	—	—	—
$\overline{RES}$	1	I	System reset input Initial reset at $\overline{RES}$=L	—	—	—
OSC1	1	I	Pin used for main system clock OSC For the external clock mode, the OSC2 is made open and the external clock is applied to the OSC1. With feedback resistance	—	—	—
OSC2	1	O				
X1	1	I	Pin used for sub-clock OSC For the external clock mode, the X2 is made open and the external clock is applied to the X1. With feedback resistance, damping resistance	—	—	—
X2	1	O				
T0 to T11	12	O	Output for FLT digit only Outputs a fixed address in the display RAM at the static mode.	Pch high breakdown voltage High-current type	Presence or absence of pull-down resistance (in bit units)	L
T12/S11 to T15/S8	4	O	Output for FLT digit/segment Outputs a fixed address in the display RAM at the static mode.	Pch high breakdown voltage High-current type	Presence or absence of pull-down resistance (in bit units)	L
S0 to S7	8	O	Output for FLT segment only Outputs a fixed address in the display RAM at the static mode.	Pch high breakdown voltage Medium-current type	Presence or absence of pull-down resistance (in bit units)	L
Vp	1		Power supply pin for FLT output pull-down resistance	—	—	—
PA_0 to PA_3	4	I/O	4-bit and single-bit input/output The input is of low threshold type for key scan and has the function to automatically fetch the key scan data into the RAM.	+15V breakdown voltage Medium-current type	PU or OD to be specified in bit units	H
PB_0 to PB_3	4	I	With 4-channel independint comparator Internal/external reference voltage selectable 4-bit/single-bit input The input function stops at the low-speed mode (1/32 mode, sub-clock mode).	—	—	Input function stop
PC_0 to PC_3	4	I/O	4-bit and single-bit input/output	+15V breakdown voltage High-current type	• PU or OD to be specified in bit units • Output at the reset mode	H/L (option)
PD_0 to PD_3	4	I/O	4-bit and single-bit input/output	+15V breakdown voltage High-current type	• PU or OD to be specified in bit units • Output at the reset mode	H/L (option)

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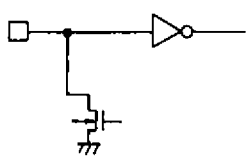
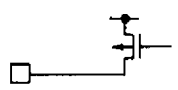
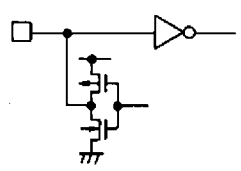
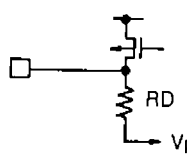
Pin Name	Pins	I/O	Functions	Output Driver	Option	During Reset
PE_0 to PE_2	3	I/O	3-bit and single-bit input/output PE_0/V_{REF0} Common with external reference voltage input of PB_{1-3} PE_1/V_{REF1} Common with external reference voltage input of PB_0 PE_2/START Common with HALT mode control START	PE_2 only: +15V breakdown voltage Other pins: Normal voltage Medium-current type	PU or OD to be specified in bit units	H
PF_0 to PF_3	4	I/O	4-bit and single-bit input/output PF_0/SI0 Common with serial input SI0 PF_1/SO0 Common with serial output SO0 $PF_2/\overline{SCK0}$ Common with serial clock input/output $\overline{SCK0}$ PF_3/INT0 Common with INT0 interrupt input	+15V breakdown voltage Medium-current type	PU or OD to be specified in bit units	H
PG_0 to PG_3	4	I/O	4-bit and single-bit input/output PG_0/SI1 Common with serial input SI1 PG_1/SO1 Common with serial output SO1 $PG_2/\overline{SCK1}$ Common with serial clock input/output $\overline{SCK1}$ $PG_3/\overline{INT1}$ Common with $\overline{INT1}$ interrupt input	+15V breakdown voltage Medium-current type	PU or OD to be specified in bit units	H
PH_0 to PH_3	4	I/O	4-bit and single-bit input/output $PH_0/\overline{DAC0}$ Common with 6-bit PWM D/A output $PH_1/\overline{DAC1}$ Common with 8/14-bit PWM D/A output PH_2/SQR Common with burst pulse output PH_3/HCNT Common with horizontal sync detection input	+15V breakdown voltage Medium-current type	PU or OD to be specified in bit units	H

User Options

1) Option of ports C, D Output Level at the Reset Mode.
For input/output common ports C, D, either of the following two output levels may be selected in a group of 4 bits during reset by option.

Option Name	Conditions, etc.
1. Output at the reset mode: "H" level	All of 4 bits of ports C, D
2. Output at the reset mode: "L" level	All of 4 bits of ports C, D

2) Option of Port Output Configuration
For each input/output common port, either of the following two output configurations may be selected by option (in bit units).

Option Name	Circuit	Conditions, etc.
1. Open drain output		Ports A, C, D, E, F, G, H
		T0~T11, T12/S11~T15/S8, S0~S7
2. Output with pull-up resistance		Ports A, C, D, E, F, G, H
3. Output with pull-down resistance		T0~T11, T12/S11~T15/S8, S0~S7

3) Watchdog Reset Option
The presence or absence of the time base timer-used watchdog reset function may be selected by option.

Option Name	Conditions, etc.
1. With watchdog reset function	Programming must be made so that the time base interrupt request flag is reset within a certain period of time not to cause the watchdog reset to be performed as long as no runaway occurs.
2. Without watchdog reset function	—

LC6538D Electrical Characteristics

1. Absolute Maximum Ratings at T_a=25°C, V_{SS}=0V

Parameter	Symbol	Applicable Pins, Remarks	Conditions	Limits	Unit
Maximum Supply Voltage	V_{DD} max	V_{DD}		−0.3 to +7.0	V
Output Voltage	V_O(1)	X2,OSC2		Allowable up to voltage generated	V
	V_O(2)	To to T11, T12/S11 to T15/S8, S0 to S7		V_{DD}−45 to V_{DD}+0.3	V
Input Voltage	V_I(1)	X1, OSC1		Allowable up to voltage generated	V
	V_I(2)	TEST, RES, PB0 to 3, OSC1, X1 at external clock mode		−0.3 to V_{DD}+0.3	V
	V_I(3)	Vp		V_{DD}−45 to V_{DD}+0.3	V
Input/Output Voltage	V_{IO}(1)	Ports A,C,D,E2,F,G,H	At open drain output option	−0.3 to +15	V
	V_{IO}(2)	Ports E0,E1		−0.3 to V_{DD}+0.3	V
		Ports A,C,D,E2,F,G,H	At pull-up MOS-provided output option	−0.3 to V_{DD}+0.3	V
Peak Output Current	I_{OP}(1)	Ports A,E,F,G,H		−2 to 10	mA
	I_{OP}(2)	Ports C,D		−2 to 30	mA
	I_{OP}(3)	T0 to T11, T12/S11 to T15/S8		−30 to 0	mA
	I_{OP}(4)	S0 to S7		−10 to 0	mA
Average Output Current	I_{OA}(1)	Ports A,E,F,G,H	Per pin Average over the period of 100 msec.	−2 to 10	mA
	I_{OA}(2)	Ports C,D	Per pin Average over the period of 100 msec.	−2 to 30	mA
	I_{OA}(3)	T0 to T11, T12/S11 to T15/S8	Per pin Average over the period of 100 msec.	−30 to 0	mA
	I_{OA}(4)	S0 to S7	Per pin Average over the period of 100 msec.	−10 to 0	mA
	ΣI_{OA}(1)	Ports A,E	Total current of all applicable pins Average over the period of 100msec.	−14 to 20	mA
	ΣI_{OA}(2)	Ports F,G,H	Total current of all applicable pins Average over the period of 100msec.	−24 to 60	mA
	ΣI_{OA}(3)	Ports C,D	Total current of all applicable pins Average over the period of 100msec.	−16 to 80	mA
	ΣI_{OA}(4)	T0 to T11, T12/S11 to T15/S8, S0 to S7	Total current of all applicable pins Average over the period of 100msec.	−100 to 0	mA
Allowable Power Dissipation	Pd max	DIP64S	T_a=−30 to +70°C	600	mW
Operating Temperature	Topr			−30 to +70	°C
Storage Temperature	Tstg			−55 to +125	°C

2. Allowable Operating Conditions at Ta=−30 to +70°C, V_{SS}=0V

Parameter	Symbol	Applicable Pins, Remarks	Conditions	V_{DD}[V]	Limits min	typ	max	Unit
Operating Supply Voltage (Including supply voltage at standby mode)	$V_{DD}(1)$	V_{DD}	0.92μs≦Tcyc <1.9μs	—	4.5		6.0	V
	$V_{DD}(2)$	V_{DD}	1.9μs≦Tcyc ≦6μs	—	4.0		6.0	V
	$V_{DD}(3)$	V_{DD}	6μs<Tcyc ≦67μs	—	3.0		6.0	V
	$V_{DD}(4)$	V_{DD}	4.19MHz OSC stop, 32kHz OSC operating	—	2.7		6.0	V
Memory Retention Supply Voltage	V_{ST}	V_{DD}	At operation completely stopped mode (HOLD mode)	—	1.8		6.0	V
"H"-Level Input Voltage	$V_{IH}(1)$	Port A of OD type	Output Nch Tr OFF	3.0 to 6.0	1.90		13.5	V
	$V_{IH}(2)$	Port A of PU type	Output Nch Tr OFF	3.0 to 6.0	1.90		V_{DD}	V
	$V_{IH}(3)$	Ports C, D of OD type	Output Nch Tr OFF	4.5 to 6.0	$0.70V_{DD}$		13.5	V
				3.0 to 6.0	$0.75V_{DD}$		13.5	V
	$V_{IH}(4)$	Ports C, D of PU type	Output Nch Tr OFF	4.5 to 6.0	$0.70V_{DD}$		V_{DD}	V
				3.0 to 6.0	$0.75V_{DD}$		V_{DD}	V
	$V_{IH}(5)$	Ports E2, F to H of OD type	Output Nch Tr OFF	4.5 to 6.0	$0.75V_{DD}$		13.5	V
				3.0 to 6.0	$0.80V_{DD}$		13.5	V
	$V_{IH}(6)$	Ports E2, F to H of PU type	Output Nch Tr OFF	4.5 to 6.0	$0.75V_{DD}$		V_{DD}	V
				3.0 to 6.0	$0.80V_{DD}$		V_{DD}	V
	$V_{IH}(7)$	Ports E0, E1	Output Nch Tr OFF	4.5 to 6.0	$0.75V_{DD}$		V_{DD}	V
				3.0 to 6.0	$0.80V_{DD}$		V_{DD}	V
	$V_{IH}(8)$	Port B	At internal reference voltage mode	4.0 to 6.0	$0.65V_{DD}$		V_{DD}	V
	$V_{IH}(9)$	OSC1, X1	Fig. 5, Fig. 6	4.5 to 6.0	$0.70V_{DD}$		V_{DD}	V
				3.0 to 6.0	$0.80V_{DD}$		V_{DD}	V
	$V_{IH}(10)$	$\overline{RES}$	Fig. 7	4.5 to 6.0	$0.75V_{DD}$		V_{DD}	V
				1.8 to 6.0	$0.80V_{DD}$		V_{DD}	V
"L"-Level Input Voltage	$V_{IL}(1)$	Port A	Output Nch Tr OFF	4.5 to 6.0	V_{SS}		0.5	V
				3.0 to 6.0	V_{SS}		0.35	V
	$V_{IL}(2)$	Ports C, D	Output Nch Tr OFF	4.5 to 6.0	V_{SS}		$0.30V_{DD}$	V
				3.0 to 6.0	V_{SS}		$0.25V_{DD}$	V
	$V_{IL}(3)$	Ports E, F, G, H	Output Nch Tr OFF	4.5 to 6.0	V_{SS}		$0.25V_{DD}$	V
				3.0 to 6.0	V_{SS}		$0.20V_{DD}$	V
	$V_{IL}(4)$	Port B	At internal reference voltage mode	4.0 to 6.0	V_{SS}		$0.35V_{DD}$	V
	$V_{IL}(5)$	$\overline{RES}$	Fig. 7	4.5 to 6.0	V_{SS}		$0.25V_{DD}$	V
				1.8 to 6.0	V_{SS}		$0.20V_{DD}$	V
	$V_{IL}(6)$	OSC1, X1	Fig. 5, Fig. 6	4.5 to 6.0	V_{SS}		$0.30V_{DD}$	V
				3.0 to 6.0	V_{SS}		$0.20V_{DD}$	V
	$V_{IL}(7)$	TEST		4.5 to 6.0	V_{SS}		$0.30V_{DD}$	V
				3.0 to 6.0	V_{SS}		$0.25V_{DD}$	V
Common-Mode Input Voltage Range	V_{CMM}	Port B	Offset voltage ≦V_{OFS}	4.5 to 6.0	$V_{SS}+1.0$		$V_{DD}-1.5$	V
Instruction Cycle Time	T_{CYC}		(Note 1)	(Note 1)	0.92		67	μs
Main Clock OSC Frequency Range	f_{OSC}	OSC1, OSC2	Crystal, ceramic resonator OSC (Note 1) Fig. 1	3.0 to 6.0	3.5	4.19	4.2	MHz
Main Clock Input Frequency Range	f_{EOSC}	OSC1	External clock (Note 1) Fig. 5	3.0 to 6.0	2.0		4.33	MHz
Main Clock Input "H"-Level Pulse Width	t_{WOSCH}	OSC1	External clock Fig. 5	3.0 to 6.0	100			ns
Main Clock Input "L"-Level Pulse Width	t_{WOSCL}	OSC1	External clock Fig. 5	3.0 to 6.0	100			ns
Main Clock Rise Time	t_{OSCR}	OSC1	External clock Fig. 5	3.0 to 6.0			30	ns

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Parameter	Symbol	Applicable Pins, Remarks	Conditions		Limits			
				V_{DD}[V]	min	typ	max	Unit
Main Clock Fall Time	t_{OSCF}	OSC1	External clock Fig. 5	3.0 to 6.0			30	ns
Main Clock OSC Constant	CO1, CO2		Fig. 1	3.0 to 6.0	Refer to Table 1.			—
Sub-clock OSC Frequency Range	f_X	X1, X2	Crystal OSC Fig. 2	2.7 to 6.0	30	32.768	35	kHz
Sub-clock Input Frequency Range	f_{EX}	X1	External clock Fig. 6	2.7 to 6.0	30		35	kHz
Sub-clock Input "H"-Level Pulse Width	t_{WXH}	X1	External clock Fig. 6	2.7 to 6.0	6		34	μs
Sub-clock Input "L"-Level Pulse Width	t_{WXL}	X1	External clock Fig. 6	2.7 to 6.0	6		34	μs
Sub-clock Input Rise Time	t_{XR}	X1	External clock Fig. 6	2.7 to 6.0			0.2	μs
Sub-clock Input Fall Time	t_{XF}	X1	External clock Fig. 6	2.7 to 6.0			0.2	μs
Sub-clock OSC Constant	CX1, CX2		Fig. 2	2.7 to 6.0	Refer to Table 2.			—

(Note 1) Since the frequency also depends on the supply voltage and operating cycle time, both must be referred to.

3. Electrical Characteristics at $T_a = -30$ to $+70°C$, $V_{SS} = 0V$

Parameter	Symbol	Applicable Pins, Remarks	Conditions	V_{DD}[V]	Limits min	typ	max	Unit
"H"-Level Input Current	$I_{IH}(1)$	Ports A, C, D, E2, F to H of OD type	Output Nch Tr OFF (Including Nch Tr OFF leakage current) V_{IN}=+13.5V	2.7 to 6.0			5.0	μA
	$I_{IH}(2)$	Ports E0, E1	Output Nch Tr OFF (Including Nch Tr OFF leakage current) $V_{IN}=V_{DD}$	2.7 to 6.0			1.0	μA
		Port B, $\overline{RES}$	$V_{IN}=V_{DD}$					
	$I_{IH}(3)$	OSC1, X1	$V_{IN}=V_{DD}$	2.7 to 6.0			10	μA
"L"-Level Input Current	$I_{IL}(1)$	Ports A, C to H of OD type	Output Nch Tr OFF $V_{IN}=V_{SS}$	2.7 to 6.0	−1.0			μA
		Port B	$V_{IN}=V_{SS}$	2.7 to 6.0	−1.0			μA
	$I_{IL}(2)$	Ports A, C to H of PU type	Output Nch Tr OFF $V_{IN}=V_{SS}$	2.7 to 6.0	−1.3	−0.35		mA
	$I_{IL}(3)$	OSC1, X1	$V_{IN}=V_{SS}$	2.7 to 6.0	−10			μA
	$I_{IL}(4)$	$\overline{RES}$	$V_{IN}=V_{SS}$	2.7 to 6.0	−60	−25		μA
"H"-Level Output Voltage	$V_{OH}(1)$	Ports A, C to H of PU type	I_{OH}=−50μA	4.0 to 6.0	V_{DD}−1.2			V
	$V_{OH}(2)$	Ports A, C to H of PU type	I_{OH}=−10μA	3.0 to 6.0	V_{DD}−0.5			V
	$V_{OH}(3)$	T0 to T11, T12/S11 to T15/S8	I_{OH}=−20mA	4.0 to 6.0	V_{DD}−1.8			V
	$V_{OH}(4)$	T0 to T11, T12/S11 to T15/S8	I_{OH}=−1mA I_{OH} in other ports is less than −1mA.	3.0 to 6.0	V_{DD}−1.0			V
	$V_{OH}(5)$	S0 to S7	I_{OH}=−5mA	4.0 to 6.0	V_{DD}−1.8			V
	$V_{OH}(6)$	S0 to S7	I_{OH}=−1mA I_{OH} in other ports is less than −1mA.	3.0 to 6.0	V_{DD}−1.0			V
"L"-Level Output Voltage	$V_{OL}(1)$	Ports C, D	I_{OL}=20mA	4.0 to 6.0			1.5	V
	$V_{OL}(2)$	Ports C, D	I_{OL}=2mA I_{OL} in other ports is less than 1mA.	3.0 to 6.0			0.5	V
	$V_{OL}(3)$	Ports A, E to H	I_{OL}=5mA	4.0 to 6.0			1.5	V
	$V_{OL}(4)$	Ports A, E to H	I_{OL}=1mA I_{OL} in other ports is less than 1mA.	3.0 to 6.0			0.5	V
"L"-Level Output Current (Current flowing in pull-down resistor)	I_{OL}	T0 to T11, T12/S11 to T15/S8, S0 to S7 of PD type	Output Pch Tr OFF V_{OUT}=3.0V Vp=−35V	5.0	190	362	760	μA
Output OFF-State Leakage Current	$I_{OFF}(1)$	T0 to T11, T12/S11 to T15/S8, S0 to S7 of OD type	Output Pch Tr OFF $V_{OUT}=V_{DD}$	3.0 to 6.0			30	μA
	$I_{OFF}(2)$	T0 to T11, T12/S11 to T15/S8, S0 to S7 of OD type	Output Pch Tr OFF $V_{OUT}=V_{DD}$−40V	3.0 to 6.0	−30			μA
Resistance of Pull-up MOS Transistor	R_{Tru}	Ports A, C to H of PU type		5.0	6	15	24	kΩ
Pull-up Resistance	Ru	$\overline{RES}$		5.0	100	220	400	kΩ
Pull-down Resistance	Rd	T0 to T11, T12/S11 to T15/S8, S0 to S7 of PD type		5.0	50	105	200	kΩ
Main Clock OSC Stabilizing Period	t_{MXS}	OSC1, OSC2	4.19MHz crystal OSC	3.0 to 6.0			30	ms
	t_{MCFS}	OSC1, OSC2	4.0MHz ceramic resonator OSC	3.0 to 6.0			10	ms

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Parameter	Symbol	Applicable Pins, Remarks	Conditions	V_{DD}[V]	Limits min	typ	max	Unit
Sub-clock OSC Stabilizing Period	t_{SXS}	X1, X2	32.768kHz crystal OSC	2.7 to 6.0			10	s
Serial Clock								
Input Clock Cycle	$t_{CKCY}(1)$	$\overline{SCK0}$, $\overline{SCK1}$	Fig. 8	4.5 to 6.0	1.6			μs
Output Clock Cycle	$t_{CKCY}(2)$	$\overline{SCK0}$, $\overline{SCK1}$	Fig. 8	4.5 to 6.0	1.84			μs
Input Clock "L"-Level Pulse width (Note 2)	$t_{CKL}(1)$	$\overline{SCK0}$, $\overline{SCK1}$	Fig. 8	4.5 to 6.0	0.7			μs
Output Clock "L"-Level Pulse Width	$t_{CKL}(2)$	$\overline{SCK0}$, $\overline{SCK1}$	Fig. 8	4.5 to 6.0	0.92			μs
Input Clock "H"-Level Pulse Width (Note 2)	$t_{CKH}(1)$	$\overline{SCK0}$, $\overline{SCK1}$	Fig. 8	4.5 to 6.0	0.7			μs
Output Clock "H"-Level Pulse Width	$t_{CKH}(2)$	$\overline{SCK0}$, $\overline{SCK1}$	Fig. 8	4.5 to 6.0	0.92			μs
Input Clock Rise Time	$t_{CKR}(1)$	$\overline{SCK0}$, $\overline{SCK1}$	Fig. 8	4.5 to 6.0			3.0	μs
Output Clock Rise Time	$t_{CKR}(2)$	$\overline{SCK0}$, $\overline{SCK1}$	Fig. 8	4.5 to 6.0			0.1	μs
Input Clock Fall Time	$t_{CKF}(1)$	$\overline{SCK0}$, $\overline{SCK1}$	Fig. 8	4.5 to 6.0			3.0	μs
Output Clock Fall Time	$t_{CKF}(2)$	$\overline{SCK0}$, $\overline{SCK1}$	Fig. 8	4.5 to 6.0			0.1	μs
Serial Input								
Data Setup Time	t_{ICK}	SI0, SI1	Specified for ↓ of $\overline{SCK0}$, $\overline{SCK1}$ Fig. 8	4.5 to 6.0	0.2			μs
Data Hold Time	t_{CKI}	SI0, SI1		4.5 to 6.0	0.2			μs
Serial Output								
Output Delay Time	t_{CKO}	SO0, SO1	Specified from ↓ of $\overline{SCK0}$, $\overline{SCK1}$ External 1kΩ External 50pF Fig. 8	4.5 to 6.0			0.5	μs
Hysteresis Voltage	V_{HYS}	Ports E to H, $\overline{RES}$		3.0 to 6.0		$0.1V_{DD}$		V
Comparator Response Speed	T_{RS}	Port B	At 100mV overdrive mode	4.5 to 6.0			50	μs
Comparator Input Offset Voltage	V_{OFS}	Port B	V_{IN}=1.0V to V_{DD}−1.5V V_{REF}=1.0V to V_{DD}−1.5V	4.5 to 6.0		±20	±100	mV
Operating Current Dissipation (Note 3)	$I_{DDOP}(1)$	V_{DD}	4.19MHz x 1/1 high-speed operation mode (T_{CYC}=0.95μs) 32.768kHz sub-clock oscillating	4.5 to 6.0		4.5	10	mA
	$I_{DDOP}(2)$	V_{DD}	4.19MHz x 1/2 high-speed operation mode (T_{CYC}=1.9μs) 32.768kHz sub-clock oscillating	4.0 to 6.0		2.7	6	mA
	$I_{DDOP}(3)$	V_{DD}	4.19MHz x 1/32 low speed operation mode (T_{CYC}=30.5μs) 32.768kHz sub-clock oscillating	3.0		0.35	0.7	mA
				6.0		1.5	3	mA
	$I_{DDOP}(4)$	V_{DD}	32.768kHz low-speed operation mode (T_{CYC}=61μs) 4.19MHz main clock stop	2.7		0.035	0.12	mA
				6.0		0.4	1.2	mA

(Note 2) When using the internal clock, $T_{CKL(2)}$ and $T_{CKH(2)}$ (pins $\overline{SCK0}$ and $\overline{SCK1}$) have a minimum pulsewidth of 0.92 μs. This value is, however, dependent on the pull-up resistor and may, in some cases, be less than the above rating. The value of the pull-up resistance should be selected to ensure a minimum pulsewidth for $T_{CKL(1)}$ and $T_{CKH(1)}$ that is greater than the rated 0.7 μs.

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Parameter	Symbol	Applicable Pins, Remarks	Conditions	V_{DD}[V]	Limits min	typ	max	Unit
Standby Current Dissipation (Note 3)	$I_{DDST(1)}$	V_{DD}	4.19MHz main clock stop 32.768kHz sub-clock oscillating (HALT mode)	2.7		4	18	μA
				6.0		120	300	μA
	$I_{DDST(2)}$	V_{DD}	Complete standby (HOLD mode)	1.8		0.02	4	μA
				6.0		0.05	10	μA

(Note 3) The current flowing in the I/O port transistors and pull-up/pull-down resistors is excluded.

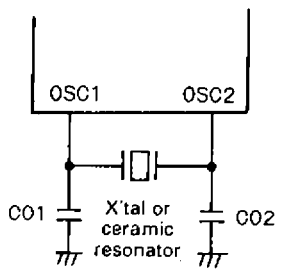


Fig. 1 Main Clock OSC Circuit

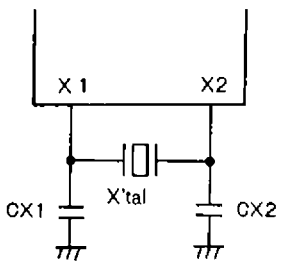


Fig. 2 Sub-clock Crystal OSC Circuit

Table 1 Main Clock OSC-Guaranteed Constants

OSC Mode	Maker	Resonator	CO1	CO2
4.194304MHz crystal OSC	Tokyo Denpa	HC-43/u CL=18pF Drive level =100mW	22pF	22pF
	Kinseki	HC-49/u CL=16pF	15pF	15pF
		HC-49/u CL=24pF	27pF	27pF
4.0MHz ceramic resonator OSC	Murata	CSA-4.00MG	33pF	33pF
		CST-4.00MG*1	Unnec-essary	Unnec-essary
	Kyocera	KBR-4.0MS	33pF	33pF
		KBR-4.0MES*1	Unnec-essary	Unnec-essary

The differential between CO1 and CO2 should be within ± 10%, including wiring capacitance.
*1: 3-pin ceramic resonator with on-chip capacitor

Table 2 Sub-clock Crystal OSC-Guaranteed Constants

OSC Mode	Maker	Resonator	CX1	CX2
32.768kHz crystal OSC	Kyocera	KF-38G-13200 CL=13pF	22pF	22pF
		KF-38G-10200 CL=10pF	20pF Trimmer	22pF

(Note) C_L: Internal load capacitance of crystal resonator

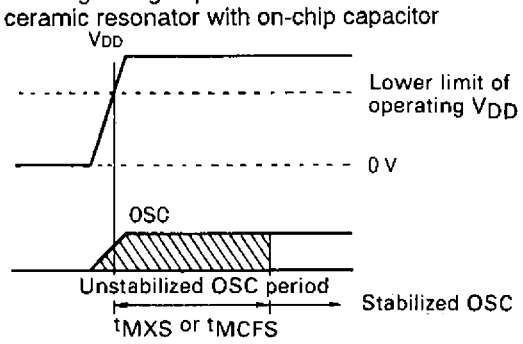


Fig. 3 Main Clock OSC Stalibizing Period

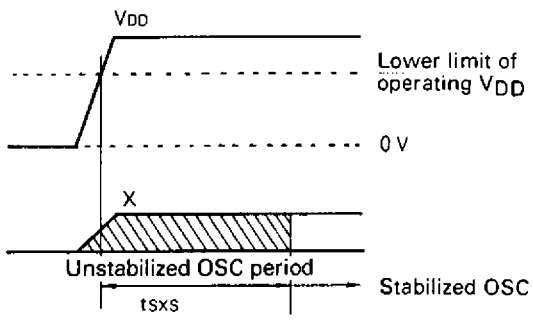


Fig. 4 Sub-clock OSC Stabilizing Period

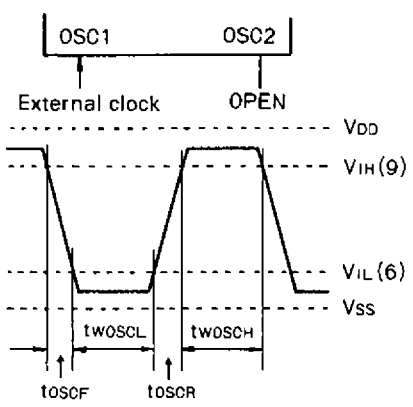


Fig. 5 Main Clock (External Clock) Input Waveform

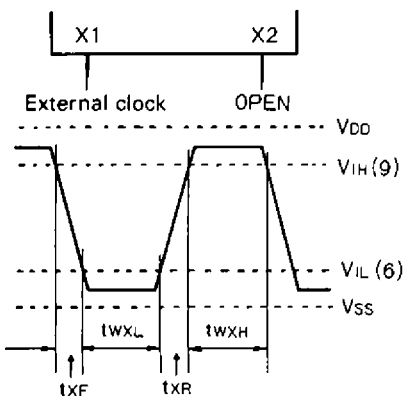
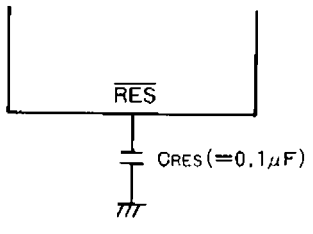
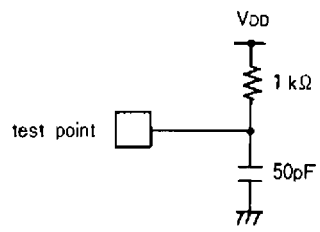


Fig. 6 Sub-clock (External Clock) Input Waveform



(Note)
When the rise time of the power supply is 0, the reset time becomes 10ms to 100ms at C_{RES}= 0.1μF.
If the rise time of the power supply is long, the value of C_{RES} must be fixed so that the reset time becomes longer than the main clock OSC stabilizing period.

Fig. 7 Reset Circuit



Serial Output Load

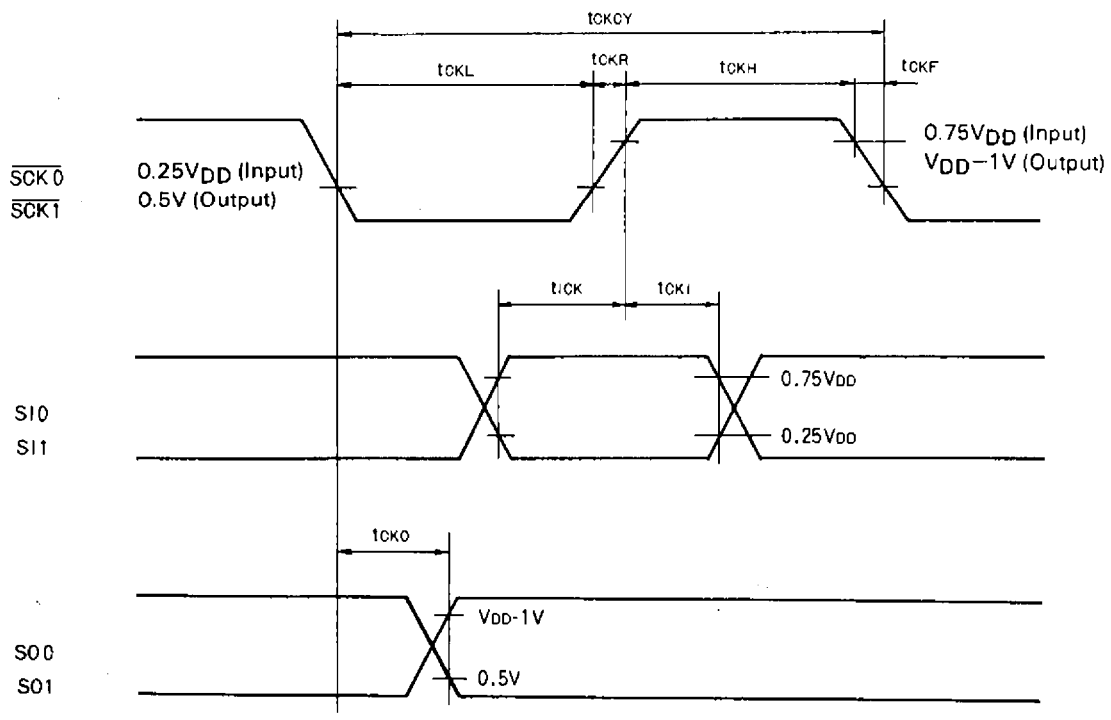


Fig. 8 Serial Clock Timing

Notes for Program Evaluation

- When evaluating the LC6538D with the evaluation chip (LC6593, LC65PG38D), the following must be observed.

Classification	Item	Function		Notes for evaluation
		Mass-production chip	Evaluation chip	
Notes for option	Ports C, D output level at reset mode	Ports C, D can be brought to "H" or "L" in a group of 4 bits.	Port C and port D can be brought to "H" or "L" by CHL pin and DHL pin, respectively.	CHL pin and DHL pin must be set according to option specified for mass-production chip.
	Watchdog reset function	The presence or absence of time base timer-used watchdog reset function can be selected.	Whether or not to perform watchdog reset function with WDC pin can be determined.	WDC pin must be set according to option specified for mass-production chip.
	Port output configuration PU/OD	PU or OD can be selected in bit units.	Only Nch OD configuration without pull-up resistance	(LC6593-applied evaluation) External resistor (10kohms) on evaluation chip board must be connected to necessary port. (LC65PG38D-applied evaluation) Resistor must be connected to necessary port on applilcation board.
	PU resistor configuration	PU resistor brought to Hi-Z at "L" output mode (Pch Tr is turned OFF)	PU resistor, being external resistor, whose impedance remains unchanged at "L" output mode.	For mass-production chip, leakage current only flows in Pch Tr at "L" output mode; for evaluation chip, current continues flowing in PU resistor at "L" output mode.
	Port output configuration PD/OD	PD or OD can be selected in bit units.	Only Pch OD configuration without pull-down resistance.	(LC6593-applied evaluation) External resistor (100kohms) on evaluation chip board must be connected to necessary port. (LC65PG38D-applied evaluation) Resistor must be connected to necessary port on application board. Load power supply must be also supplied on application board side.
Notes for OSC	Constants for main clock	(Crystal OSC), (Ceramic resonator OSC) Catalog-guaranteed constants provide OSC at frequency specified in catalog.	(Crystal OSC), (Ceramic resonator OSC) Different from mass-production chip in circuit design and characteristic. OSC may be made unstable by wiring capacitance.	(Crystal OSC), (Ceramic resonator OSC) External constants must be fine-adjusted according to service conditions. Refer to note given below.
	Constants for sub-clock	(Crystal OSC) Catalog-guaranteed constants provide OSC at frequency specified in catalog.	(Crystal OSC) Different from mass-production chip in circuit design and characteristic. OSC may be made unstable by wiring capacitance.	(Crystal OSC) External conostants must be fine-adjusted according to service conditions. Refer to note given below.
Notes for electrical characteristics	OSC frequency for main clock, sub-clock	OSC frequency characteristic as indicated in catalog	Different from mass-production chip in circuit design and characteristic.	ES, CS must be used to evaluate characteristic in detail.
	Operating current, standby current	Current characteristic as indicated in catalog	Different from mass-production chip in circuit design and characteristic.	Standby current cannot be evaluated in detail. However, standby current can be confirmed roughly in the manner shown below. Be sure to confirm standby current. ES, CS must be used to evaluate characteristic in detail.
	Operating voltage	Supply voltage range as indicated in catalog	Restricted to the operating range of EPROM, other LSI	Evaluation chip must be also used at V_{DD} = 5V±5% at which EPROM, other LSI are used. Therefore, V_{DD} = 5V±5% only can be used for evaluation of mass-production microcomputers.
	Operating temperature	Temperature range as indicated in catalog	Guaranteed temperature range: 10°C to 40°C	LC6593 and LC65PG38D must be used at 10°C to 40°C for evaluation.

< Confirmation methods for the standby function >

The standby current at the standby mode of the evaluation chip can be evaluated not exactly but approximately. Then, do the following steps.

(a) Confirmation of the standby state
Be sure to confirm whether or not the LSI enters the standby mode when the standby conditions are satisfied.
The following Table gives the current dissipation (typ.) at each mode as a guideline for confirmation of mode.

Mode	Main clock (4.19MHz)	Sub-clock (32kHz)	Current dissipation (typ.)
NORMAL, main clock 1/1 mode	OSC	OSC	Approx. 3.5mA to 3.7mA
NORMAL, main clock 1/2 mode	OSC	OSC	Approx. 2.3mA to 2.5mA
NORMAL, main clock 1/32 mode	OSC	OSC	Approx. 1mA to 1.2mA
NORMAL, sub-clock mode	OSC	OSC	
NORMAL, sub-clock mode	Stop	OSC	Approx. 100μA to 300μA
HALT, main clock 1/1 mode	OSC	OSC	Approx. 1mA
HALT, main clock 1/2 mode	OSC	OSC	
HALT, main clock 1/32 mode	OSC	OSC	
HALT, sub-clock mode	OSC	OSC	
HALT, sub-clock mode	Stop	OSC	Approx. 50μA
HOLD mode	Stop	Stop	Several nA to 300nA

Note 1) The current dissipation values shown above are the values obtained when a separate power supply is used for the EPROM power supply.
2) The current dissipation values shown above are the values obtained when the WDC, CHL, DHL pins are brought to "L" level.
When brought to "H" level, the current dissipation value per pin increases by approximately 30μA.
3) The current dissipation at the NORMAL mode varies by the value of current dissipated in the pull-up resistor of IM0 to IM7.
IM0 to IM7: The current dissipation per bit at "L" level increases by approximately 25μA.
4) The current dissipation values at the HALT or HOLD mode are the values obtained when the EPROM is removed.
5) All other pins for the evaluation chip are left open.

(b) Confirmation by the load current
Your program must be designed so that the current is not transmitted to the input/output ports prior to the execution of the HALT instruction. This can reduce the useless dissipation of the load current at the standby mode and be confirmed on an oscilloscope.
1) Design your program so that the current is not transmitted to the output ports prior to the execution of the HALT instruction.
2) Design your program and peripherals so that the input/output ports are not brought to the floating state (Hi-Z) at the standby mode.
If brought to the floating state (Hi-Z), current flows in the microcomputer input circuit section, causing more current dissipation. Therefore, the backup enable time is shortened extremely in applications where the capacitor backup is used.

< OSC constants when the EVA800-TB6538 is used >

When developing your program using evaluation chip board EVA800-TB6538, adjust the capacitor value according to the stray capacitance of the circuit because the crystal/ceramic resonator OSC constants for main clock and the crystal OSC constants for sub-clock depend on the conditions for evaluation and the cable length, etc.

LC6538D INSTRUCTION SET (by function)

Symbol	Description
AC	: Accumulator
ACt	: Accumulator bit t
CF	: Carry flag
CTL	: Control register
MSTEN	: Master interrupt enable flag
DP	: Data pointer
E	: E register
bFn	: Flag bit n
M1	: Memory 1
M2	: Memory 2
M1(DP)	: Memory 1 addressed by DP
M2(DP)	: Memory 2 addressed by DP
P(DPL)	: Input/output port addressed by DPL
GP(DP)	: Pseudo port specified by DP
PC	: Program counter
STACK	: Stack register
TM0	: Timer 0
TM0F	: Timer 0 interrupt request flag
bAt,bHa,bLa	: Working register
ZF	: Zero flag

( ) [ ]	: Contents
←	: Transfer and direction
+	: Addition
−	: Subtraction
∧	: AND
∨	: OR
∨	: Exclusive OR

Instruction group	Mnemonic		Instruction code $D_7D_6D_5D_4$	Instruction code $D_3D_2D_1D_0$	Bytes	Cycles	Function	Description	Status flag affected	Remarks
Accumulator manipulation instructions	CLA	Clear AC	1 1 0 0	0 0 0 0	1	1	AC ← 0	The AC contents are cleared.	ZF	* 1
	CLC	Clear CF	1 1 1 0	0 0 0 1	1	1	CF ← 0	The CF contents are cleared.	CF	
	STC	Set CF	1 1 1 1	0 0 0 1	1	1	CF ← 1	The CF is set.	CF	
	CMA	Complement AC	1 1 1 0	1 0 1 1	1	1	AC ← $\overline{(AC)}$	The AC contents are complemented.	ZF	
	INC	Increment AC	0 0 0 0	1 1 1 0	1	1	AC ← (AC) + 1	The AC contents are incremented +1.	ZF CF	
	DEC	Decrement AC	0 0 0 0	1 1 1 1	1	1	AC ← (AC) − 1	The AC contents are decremented −1.	ZF CF	
	RAL	Rotate AC left through CF	0 0 0 0	0 0 0 1	1	1	AC_0 ← (CF), AC_{n+1} ← AC_n, CF ← (AC_3)	The AC contents are shifted left through the CF.	ZF CF	
	TAE	Transfer AC to E	0 0 0 0	0 0 1 1	1	1	E ← (AC)	The AC contents are transferred to the E.		
	XAE	Exchange AC with E	0 0 0 0	1 1 0 1	1	1	(AC) ⇆ (E)	The AC contents and the E conents are exchanged.		
Memory manipulation instructions	INM	Increment M1	0 0 1 0	1 1 1 0	1	1	M1(DP) ← [M1(DP)]+1	The M1(DP) contents are incremented +1.	ZF CF	
	DEM	Decrement M1	0 0 1 0	1 1 1 1	1	1	M1(DP) ← [M1(DP)]−1	The M1(DP) contents are decremented −1.	ZF CF	
	SMB bit	Set M1 data bit	0 0 0 0	1 0 B_1B_0	1	1	M1(DP, B_1B_0)←1	A single bit of the M1(DP) specified with B_1B_0 is set.		
	RMB bit	Reset M1 data bit	0 0 1 0	1 0 B_1B_0	1	1	M1 (DP,B_1B_0)←0	A single bit of the M1(DP) specified with B_1B_0 is reset.	ZF	
Arithmetic operation/comparison instructions	AD	Add M1 to AC	0 1 1 0	0 0 0 0	1	1	AC ← (AC)+[M1(DP)]	Binary addition of the AC contents and the M1(DP) contents is performed and the result is stored in the AC.	ZF CF	
	ADC	Add M1 to AC with CF	0 0 1 0	0 0 0 0	1	1	AC ← (AC)+[M1(DP)] +(CF)	Binary addition of the AC, CF contents and the M1 (DP) contents is performed and the result is stored in the AC.	ZF CF	
	DAA	Decimal adjust AC in addition	1 1 1 0	0 1 1 0	1	1	AC ← (AC) + 6	6 is added to the AC contents.	ZF	
	DAS	Decimal adjust AC in subtraction	1 1 1 0	1 0 1 0	1	1	AC ← (AC) + 10	10 is added to the AC contents.	ZF	
	EXL	Exclusive OR M1 to AC	1 1 1 1	0 1 0 1	1	1	AC ← (AC) ∨ [M1(DP)]	The AC contents and the M1(DP) contents are exclusive-ORed and the result is stored in the AC.	ZF	
	AND	AND M1 to AC	1 1 1 0	0 1 1 1	1	1	AC ← (AC) ∧ [M1(DP)]	The AC contents and the M1(DP) contents are ANDed and the result is stored in the AC.	ZF	
	OR	OR M1 to AC	1 1 1 0	0 1 0 1	1	1	AC ← (AC) ∨ [M1(DP)]	The AC contents and the M1(DP) contents are ORed and the result is stored in the AC.	ZF	
	CM	Compare AC with M1	1 1 1 1	1 0 1 1	1	1	$\overline{[M1(DP)]}$+(AC)+1	The AC contents and the M1(DP) contents are compared and the CF and ZF are set/reset.	ZF CF	
	CI data	Compare AC with immediate data	0 0 1 0 0 1 0 0	1 1 0 0 $I_3I_2I_1I_0$	2	2	$\overline{I_3I_2I_1I_0}$ +(AC)+1	The AC contents and the immediate data $I_3I_2I_1I_0$ are compared and the ZF and CF are set/reset.	ZF CF	
	CLI data	Compare DP_L with immediate data	0 0 1 0 0 1 0 1	1 1 0 0 $I_3I_2I_1I_0$	2	2	$(DP_L) \vee I_3I_2I_1I_0$	The DP_L contents and the immediate data $I_3I_2I_1I_0$ are compared.	ZF	
Load/store instructions	LI data	Load AC with immediate data	1 1 0 0	$I_3I_2I_1I_0$	1	1	AC ← $I_3I_2I_1I_0$	The immediate data $I_3I_2I_1I_0$ is loaded in the AC.	ZF	* 1
	S	Store AC to M1	0 0 0 0	0 0 1 0	1	1	M1(DP) ← (AC)	The AC contents are stored in the M1(DP).		
	L	Load AC from M1	0 0 1 0	0 0 0 1	1	1	AC ← [M1(DP)]	The M1(DP) contents are loaded in the AC.	ZF	
	XM data	Exchange AC with M1, then modify DP_H with immediate data	1 0 1 0	0 $M_2M_1M_0$	1	2	(AC) ⇆ [M1(DP)] DP_H ← $(DP_H) \vee 0M_2M_1M_0$	The AC contents and the M1(DP) contents are exchanged and then the DP_H contents are modified with the contents of $(DP_H) \vee 0M_2M_1M_0$.	ZF	The ZF is set/reset according to the result of $(DP_H) \vee 0M_2M_1M_0$
	X	Exchange AC with M1	1 0 1 0	0 0 0 0	1	2	(AC) ⇆ [M1(DP)]	The AC contents and the M1(DP) contents are exchanged.	ZF	The ZF is set/reset according to the DP_H contents at the time of instruction execution.
	XI	Exchange AC with M1, then increment DP_L	1 1 1 1	1 1 1 0	1	2	(AC) ⇆ [M1(DP)] DP_L ← $(DP_L) + 1$	The AC contents and the M1(DP) contents are exchanged and then the DP_L contents are incremented +1.	ZF	The ZF is set/reset according to the result of $(DP_L + 1)$.
	XD	Exchange AC with M1, then decrement DP_L	1 1 1 1	1 1 1 1	1	2	(AC) ⇆ [M1(DP)] DP_L ← $(DP_L) - 1$	The AC contents and the M1(DP) contents are exchanged and then the DP_L contents are decremented −1.	ZF	The ZF is set/reset according to the result of $(DP_L - 1)$

Comparison result	CF	ZF
[M1(DP)] > (AC)	0	0
[M1(DP)] = (AC)	1	1
[M1(DP)] < (AC)	1	0

Comparison result	CF	ZF
$I_3I_2I_1I_0$ > (AC)	0	0
$I_3I_2I_1I_0$ = (AC)	1	1
$I_3I_2I_1I_0$ < (AC)	1	0

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Instruction group	Mnemonic		Instruction code		Bytes	Cycles	Function	Description	Status flag affected	Remarks
			$D_7 D_6 D_5 D_4$	$D_3 D_2 D_1 D_0$						
	RTBL	Read table data from program ROM	0 1 1 0	0 0 1 1	1	2	AC E ← ROM (PCh E. ACl	The contents of ROM addressed by the PC whose low-order 8 bits are replaced with the E and AC contents are loaded in the AC and E.		
Data pointer manipulation instructions	LDZ data	Load DP_H with Zero and DP_L with immediate data respectively	1 0 0 0	$I_3 I_2 I_1 I_0$	1	1	$DP_H \leftarrow 0$ $DP_L \leftarrow I_3 I_2 I_1 I_0$	The DP_H and DP_L are loaded with 0 and the immediate data $I_3I_2I_1I_0$ respectively.		
	LHI data	Load DP_H with immediate data	0 1 0 0	$I_3 I_2 I_1 I_0$	1	1	$DP_H \leftarrow I_3 I_2 I_1 I_0$	The DP_H is loaded with the immediate data $I_3I_2I_1I_0$.		
	IND	Increment DP_L	1 1 1 0	1 1 1 0	1	1	$DP_L \leftarrow (DP_L)+1$	The DP_L contents are incremented +1.	ZF	
	DED	Decrement DP_L	1 1 1 0	1 1 1 1	1	1	$DP_L \leftarrow (DP_L)-1$	The DP_L contents are decremented −1.	ZF	
	TAL	Transfer AC to DP_L	1 1 1 1	0 1 1 1	1	1	$DP_L \leftarrow (AC)$	The AC contents are transferred to the DP_L		
	TLA	Transfer DP_L to AC	1 1 1 0	1 0 0 1	1	1	$AC \leftarrow (DP_L)$	The DP_L contents are transferred to the AC	ZF	
	XAH	Exchange AC with DP_H	0 0 1 0	0 0 1 1	1	1	$(AC) \rightleftarrows (DP_H)$	The AC contents and the DP_H contents are exchanged.		
Working register manipulation instructions	XAi XA0 XA1 XA2 XA3	Exchange AC with working register Ai	1 1 1 0	i to 0 0 0 0	1	1	$(AC) \rightleftarrows (bA0)$	The AC contents and the contents of working register Ai are exchanged. Ai is assigned one of bA0, bA1, bA2, bA3 according to i_1i_0 of specified register bank b.		
			1 1 1 0	0 1 0 0	1	1	$(AC) \rightleftarrows (bA1)$			
			1 1 1 0	1 0 0 0	1	1	$(AC) \rightleftarrows (bA2)$			
			1 1 1 0	1 1 0 0	1	1	$(AC) \rightleftarrows (bA3)$			
	XHa XH0 XH1	Exchange DP_H with working register Ha	1 1 1 1	a 0 0 0 0	1	1	$(DP_H) \rightleftarrows (bH0)$	The DP_H contents and the contents of working register Ha are exchanged. Ha is assigned either of bH0 or bH1 according to a of specified register bank b.		
			1 1 1 1	1 1 0 0	1	1	$(DP_H) \rightleftarrows (bH1)$			
	XLa XL0 XL1	Exchange DP_L with working register La	1 1 1 1	a 0 0 0 0	1	1	$(DP_L) \rightleftarrows (bL0)$	The DP_L contents and the contents of working register La are exchanged. La is assigned either of bL0 to bL1 according to a of specified register bank b.		
			1 1 1 1	0 1 0 0	1	1	$(DP_L) \rightleftarrows (bL1)$			
	SRBA	Set Register Bank Address	1 1 1 1	0 0 1 0	1	1	RBF ← i1i0 of SB	The bank value specified by the SB instruction is set in the register bank flag.		
Flag manipulation instructions	SFB flag	Set flag bit	0 1 0 1	$B_3 B_2 B_1 B_0$	1	1	$bF_n \leftarrow 1$	The flag specified with $B_3B_2B_1B_0$ of specified register bank b is set.		
	RFB flag	Reset flag bit	0 0 0 1	$B_3 B_2 B_1 B_0$	1	1	$bF_n \leftarrow 0$	The flag specified with $B_3B_2B_1B_0$ of specified register bank b is reset.	ZF	The flags are divided into 16 groups of OF0 to OF3, OF4 to OF7 -- -- , 3F8 to 3F11, 3F12 to 3F15. The ZF is set/reset according to the 4 bits including a single bit specified with immediate data $B_3B_2B_1B_0$.
Jump/subroutine instructions	JMP addr	Jump in the current bank	0 1 1 0 $P_7 P_6 P_5 P_4$	1 $P_{10}P_9P_8$ $P_3 P_2 P_1 P_0$	2	2	$PC \leftarrow PC_{12} PC_{11}$ (or $\overline{PC_{11}}$) $P_{10}P_9P_8P_7P_6P_5$ $P_4P_3P_2P_1P_0$	A jump to the address specified with the $PC_{12}PC_{11}$ (or $\overline{PC_{11}}$) and immediate data $P_{10}P_9P_8P_7P_6P_5P_4P_3P_2P_1P_0$ occurs.		If the BANK and SB instructions are executed consecutively, the bank is changed.
	JPEA	Jump in the current page modified by E and AC	1 1 1 1	1 0 1 0	1	1	$PC_{7\sim0} \leftarrow (E.AC)$	A jump to the address specified with the contents of the PC whose low-order 8 bits are replaced by the E and AC contents occurs.		
	CZP addr	Call subroutine in the zero page	1 0 1 1	$P_3 P_2 P_1 P_0$	1	1	STACK ← (PC)+1 PC_{12-6}, $PC_{1\sim0} \leftarrow 0$ $PC_{5\sim2} \leftarrow P_3P_2P_1P_0$	A subroutine in page 0 of bank 0 is called.		
	CAL addr	Call subroutine in the zero bank	1 0 1 0 $P_7 P_6 P_5 P_4$	1 $P_{10}P_9P_8$ $P_3 P_2 P_1 P_0$	2	2	STACK ← (PC)+2 $PC_{12\sim0} \leftarrow 00P_{10}P_9P_8$ $P_7P_6P_5P_4P_3P_2P_1P_0$	A subroutine in bank 0 is called.		
	RT	Return from subroutine	0 1 1 0	0 0 1 0	1	1	PC ← (STACK)	A return from a subroutine occurs.		
	RTI	Return from interrupt routine	0 0 1 0	0 0 1 0	1	1	PC ← (STACK) CF ZF ← CSF. ZSF	A return from an interrupt service routine occurs.	ZF CF	
	BANK	Change bank	1 1 1 1	1 1 0 1	1	1	$PC_{11} \leftarrow (\overline{PC_{11}})$ GP(DP) M2(DP)	The bank of ROM is specified. The pseudo port is specified. The RAM2 is specified.		
	SB	Set bank	0 1 1 0	0 1 i1 i0	1	1	PC_{12} $PC_{11} \leftarrow i_1, i_0$ RBF ← i1i0	The bank of ROM is specified. The bank of working register, flag is specified.		

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Instruction group	Mnemonic		Instruction code $O_7 D_6 D_5 D_4$	Instruction code $D_3 D_2 D_1 D_0$	Bytes	Cycles	Function	Description	Status flag affected	Remarks
Branch instructions	BAt addr	Branch on AC bit	0 1 1 1 $P_7 P_6 P_5 P_4$	0 0 $t_1 t_0$ $P_3 P_2 P_1 P_0$	2	2	$PC_{7\sim0} \leftarrow P_7 P_6 P_5 P_4 P_3 P_2 P_1 P_0$ if ACt = 1	If a single bit of the AC specified with the immediate data $t_1 t_0$ is 1, a branch to the address specified with the immediate data $P_7P_6P_5P_4P_3P_2P_1P_0$ within the same page occurs.		Mnemonic is BA0 to BA3 according to the value of t.
	BNAt addr	Branch on no AC bit	0 0 1 1 $P_7 P_6 P_5 P_4$	0 0 $t_1 t_0$ $P_3 P_2 P_1 P_0$	2	2	$PC_{7\sim0} \leftarrow P_7 P_6 P_5 P_4 P_3 P_2 P_1 P_0$ if ACt = 0	If a single bit of the AC specified with the immediate data $t_1 t_0$ is 0, a branch to the address specified with the immediate data $P_7P_6P_5P_4P_3P_2P_1P_0$ within the same page occurs.		Mnemonic is BNA0 to BNA3 according to the value of t.
	BMt addr	Branch on M1 bit	0 1 1 1 $P_7 P_6 P_5 P_4$	0 1 $t_1 t_0$ $P_3 P_2 P_1 P_0$	2	2	$PC_{7\sim0} \leftarrow P_7 P_6 P_5 P_4 P_3 P_2 P_1 P_0$ if [M1(DP, $t_1 t_0$)] = 1	If a single bit of the M1(DP) specified with the immediate data $t_1 t_0$ is 1, a branch to the address specified with the immediate data $P_7P_6P_5P_4P_3P_2P_1P_0$ within the same page occurs.		Mnemonic is BM0 to BM3 according to the value of t.
	BNMt addr	Branch on no M1 bit	0 0 1 1 $P_7 P_6 P_5 P_4$	0 1 $t_1 t_0$ $P_3 P_2 P_1 P_0$	2	2	$PC_{7\sim0} \leftarrow P_7 P_6 P_5 P_4 P_3 P_2 P_1 P_0$ if [M1(DP, $t_1 t_0$)] = 0	If a single bit of the M1(DP) specified with the immediate data $t_1 t_0$ is 0, a branch to the address specified with the immediate data $P_7P_6P_5P_4P_3P_2P_1P_0$ within the same page occurs.		Mnemonic is BNM0 to BNM3 according to the value of t.
	BPt addr	Branch on Port bit	0 1 1 1 $P_7 P_6 P_5 P_4$	1 0 $t_1 t_0$ $P_3 P_2 P_1 P_0$	2	2	$PC_{7\sim0} \leftarrow P_7 P_6 P_5 P_4 P_3 P_2 P_1 P_0$ if [P(DP_L $t_1 t_0$)] = 1	If a single bit of port P(DP_L) specified with the immediate data $t_1 t_0$ is 1, a branch to the address specified with the immediate data $P_7P_6P_5P_4P_3P_2P_1P_0$ within the same page occurs.		Mnemonic is BP0 to BP3 according to the value of t.
	BNPt addr	Branch on no Port bit	0 0 1 1 $P_7 P_6 P_5 P_4$	1 0 $t_1 t_0$ $P_3 P_2 P_1 P_0$	2	2	$PC_{7\sim0} \leftarrow P_7 P_6 P_5 P_4 P_3 P_2 P_1 P_0$ if [P(DP_L, $t_1 t_0$)] = 0	If a single bit of port P(DP_L) specified with the immediate data $t_1 t_0$ is 0, a branch to the address specified with the immediate data $P_7P_6P_5P_4P_3P_2P_1P_0$ within the same page occurs.		Mnemonic is BNP0 to BNP3 according to the value of t.
	BC addr	Branch on CF	0 1 1 1 $P_7 P_6 P_5 P_4$	1 1 1 1 $P_3 P_2 P_1 P_0$	2	2	$PC_{7\sim0} \leftarrow P_7 P_6 P_5 P_4 P_3 P_2 P_1 P_0$ if CF = 1	If the CF is 1, a branch to the address specified with the immediate data $P_7P_6P_5P_4P_3P_2P_1P_0$ within the same page occurs.		
	BNC addr	Branch on no CF	0 0 1 1 $P_7 P_6 P_5 P_4$	1 1 1 1 $P_3 P_2 P_1 P_0$	2	2	$PC_{7\sim0} \leftarrow P_7 P_6 P_5 P_4 P_3 P_2 P_1 P_0$ if CF = 0	If the CF is 0, a branch to the address specified with the immediate data $P_7P_6P_5P_4P_3P_2P_1P_0$ within the same page occurs.		
	BZ addr	Branch on ZF	0 1 1 1 $P_7 P_6 P_5 P_4$	1 1 1 0 $P_3 P_2 P_1 P_0$	2	2	$PC_{7\sim0} \leftarrow P_7 P_6 P_5 P_4 P_3 P_2 P_1 P_0$ if ZF = 1	If the ZF is 1, a branch to the address specified with the immediate data $P_7P_6P_5P_4P_3P_2P_1P_0$ within the same page occurs.		
	BNZ addr	Branch on no ZF	0 0 1 1 $P_7 P_6 P_5 P_4$	1 1 1 0 $P_3 P_2 P_1 P_0$	2	2	$PC_{7\sim0} \leftarrow P_7 P_6 P_5 P_4 P_3 P_2 P_1 P_0$ if ZF = 0	If the ZF is 0, a branch to the address specified with the immediate data $P_7P_6P_5P_4P_3P_2P_1P_0$ within the same page occurs.		
	BFn addr	Branch on flag bit	1 1 0 1 $P_7 P_6 P_5 P_4$	$n_3 n_2 n_1 n_0$ $P_3 P_2 P_1 P_0$	2	2	$PC_{7\sim0} \leftarrow P_7 P_6 P_5 P_4 P_3 P_2 P_1 P_0$ if bFn = 1	If the immediate data $n_3n_2n_1n_0$ specified flag bit of the 16 flags of specified register bank b is 1, a branch to the address specified with immediate data $P_7P_6P_5P_4P_3P_2P_1P_0$ within the same page occurs.		Mnemonic is BF0 to BF15 according to the value of n.
	BNFn addr	Branch on no flag bit	1 0 0 1 $P_7 P_6 P_5 P_4$	$n_3 n_2 n_1 n_0$ $P_3 P_2 P_1 P_0$	2	2	$PC_{7\sim0} \leftarrow P_7 P_6 P_5 P_4 P_3 P_2 P_1 P_0$ if bFn = 0	If the immediate data $n_3n_2n_1n_0$ specified flag bit of the 16 flags of specified register bank b is 0, a branch to the address specified with immediate data $P_7P_6P_5P_4P_3P_2P_1P_0$ within the same page occurs.		Mnemonic is BNF0 to BNF15 according to the value of n.
Input/output instructions	IP	Input port to AC	0 0 0 0	1 1 0 0	1	1	AC ← [P(DPL)] or [GP(DP)] or [M2(DP)]	The contents of port P(DP_L) or pseudo port GP(DP) or RAM2 are loaded in the AC.	ZF	
	OP	Output AC to port	0 1 1 0	0 0 0 1	1	1	P(DPL) or GP(DP) or M2(DP) ← (AC)	The AC contents are output to port P(DP_L) or pseudo port GP(DP) or RAM2.		
	SPB bit	Set port bit	0 0 0 0	0 1 B_1 B_0	1	2	P(DPL, B_1B_0) or GP(DP, B_1B_0) or M2(DP, B_1B_2) ← 1	A single bit in port P(DP_L) or pseudo port GP(DP) or RAM2 specified with immediate data B_1B_0 is set.		When this instruction is executed, the E contents are destroyed.
	RPB bit	Reset port bit	0 0 1 0	0 1 B_1 B_0	1	2	P(DPL, B_1B_0) or GP(DP, B_1B_0) or M2(DP, B_1B_2) ← 0	A single bit in port P(DP_L) or pseudo port GP(DP) or RAM2 specified with immediate data B_1B_0 is reset.	ZF	When this instruction is executed, the E contents are destroyed.
Other instructions	SCTL bit	Set control register bit	0 0 1 0 1 0 0 0	1 1 0 0 B_3 B_2 B_1 B_0	2	2	CTL, $B_3B_2B_1B_0$ ← 1 or MSTEN ← 1	The immediate data $B_3B_2B_1B_0$-specified bits of the control register (individual interrupt enable flag) or the master interrupt enable flag is set.		*2
	RCTL bit	Reset control register bit	0 0 1 0 1 0 0 1	1 1 0 0 B_3 B_2 B_1 B_0	2	2	CTL, $B_3B_2B_1B_0$ ← 0 or MSTEN ← 0	The immediate data $B_3B_2B_1B_0$-specified bits of the control register (individual interrupt enable flag) or the master interrupt enable flag is reset.	ZF	*2
	WTTM	Write timer ← 0	1 1 1 1	1 0 0 1	1	1	TM0 ← (E), (AC) TMOF ← 0	The E and AC contents are loaded in the timer 0. The TMF is reset.	TMOF	
	HALT	Halt	1 1 1 1	0 1 1 0	1	1	Halt, Hold	The standby mode is entered.		
	NOP	No operation	0 0 0 0	0 0 0 0	1	1	No operation	No operation is performed, but 1 machine cycle is consumed.		

*1 If the CLA instruction is used consecutively in such a manner as CLA, CLA, ·····, the first CLA instruction only is effective and the following CLA instructions are changed to the NOP instructions. This is also true of the LI instruction.

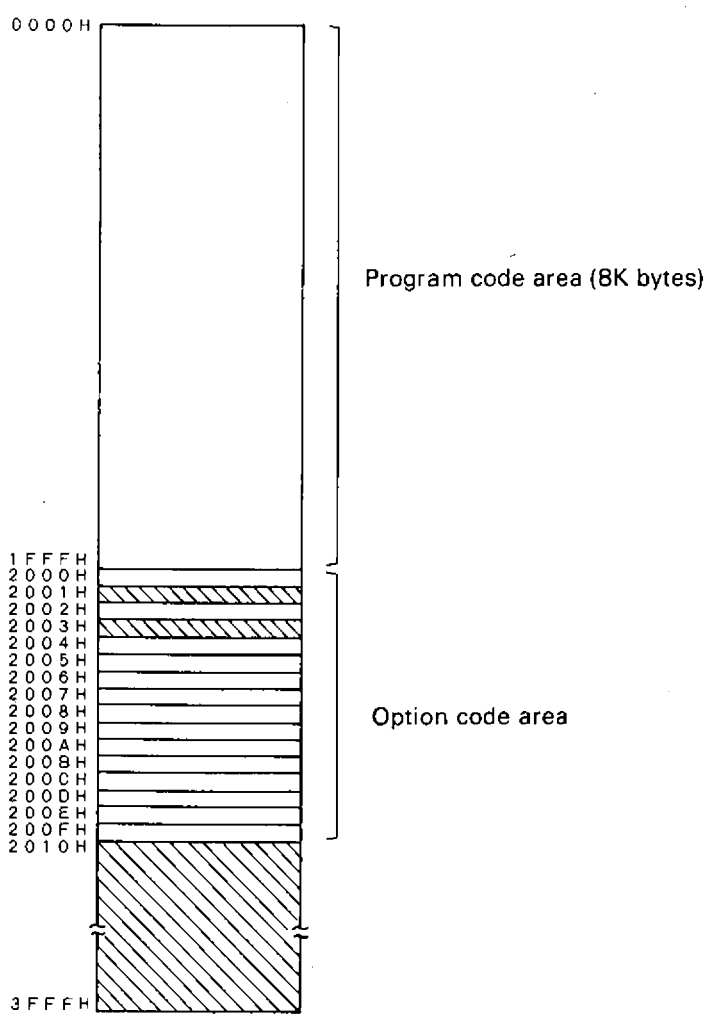
*2 $B_3B_2B_1B_0$ = 0000B to 1000B

LC6538D Option Code Specifying Method

General Description

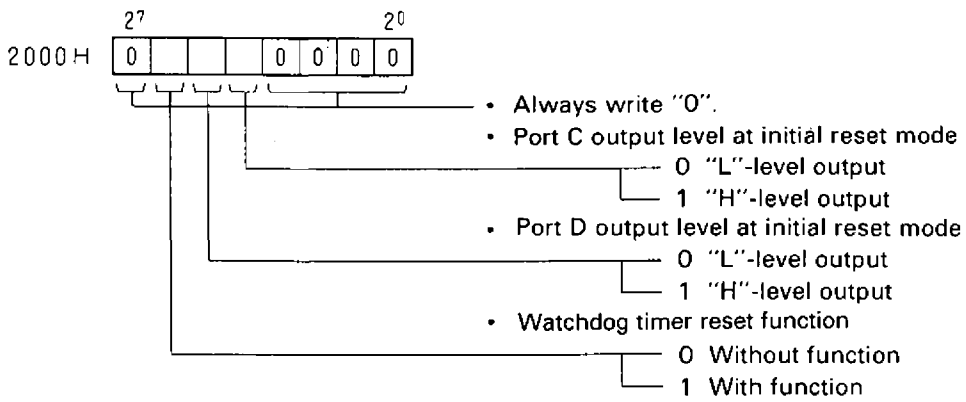
It is requested that you should submit to us various mask options of the LC6538D together with the program code which are stored in an EPROM.
By using our cross assembler for the LC6538D, the option code can be specified interactively and stored in the EPROM.
If our cross assembler is not used, specify the option code as shown below. (This is the same as the method where the cross assembler is created.)
The Type No. of the EPROM to be submitted is 27128.

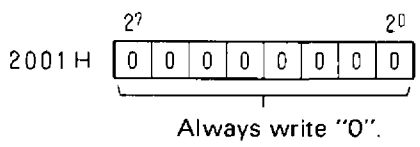
EPROM address map

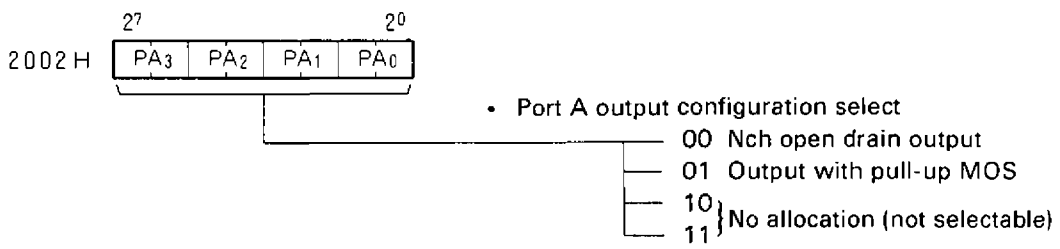


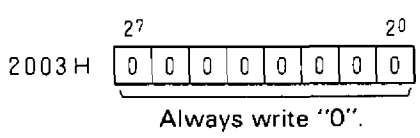
Always write "00" in this shaded area.

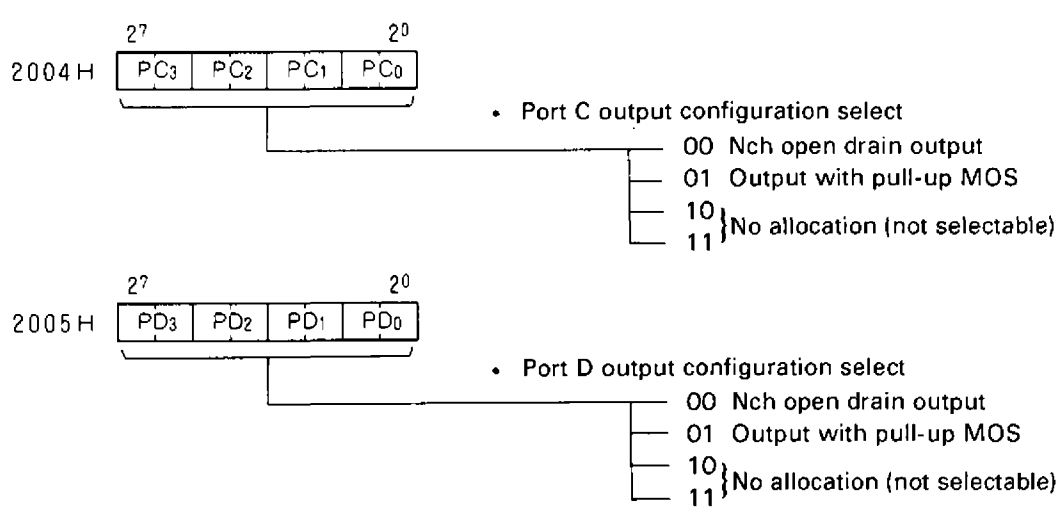
Option Code Contents











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2006H

2^7				2^0
0	0	PE_2	PE_1	PE_0

Always write "0".

- Port E output configuration select
  - 00 Nch open drain output
  - 01 Output with pull-up MOS
  - 10, 11 } No allocation (not selectable)

2007H

2^7			2^0
PF_3	PF_2	PF_1	PF_0

- Port F output configuration select
  - 00 Nch open drain output
  - 01 Output with pull-up MOS
  - 10, 11 } No allocation (not selectable)

2008H

2^7			2^0
PG_3	PG_2	PG_1	PG_0

- Port G output configuration select
  - 00 Nch open drain output
  - 01 Output with pull-up MOS
  - 10, 11 } No allocation (not selectable)

2009H

2^7			2^0
PH_3	PH_2	PH_1	PH_0

- Port H output configuration select
  - 00 Nch open drain output
  - 01 Output with pull-up MOS
  - 10, 11 } No allocation (not selectable)

200AH

2^7			2^0
T3	T2	T1	T0

- Digit-only pin output configuration select — (1)
  - 00 Pch open drain output
  - 01 No allocation (not selectable)
  - 10 Output with pull-down resistance
  - 11 No allocation (not selectable)

200BH

2^7			2^0
T7	T6	T5	T4

- Digit-only pin output configuration select — (2)
  - 00 Pch open drain output
  - 01 No allocation (not selectable)
  - 10 Output with pull-down resistance
  - 11 No allocation (not selectable)

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200CH

2^7			2^0
T11	T10	T9	T8

- Digit-only pin output configuration select — (3)
  - 00 Pch open drain output
  - 01 No allocation (not selectable)
  - 10 Output with pull-down resistance
  - 11 No allocation (not selectable)

200DH

2^7			2^0
T15/S8	T14/S9	T13/S10	T12/S11

- Digit/segment common pin output configuration select
  - 00 Pch open drain output
  - 01 No allocation (not selectable)
  - 10 Output with pull-down resistance
  - 11 No allocation (not selectable)

200EH

2^7			2^0
S3	S2	S1	S0

- Segment-only pin output configuration select — (1)
  - 00 Pch open drain output
  - 01 No allocation (not selectable)
  - 10 Output with pull-down resistance
  - 11 No allocation (not selectable)

200FH

2^7			2^0
S7	S6	S5	S4

- Segment-only pin output configuration select — (2)
  - 00 Pch open drain output
  - 01 No allocation (not selectable)
  - 10 Output with pull-down resistance
  - 11 No allocation (not selectable)

Notes on Programming

- In this section, we shall describe the notes on developing programs for the LC6538D microcomputer.

<table>
<tr><th colspan="2">Item</th><th>Function</th><th>Notes</th></tr>
<tr><td rowspan="4">System clock</td><td>System clock mode</td><td>One of the following clock sources can be selected on your program as the system clock source for the LC6538D microcomputer.
① Main clock 1/1 mode (T_{CYC}=0.95μs)
② Main clock 1/2 mode (T_{CYC}=1.9μs)
③ Main clock 1/32 mode (T_{CYC}=30.5μs)
④ Sub-clock mode (T_{CYC}=61μs)
(Note) Main clock: 4.194304MHz
Sub-clock: 32.768kHz</td><td>● The main clock must be supplied at the system start-up.
● The sub-clock must be supplied when your application is designed to use the sub-clock mode.</td></tr>
<tr><td>System clock select</td><td>The system clock source can be selected by setting data in the clock mode flag (CMF: 2 bits) of the system clock control register.
<table><tr><th>CMF</th><th>Mode</th></tr><tr><td>0</td><td>Main clock 1/32 mode (at the reset)</td></tr><tr><td>1</td><td>Main clock 1/1 mode</td></tr><tr><td>2</td><td>Main clock 1/2 mode</td></tr><tr><td>3</td><td>Sub-clock mode</td></tr></table></td><td>● System clock modes can be changed only when the main clock oscillation is stable or the clock signals are sent from external clock with the 4MSTPF flag set to "0".
● The clock mode newly selected by the CMF flag is actually activated up to 64/f_{OSC} cycles later after data is set in that flag. To change high-speed mode to low-speed mode and then start the standby mode, execute the HALT instruction after the buffer time elapses.
● Clock modes should be changed, with supplied voltage at 4.0V or greater.</td></tr>
<tr><td>Main clock oscillation halt/start</td><td>The main clock operation (halt/start) can be controlled by setting data in the 4MSTPF flag of the system clock control register.
<table><tr><th>4MSTPF</th><th>Main clock</th></tr><tr><td>0</td><td>Start (at the reset)</td></tr><tr><td>1</td><td>Halt</td></tr></table></td><td>● If one of the main clock modes is selected as the system clock source, you must not set the 4MSTPF flag to "1".
● Set the 4MSTPF flag to "1" after the sub-clock mode becomes actually activated. That is, you have to set the flag to "1" after the sub-clock mode is specified by the flag data and then becomes activated after the buffer time elapses.
● To change the main clock halt state at the sub-clock mode to one of the main clock modes, set the 4MSTPF flag to "0" and wait at least until the main clock oscillation becomes stable. Wait for t_{MXS} or M_{CFS} cycles.</td></tr>
<tr><td>Low-speed operation mode</td><td>The following blocks are forced to stop their functions when the low-speed operation mode (main clock 1/32 mode or sub-clock mode) is selected.
<table><tr><th>Item</th><th>Contents</th></tr><tr><td>Port B (comparator input)</td><td>If data is input to the accumulator (AC) from port B, 0 (zero) is input to the AC.</td></tr><tr><td>H counter</td><td>The contents of the H counter are cleared.</td></tr><tr><td>Display controller</td><td>Not to support dynamic display mode operation</td></tr></table></td><td>● Do not use the blocks at the left column during the low-speed operation mode.
● Note that the low-speed operation is selected at the system reset.</td></tr>
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	Item	Function	Notes
Standby mode	HALT mode activation/release	(Activation) The HALT mode can be activated by executing the HALT instruction when the SLPF flag of the standby control register has been already set to "0". However, the HALT instruction will be processed equally as the NOP instruction when the following HALT mode release conditions are satisfied. (Release) ① Reset ② The PE2/START pin signal level is "H" with the WG2=1. ③ The interrupt release signal is delivered with the WG3=1. ④ The overflow signal is generated by the time base timer circuit.	● If you want to release the HALT mode by using the PE_2/START pin "H" level signal or interrupt release signal, set the WG2 or WG3 flag prior to the execution of the HALT instruction.
	HOLD mode activation/release	(Activation) The HOLD mode can be selected by executing the HALT instruction with the SLPF="1". (Release) Reset	● The HOLD mode can be released only by the reset signal. ● Execute a single NOP instruction prior to the execution of the HALT instruction for activating the HOLD mode. ● Never output logic "1" to bit 1 of the standby control register (STBC).
	Watchdog timer reset (effective only if the watchdog timer function has been selected by option)	The time base timer can be used to detect runaway and cause watchdog reset to occur.	● You have to create a routine which allows the TBF flag to be reset every program-defined time cycle (0.5sec. max.). ● The clock which has been already in operation must be selected as the time base timer source. ● If the time base interrupt request flag (TBF) is set to "1" prior to HALT activation, the HALT mode release signal triggered by time base overflow signal and watchdog reset signal are to be generated at the same time. To avoid the generation of watchdog reset signal in the above case, there are two methods as follows: ① Reset the TBF flag immediately before the HALT instruction is executed. or ② Set the time base interrupt enable flag (TBEN) and HALT release enable flag (WG3) before the HALT instruction is executed.
Interrupt	Interrupt enable flag (Control register: 8 bits)	● There are 8 interrupt enable flags, which are assigned to 8 interrupt sources. These flags are set to enable interrupt requests by SCTL0 to SCTL7 instructions. Note that two or more flags cannot be set at a time. ● All the interrupt enable flags are set to disable interrupt at the reset mode.	● The interrupt enable flags are not reset after interrupt processing is carried out. If you want to reset interrupt enable flag, you have to use the RCTL instruction. ● All the interrupt enable flags are reset when the HOLD mode is started up. You have to set necessary flags after the HOLD mode is released.

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Item			Function	Notes
Interrupt	Interrupt request flag		• There are 8 interrupt request flags, which are assigned to 8 interrupt sources. Four interrupt request flags are assigned as an interrupt extended register. That is, 8 interrupt request flags are assigned as two internal extended registers. Therefore, these registers can be accessed by executing the BANK and IP/OP instructions consecutively. If you input data to the accumulator (AC) from one of these registers, you can use the BANK and IP instructions consecutively. If you output data to one of these registers, you can use the BANK and OP instructions consecutively. However, you cannot set any bit of the internal extended register. If you are to reset some bits of the register, set data of 0 for them but 1 for other bits in the accumulator and output the data to interrupt request register by executing the BANK and OP instructions consecutively. • Flags other than timer 1 interrupt request flag (TM1F) are set to "0" at the reset mode. • The TM0F, SI00F, SI01F flags are reset at the time of WTTM instruction execution, SI00, SI01 data transfer start, respectively.	• These flags are not reset even after interrupt processing is carried out. Reset the interrupt source flag of a corresponding interrupt source factor when interrupt processing is performed. • All the flags are reset when the HOLD mode is started up. • The interrupt request register cannot be manipulated by the BANK + SPB/RPB instructions.
Notes on use of common ports	Port E	PE_0/V_{REF0} PE_1/V_{REF1}	Port E_0 and E_1 can be also used as the external reference voltage input pins V_{REF0} and V_{REF1} for comparator input (port B).	• If you want to use these pins as V_{REF0}, V_{REF1}, and START, you have to output logic "1" to the PE_0, PE_1, and PE_2. (At the reset mode, the PE_0 to PE_2 pins are all set to "1".)
		PE_2/START	Port E_2 can be also used as the HALT mode control pin START.	
	Port F	PF_0/SI_0 $PF_1/SO0$ $PF_2/\overline{SCK0}$	Port F_0 and F_1, and F_2 can be also used as the SI0, SO0, and $\overline{SCK0}$ pins for serial data transfer 0.	• If you want to use these pins as SI0, SO0, $\overline{SCK0}$, and INT0, you have to output logic "1" to the PF_0, PF_1, PF_2, and PF_3. (At the reset mode, the PF_0 to PF_3 pins are all set to "1".)
		PF_3/INT0	Port F_3 can be also used as the INT0 pin for external interrupt 0 input.	
	Port G	$PG_0/SI1$ $PG_1/SO1$ $PG_2/\overline{SCK1}$	Port G_0, G_1, and G_2 can be also used as the SI1, SO1, and $\overline{SCK1}$ pins for serial data transfer 1.	• If you want to use these pins as SI1, SO1, $\overline{SCK1}$, and $\overline{INT1}$, you have to output logic "1" to the PG_0, PG_1, PG_2, and PG_3. (At the reset mode, the PG0 to PG3 pins are all set to "1".)
		$PG_3/\overline{INT1}$	Port G_3 can be also used as the $\overline{INT1}$ pin for external interrupt 1 input.	
	Port H	$PH_0/\overline{DAC0}$ $PH_1/\overline{DAC1}$	• Port H_0 and H_1 can be also used as the $\overline{DAC0}$ and $\overline{DAC1}$ pins for PWM type DAC output.	• If you want to use these pins as $\overline{DAC0}$, $\overline{CAC1}$, and SQR pins, you have to output logic "0" to the PH_0, PH_1, and PH_2. (At the reset mode, the PH_0, PH_1, and PH_2 pins are all set to "1".)
		PH_2/SQR	• Port H_2 can be also used as the SQR pin for burst pulse signal output.	
		PH_3/HCNT	• Port H_3 can be also used as the HCNT pin for horizontal sync signal input.	• If you want to use these pins as HCNT, you have to output logic "1" to the PH_3. (At the reset mode, the PH_3 pin is set to "1".)

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Item		Function		Notes
Display controller	Operational status at system clock selection	When the CPU has entered low-speed operation mode (main clock 1/32 mode or sub-clock mode), dynamic display mode operation is not successfully carried out.		● When low-speed operation mode is employed, do not select the dynamic display mode.
	Operational status at standby mode	Dynamic display mode	● Segment output pin----"H"-level output at all the pins ● Digit output pin----Unpredictable ● Fixed address output pin------Keeps old contents.	● Select display OFF mode prior to the standby mode activation so that no current is dissipated by FLT pin.
		Static display mode	● S0 to S7 pins---"H"-level output at all the pins ● T0 to T11 T12/S11 to T15/S8 pins------Keeps old contents.	
		Display OFF mode	● All FLT pins----"L"-level output at the all pins	