Ordering number: EN2058A

CMOS LSI

No.2058A

LC5812

4-Bit Microcomputer with Internal LCD Driver

The LC5812 series models are 4-bit, single-chip, high-performance microcomputers equipped with LCD drivers. They are produced by CMOS technology. Their numerous features include low-voltage operation and low current dissipation.

A 4 bit parallel-processing ALU, program memory (ROM), data memory (RAM), input and output ports, a timer, a clock generator, and LCD drivers, among other things, are integrated on a single chip.

A set of 134 instructions, including the operation and processing instructions executable in 4-bit units and various conditional branch instructions and LCD driver data transfer instructions form an easy-to-use and effective instruction system.

In HALT mode the user can readily implement the clock function during low-power dissipation. To minimize the current required, overall internal operation is stopped except for the oscillation and frequency divider circuits and the LCD drivers.

In HOLD mode the operation of the system clock oscillation is stopped so that the current dissipation becomes much less.

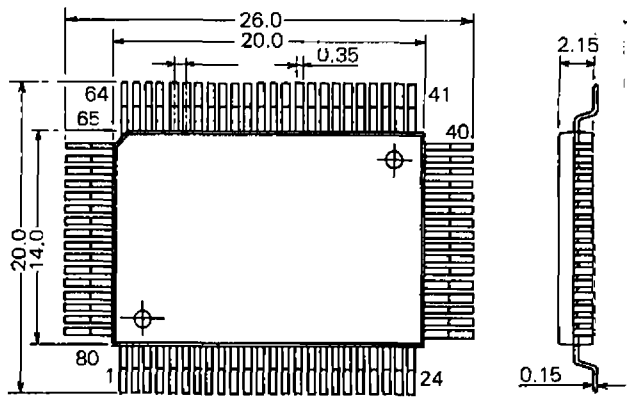
The LC5812 is very useful for controlling electronic tuners, cameras, and other portable devices at low voltage, with low power dissipation.

Features

- A wide supply voltage range

	Cycle time	Supply voltage range	Remarks
LC5812	122μs	V_{SS2} = −2.0 to −3.6V	32k crystal
LC5812H	122μs	V_{SS2} = −2.0 to −5.0V	32k crystal
	61μs	V_{SS2} = −2.3 to −5.0V	65k crystal
	40μs	V_{SS2} = −3.5 to −5.0V	400k ceramic resonator
	20μs	V_{SS2} = −4.5 to −5.0V	800k ceramic resonator

Package Dimensions 3044B
(unit: mm)



SANYO : QIP80A

SANYO Electric Co.,Ltd. Semiconductor Business Headquarters
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110 JAPAN

○ Micro-level operating current
Only micro-level current is needed to operate the equipment if the HALT function is used efficiently. Although the exact current dissipation depends on the oscillation frequency (and the oscillator) and the program structure, a typical current requirement is about 5μA to run the clock program if the optimum technique is used to design the program.

○ Enhanced HALT/HOLD release and interrupt functions
- Five types of HALT/HOLD release functions and five types of interrupt functions
- External interrupt function (included in the above 5 interrupt functions)
- Up to 8 levels of subroutine nesting (common with interrupts)

○ Enhanced hardware for greater processing capability
- Built-in segment PLA circuit: Is able to join the LCD driver outputs to any patterns on the LCD panel without software.
- Built-in decimal up/down counter
- Built-in 8-bit programmable timer
- The entire RAM area can be used as a working area (bank switching).
- Built-in data pointer
- All instructions per step operation
- Built-in clock oscillator and frequency divider circuit

○ Various LCD output terminals for LCD panel drive (42 terminals)

LCD panel		Number of LCD segments
1/3 bias	1/3 duty	126 segments (max.)
1/2 bias	1/3 duty	126 segments (max.)
1/2 bias	1/2 duty	84 segments (max.)
Static		42 segments (max.)

○ The LCD panel drive output terminal can be switched to the general-purpose output terminal.

○ A number of input and output terminals are provided.

Input dedicated port:	2 ports/8 pins
Input/output port:	2 ports/8 pins
Output dedicated port:	1 port/4 pins

○ An initial reset terminal is provided.

○ Built-in oscillation circuit for system clock
Two kinds of oscillation circuits are available: one for the system clock and the other for clock oscillation.

○ Number of instructions: 134

○ ROM: 2,048 x 16 bits

○ RAM. 152 x 4 bits

○ Form of shipment: QIP80 (or chip)

Application Development Support System

An evaluation chip (LC5897) and special devices for the application development tool will be provided.

- ○ SDS410 system

  Enables the user to create an application development program in assembler language (edit-assembling).

- ○ EVA510 + TB5812 + DCB1 + Application Evaluation Board + LC5897

  Modification and debugging of the application development program are possible by connecting to the SDS410.
  The EVA510 is identical with the EVA410 except that the control ROM has been replaced.

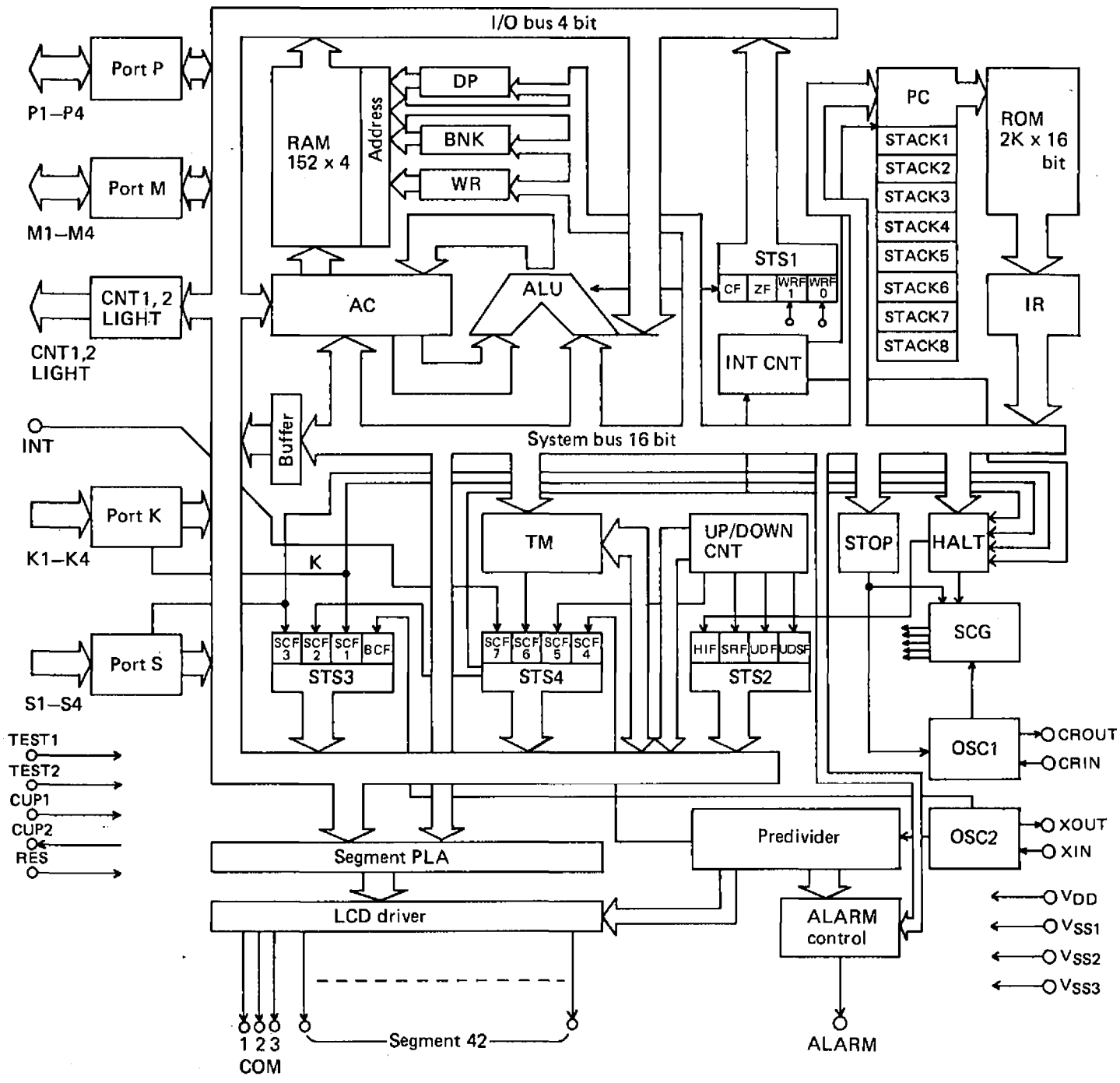
- ○ TB5812 + DCB1 + Application Evaluation Board + LC5897

  Load and evaluation is possible using the EPROM (2732) in which the data for the application development program is contained.

Note) The application evaluation board is created by the user.
Either LEDs or on LCD can be used as the display element.

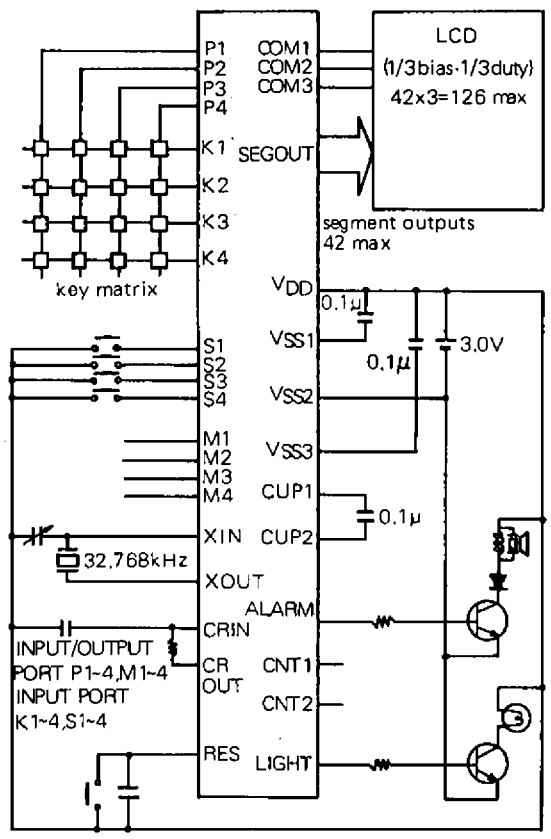
Application Examples

- ○ Portable equipment (camera control, various card controls, high-quality electric calculators and timers)
- ○ Acoustic equipment (electronic control, electronic tuning, and clocks)
- ○ Household electrical apparatus (remote control, and timer control)
- ○ Telephone equipment (telephone control, and display control)



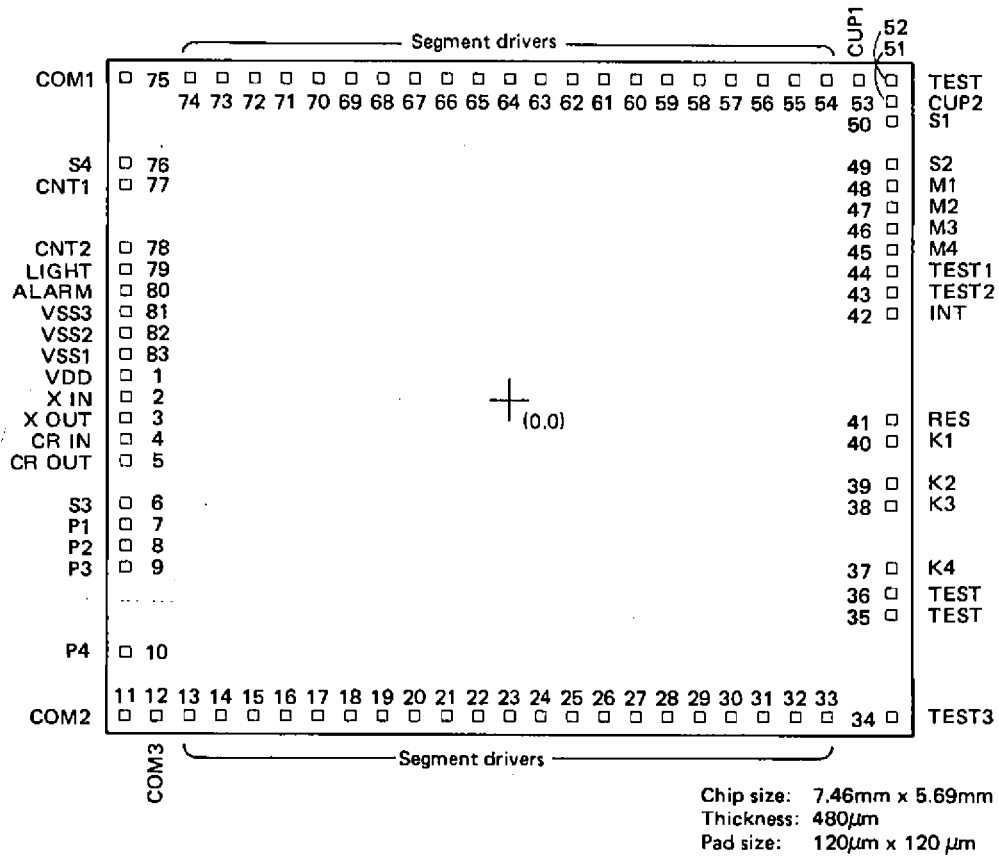
DP:	Data pointer	STS3.	Status register 3
BNK:	Bank register	STS4:	Status register 4
WR:	Working register	CF:	Carry flag
AC:	Accumulator	ZF:	Zero flag
ALU:	Arithmetic and logical unit	WRF0:	Working flag 0
INT:	Interrupt control circuit	WRF1:	Working flag 1
PC:	Program counter	BCF:	Test flag
UP/DOWN CNT:	Decimal up/down counter	SCF1:	S port flag
		SCF2:	STS4 flag
		SCF3:	K port flag
TIM:	Preset timer	SCF4:	Divider overflow flag
IR:	Instruction register	SCF5:	UP/DOWN CNT overflow flag
STOP:	HOLD control circuit	SCF6:	Timer overflow flag
HALT.	HALT control circuit	SCF7:	INT signal change flag
SCG:	System clock generator	ICF:	Internal clock flag
STS1:	Status register 1		
STS2:	Status register 2		

Application Circuit — Example (1/3 bias — 1/3 duty)



Unit (capacitance: F)

Pad Arrangement of LSI Chip



Chip size: 7.46mm x 5.69mm
Thickness: 480μm
Pad size: 120μm x 120 μm

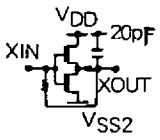
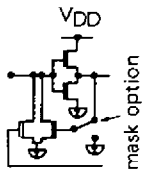
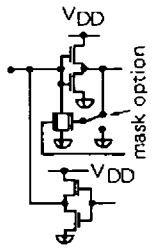
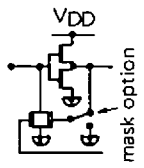
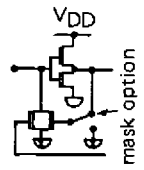
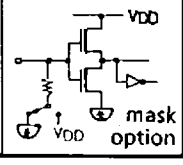
Pin Layout

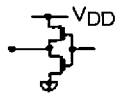
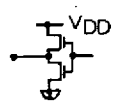
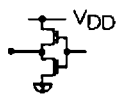
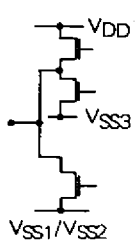
Pad name and coordinates

QIP80 pin arrangement				
	Pad No.	Pad name	X (um)	Y (um)
72	1	V_{DD}	−3581	+214
73	2	XIN	〃	+3
74	3	XOUT	〃	−176
75	4	CRIN	〃	−369
76	5	CROUT	〃	−549
77	6	S3	〃	−1048
78	7	P1	〃	−1228
79	8	P2	〃	−1408
80	9	P3	〃	−1588
1	10	P4	〃	−2380
2	11	COM2	〃	−2696
3	12	COM3	−3367	−2696
4	13	seg	−2823	〃
5	14	↑	−2528	〃
6	15	↑	−2233	〃
7	16	↑	−1938	〃
8	17	↑	−1643	〃
9	18	↑	−1347	〃
10	19	↑	−1052	〃
11	20	↑	−757	〃
12	21	↑	−462	〃
13	22	↑	−156	〃
14	23	↑	+150	〃
15	24	↑	+456	〃
16	25	↑	+762	〃
17	26	↑	+1068	〃
18	27	↑	+1374	〃
19	28	↑	+1680	〃
20	29	↑	+1986	〃
21	30	↑	+2292	〃
22	31	↑	+2598	〃
23	32	↑	+2904	〃
24	33	seg	+3210	〃
25	34	TEST3	+3581	〃
−	35	TEST	〃	−1795
−	36	TEST	〃	−1584
26	37	K4	〃	−1402
27	38	K3	〃	−1049
28	39	K2	〃	−868
29	40	K1	〃	−515
30	41	RES	+3581	−335
31	42	INT	〃	+698

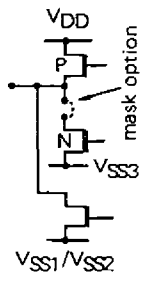
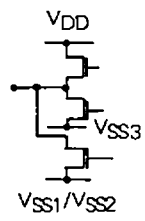
QIP80 pin arrangement				
	Pad No.	Pad name	X (um)	Y (um)
32	43	TEST2	+3581	+878
33	44	TEST1	〃	+1105
34	45	M4	〃	+1285
35	46	M3	〃	+1465
36	47	M2	〃	+1645
37	48	M1	〃	+1825
38	49	S2	〃	+2005
39	50	S1	〃	+2317
40	51	CUP2	〃	+2497
−	52	TEST	〃	+2696
41	53	CUP1	+3300	〃
42	54	seg	+3059	〃
43	55	↓	+2764	〃
44	56	↓	+2469	〃
45	57	↓	+2174	〃
46	58	↓	+1878	〃
47	59	↓	+1583	〃
48	60	↓	+1288	〃
49	61	↓	+993	〃
50	62	↓	+687	〃
51	63	↓	+381	〃
52	64	↓	+75	〃
53	65	↓	−231	〃
54	66	↓	−537	〃
55	67	↓	−843	〃
56	68	↓	−1149	〃
57	69	↓	−1455	〃
58	70	↓	−1761	〃
59	71	↓	−2067	〃
60	72	↓	−2373	〃
61	73	↓	−2679	〃
62	74	seg	−2985	〃
63	75	COM1	−3581	〃
64	76	S4	〃	+2101
65	77	CNT1	〃	+1849
66	78	CNT2	〃	+1298
67	79	LIGHT	〃	+1114
68	80	ALARM	〃	+934
69	81	V_{SS3}	〃	+754
70	82	V_{SS2}	〃	+574
71	83	V_{SS1}	〃	+394

- The values (X, Y) indicate the coordinates of each pad center with the center of the chip as the origin.
- The TEST terminal should be open during normal operation.
- If the chip is used, the substrate must be tied to V_{DD}.

Terminal name	Input/ Output	Circuit configuration	Function	Option	Status during reset
X IN X OUT	Input Output		Connects 32.768kHz or 65.536kHz crystal between X IN and X OUT for oscillation. Used for the timer reference clock and system clock. X OUT incorporates a 20pF capacitor to V_{DD}.	(1) For 32K (2) For 65K *Option (2) is available only on the LC5812H.	
S1 S2 S3 S4	Input		Input-dedicated port Has a 7ms or 32ms chatter removal circuit. By applying V_{DD} to S1 through S4 simultaneously, the internal LSI devices are reset (mask option). (The chatter removal time is for the 32.768kHz option.)	(1) Selection of "L" level Hold Tr. (2) Use of initial reset by simultaneous application of V_{DD} to S1 through S4.	Pull-down resistance is ON during reset.
P2 P3 P4 M1 M2 M3 M3	Input/ Output		I/O port with mode switched by instructions to perform the following operations: (1) Input port: Writes data in RAM (2) Output port: Outputs data from RAM.	Selection of "L" level Hold Tr.	
K1 K2 K3 K4	Input		(1) Used to send data to RAM via 7ms or 32ms chatter removal circuit. (2) Is able to operate the decimal counter in the LSI circuit with a K2 and K4 signal, according to instruction. (The chatter removal time is for the 32.768kHz option.)	Selection of "L" level Hold Tr.	
INT	Input		Controls the external interrupt request. (The mask option interlocks with port K.)	Selection of "L" level Hold Tr.	
RES	Input		Resets the internal LSI devices.	(1) Reset at the "H" level (with pull-down resistor) (2) Reset at the "L" level (with pull-up resistor)	

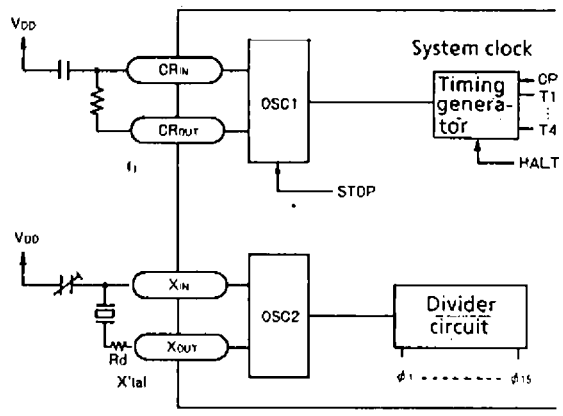
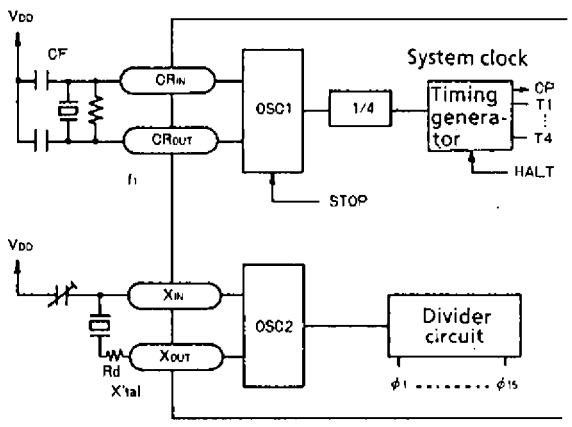
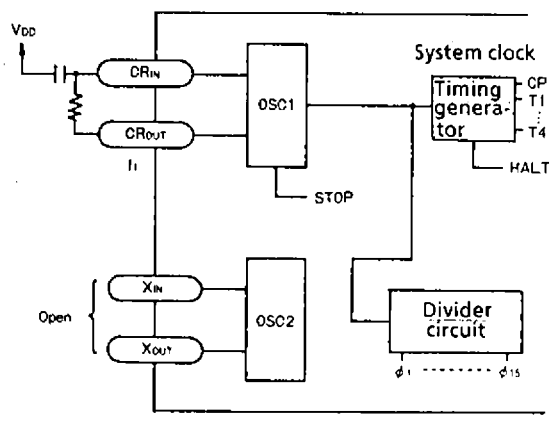
Terminal name	Input/ Output	Circuit configuration	Function	Option	Status during reset
CNT1 CNT2	Output		Output-dedicated port	(1) "L" output during reset. (2) "H" output during reset. *Options 1 and 2 can be specified for each of CNT1 and CNT2.	"L" or "H" output (according to mask option).
LIGHT	Output		Output-dedicated port Suitable for outputting the signals which drive the light transistor.	(1) "L" output during reset. (2) "H" output during reset.	"L" or "H" output (according to mask option)
ALARM	Output		Output-dedicated port Is able to output a 4kHz, 2kHz, or 1kHz modulating signal, according to instruction. Can also output nonmodulating signals. (The modulating frequency is for the 32.768kHz option.)	(1) "L" output during reset. (2) "H" output during reset.	"L" or "H" output (according to mask option).
V_{DD}			(+) supply voltage terminal.		
V_{SS3} V_{SS2} V_{SS1}			V_{SS2} is a supply terminal. V_{SS1} and V_{SS3} are used to supply LCD driving power.		
CUP1 CUP2			Connection terminal for voltage rise (fall) capacitor.		
COM1 COM2 COM3	Output		Output port for common electrodes of LCD panel. Use of terminals varies. (The alternating frequency is for the 32.768kHz option.)	(1) Lighting specification: • Static • Duplex • 1/2 bias 1/3 duty • 1/3 bias 1/3 duty	

	Static	1/2 duty	1/3 duty
COM1	○	○	○
COM2	–	○	○
COM3	–	–	○
Alternating frequency	32Hz	32Hz	43Hz

Terminal name	Input/ Output	Circuit configuration	Function	Option	Status during reset
Segment driver (A group)	Output		LCD panel segment output port. • The terminal can be switched to the output dedicated port depending on the mask option. • If the internal LSI devices are reset, the static lighting signal is fed to COM1 through COM3 and to each of the LCD segment outputs, and all LCD panel segments go on or go off. (on/off:to be specified by mask option) • The segment PLA system is used to draw all patterns on the LCD panel.	① Output for LCD drive ② CMOS output port ③ Pch open drain output port Options ①,②, and ③ can be selected in bit units.	To be specified by mask option ① Lighted mode · Lighted mode (LCD use) · "H" level (DC use) ② Unlighted mode · Unlighted mode (LCD use) · "L" level (DC use)
Segment driver (B group)	Output		LCD panel segment output port. • The terminal can be switched to the output dedicated port depending on the mask option. • If the internal LSI devices are reset the static lighting signal is fed to COM1 through COM3 and to each of the LCD segment outputs, and all LCD panel segments go on or go off. (on/off:to be specified by mask option) • The segment PLA system is used to draw all patterns on the LCD panel.	① Output for LCD drive ② CMOS output port Options ① and ② can be selected in bit units.	To be specified by mask option ① Lighted mode · Lighted mode (LCD use) · "H" level (DC use) ② Unlighted mode · Unlighted mode (LCD use) · "L" level (DC use)
TEST 3 TEST TEST TEST2 TEST1 TEST			Test terminals (the user should not use these terminals).		
CR IN CR OUT			CR oscillation port. The oscillation can be stopped by the HOLD instruction.	(1) CR oscillation	

Note) ⏚ indicates the connection to V_{SS2}.

Oscillation Circuit Option

Option	Circuit configuration	Remarks
CR & X'tal		Cycle time = $f_1/4$ Output from the divider circuit is used as program timer input signal, LCD drive waveform generating signal, or interrupt signal generation, etc. Note) For X'tal = 32.768kHz, set Rd = 0Ω
CF & X'tal		Cycle time = $f_1/16$ Output from the divider circuit is used as program timer input signal, LCD drive waveform generating signal, or interrupt signal generation, etc. Note) For X'tal = 32.768kHz, set Rd = 0Ω
CR option		Cycle time = $f_1/4$ Output from the divider circuit is used as program timer input signal, LCD drive waveform generating signal, or interrupt signal generation, etc.

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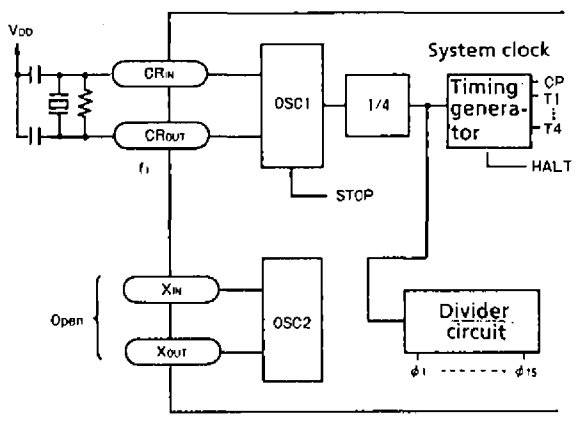
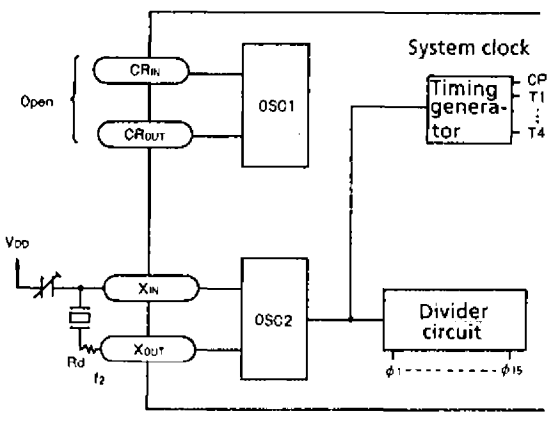
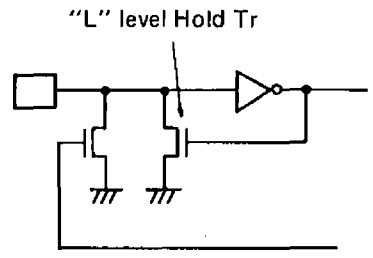
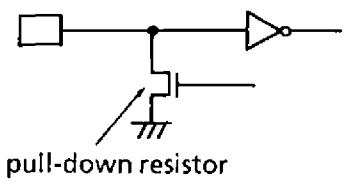
Option	Circuit configuration	Remarks
CF option		Cycle time = $f_1/16$ Output from the divider circuit is used as program timer input signal, LCD drive waveform generating signal, or interrupt signal generation, etc. LC5812H only.
X'tal option		Cycle time = $f_2/4$ Output from the divider circuit is used as program timer input signal, LCD drive waveform generating signal, or interrupt signal generation, etc. Note) For X'tal = 32.768kHz, set Rd = 0Ω

Input Port Option

Option	Circuit configuration	Remarks:
"L" level Hold Tr is used.		• The Hold Tr option is used to reduce the current required for a push-button switch for S1, or a slide switch for S2. • The "L" level signal can be held after the pull-down resistor is set to ON for a short period of time by software during the opening of input.
"L" level Hold Tr is not used.		• The pull-down Tr can be used as a pull-down resistor. • The pull-down Tr can be set to ON/OFF by software.

These options are provided for the S, K, M, and P ports. Be sure to specify NOT USED for the M or P port when using it as an output port.

LCD Output Options

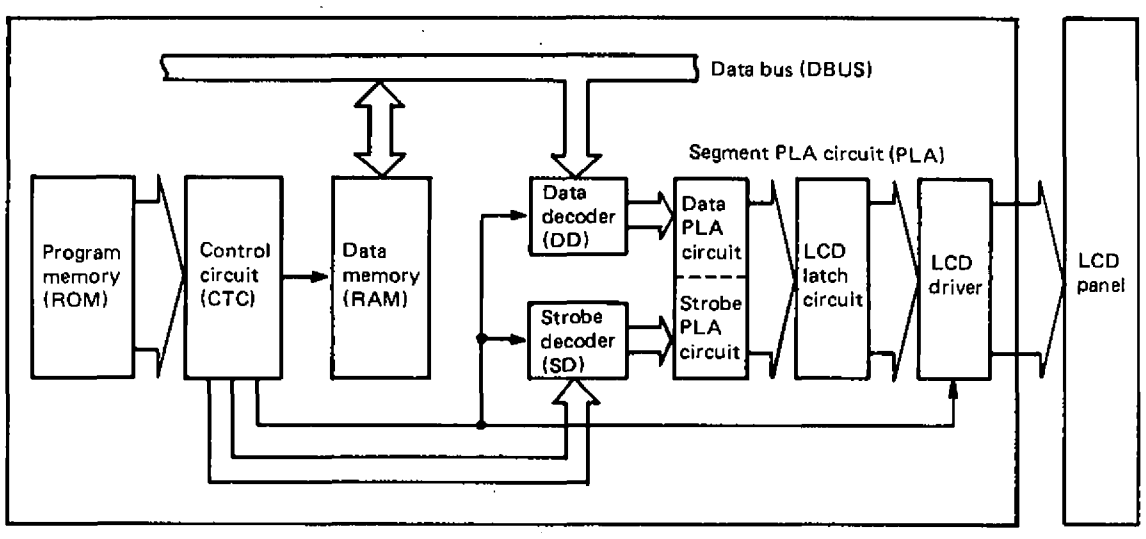
LCD output options for the LCD drive, the CMOS output port and the Pch open drain can be selected.

Option	Output Form
LCD drive	• Terminal for LCD segment drive. • The drive method is determined according to the LCD lighting system specified separately. The LCD lighting system is common to all terminals, and can be selected from among the static, duplex, 1/2 bias-1/3 duty, and 1/3 bias-1/3 duty methods.
CMOS output port	• General-purpose CMOS type output port.
Pch open drain output port	• General-purpose Pch open drain type output port. • Usable according to the PLA option for the predetermined ports.

Alternating waveform for the LCD driver for LCD output is generated by hardware logic.

Segment PLA Circuit

The following figure is a schema of the structure of the segment PLA circuit.



The contents of data memory are sent to the LCD latch circuit for display either as is or after being decoded by the data decoder. The PLA circuit is used to rearrange the input data to output it to the display latch. With this circuit, data memory can be edited to suit LCD panel specifications without software processing. The PLA circuit can be specified by ROM for PLA, which is supplied with program ROM.

Alarm Output

The following frequency divider output can be used directly as an alarm output:

1) Output signal either as $\phi 3$ or $\phi 4$ or $\phi 5$.
2) Any combination output signal at $\phi 10$, $\phi 11$, $\phi 12$, $\phi 13$, $\phi 14$ and $\phi 15$.
3) Modulating output signal of 1) or 2).

These signals can be output by software.
ϕN indicates the output at the Nth step of the oscillator frequency divider.

Resetting Internal Logic

There are three functions for resetting internal logic:

① Built-in power-ON clear circuit
----- Use of this option can be determined by the mask option.

② Reset terminal RES

③ Simultaneous operation of S1 through S4
----- Use of this option can be determined by the mask option.

These reset functions are explained below.

1) Built-in power-ON clear circuit
The initial-clear circuit provided in the microcomputer automatically operates and resets internal logic when power is turned on. This function is very useful in that it can be activated without external devices. But it has the two disadvantages listed below. It is, therefore, recommended that this function be used with other reset functions, or that other methods be used according to applications.

Disadvantages:

a) The circuit may not operate under certain power-rise conditions during the power-ON sequence or due to chatter.

b) Malfunctions may take place due to pulse noise in the power or a sudden change in status.

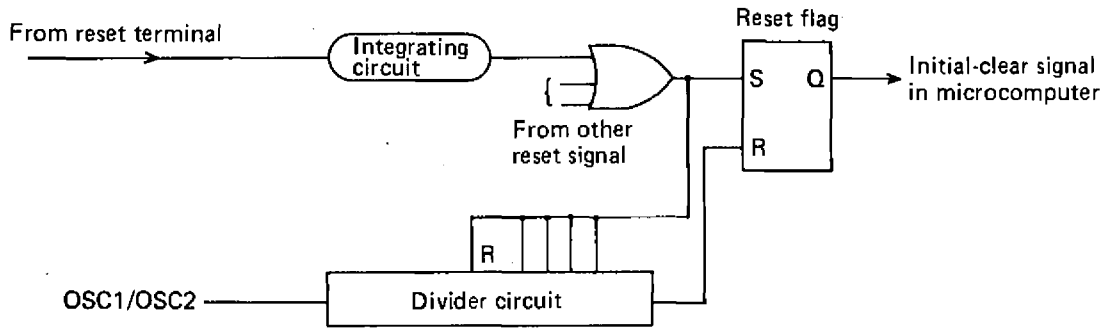
One of the following two reset options can be selected:

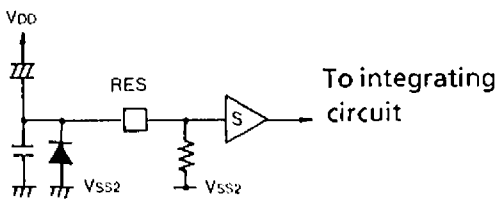
INHIBIT: The built-in power-ON clear circuit is not used
----- Use this option where malfunctions due to pulse noise in the power may take place.

NORMAL ACTION: The built-in power-ON clear circuit is used.
----- This option should be selected only when pulse noise does not affect the power.

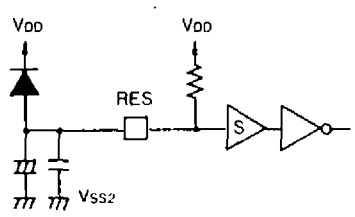
2) Reset terminal RES

When the reset signal is fed to the reset terminal, the reset flag in the micrcomputer is set and part of the divider circuit is reset. Internal logic is reset by the internal reset flag which is reset by the overflow signal from the divider circuit. The reset status of the logic circuit is released and the program coutner starts operating.



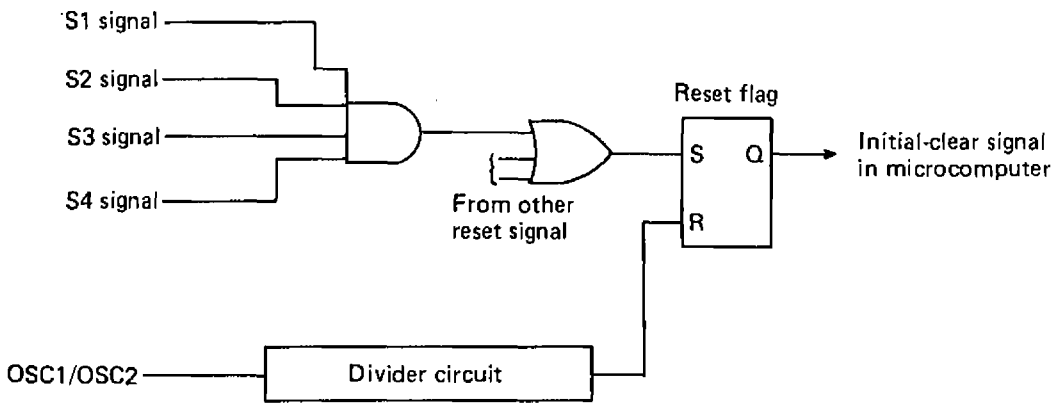


a) with Pull-down R (H-RESET)



b) with Pull-up R (L-RESET)

3) Simultaneous operation of S1 through S4
By applying V_{DD} level voltage to S1 through S4 simultaneously, internal logic can be cleared (initial clear).
(Use of this option can be specified by the mask option.)



Interrupt Function

- Five factors and four vector addresses are provided for the interrupt function.
  - External interrupt terminal (INT) } Same vector address
  - Change of signal to port S ro K }
  - Underflow of programmable timer
  - Overflow of divider circuit
  - Overflow/underflow of decimal UP/DOWN counter

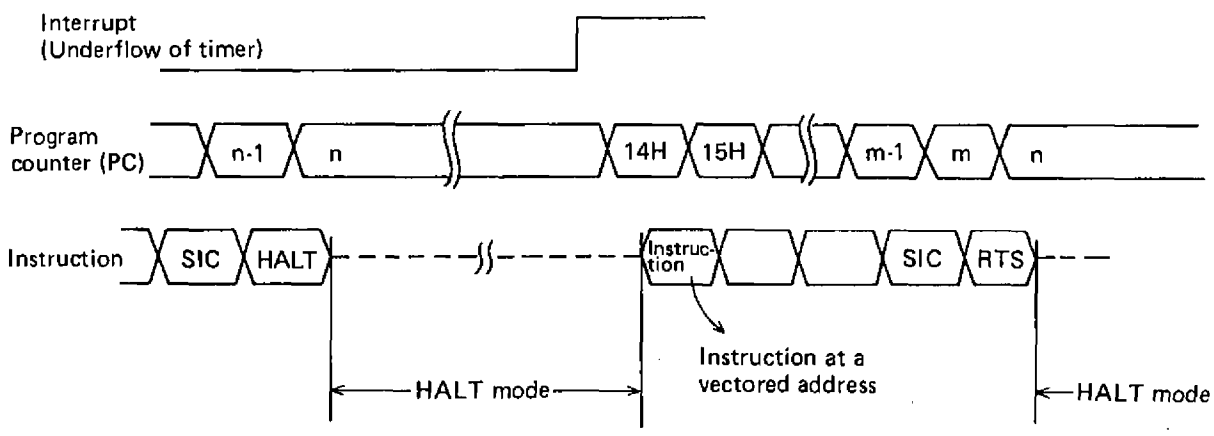
HALT function

- Can stop the CPU's system clock in HALT mode with the HALT instruction.
- Reduces the operating current to the oscillation circuit+HALT release signal+LCD drive circuit current during HALT.
- The following five factors cause HALT release request signals:

  – External interrupt terminal (INT)
  – Change of signal to port S or K
  – Underflow of programmable timer
  – Overflow of divider circuit
  – Overflow or underflow of decimal UP/DOWN counter

The factors for the HALT release request signal are the same as those for the interrupt request signal, but the use of any factor can be specified in programs.

If an interrupt occurs in HALT mode, the operation called for by the interrupt is performed, and the CPU returns to HALT mode.



Release of HALT by Interrupt

HOLD Function

- Can stop the operation of the oscillation circuit (OSC1) in HOLD mode with the STOP instruction.
- Reduces the current dissipation to the minimum during HOLD because OSC1 and CPU are stopped.

Relationship between the oscillation options and the HOLD release functions

Item	Reset signal (RES/RES)	Interrupt request signal	HALT release request signal	Note
CR & X'tal option	○	○	○	
CF & X'tal option	○	×	×	
CR option	○	×	×	
CF option	○	×	×	
X'tal option	×	×	×	HOLD function can not be used.

○: can be used to release HOLD.
×: cannot be used to release HOLD.

Decimal UP/DOWN Counter Function

A hardware function that counts external pulse or the internal reference pulse in decimal notation. One of the following three operations can be selected by software:

① The counting of pulses from port K4 with UP and DOWN switched by the signal level of port K2.

② The counting of pulses from port K4 with UP and DOWN switched by the phase difference signal of port K2.

③ The counting of divider circuit signals of the oscillator in ascending order.
----- With this function, a chrono counter in units of 1/100 second can be implemented by using a 32.768 kHz crystal oscillator.

Option List

		LC5812	LC5812H	Remarks
LCD lighting method		Static	Static	Select "Unused" when the LCD output ports are all used as general-purpose ports.
		Duplex	Duplex	
		1/2 bias 1/3 duty	1/2 bias 1/3 duty	
		1/3 bias 1/3 duty	1/3 bias 1/3 duty	
		Unused	Unused	
"L" level Hold Tr	S ports (S1 to S4)	"L" level Hold Tr is used. "L" level Hold Tr is not used.	"L" level Hold Tr is used. "L" level Hold Tr is not used.	
	M ports (M1 to M4)	"L" level Hold Tr is used. "L" level Hold Tr is not used.	"L" level Hold Tr is used. "L" level Hold Tr is not used.	
	K ports (K1 to K4)	"L" level Hold Tr is used. "L" level Hold Tr is not used.	"L" level Hold Tr is used. "L" level Hold Tr is not used.	
	INT port	"L" level Hold Tr is used. "L" level Hold Tr is not used.	"L" level Hold Tr is used. "L" level Hold Tr is not used.	
	P ports (P1 to P4)	"L" level Hold Tr is used. "L" level Hold Tr is not used.	"L" level Hold Tr is used. "L" level Hold Tr is not used.	
Oscillator selection		CR & XTAL	CR & XTAL	Do not specify CF on the LC5812, because it is not allowed to use CF on the model.
		CR	CF & XTAL	
		XTAL	CR	
			CF	
			XTAL	
Internal power-on reset function		Unused Used	Unused Used	
Simultaneous operation of S1 through S4 for reset		Used Unused	Used Unused	
Selection of RES polarity		"H" level reset (Pull-down) "L" level reset (Pull-up)	"H" level reset (Pull-down) "L" level reset (Pull-up)	
Selection of output terminal polarity	CNT1	"H" level during reset (Normal "H") "L" level during reset (Normal "L")	"H" level during reset (Normal "H") "L" level during reset (Normal "L")	
	CNT2	"H" level during reset (Normal "H") "L" level during reset (Normal "L")	"H" level during reset (Normal "H") "L" level during reset (Normal "L")	
	ALARM	"H" level during reset (Normal "H) "L" level during reset (Normal "L")	"H" level during reset (Normal "H") "L" level during reset (Normal "L")	
	LIGHT	"H" level during reset (Normal "H") "L" level during reset (Normal "L")	"H" level during reset (Normal "H") "L" level during reset (Normal "L")	

LC5812

V_{DD}=0V 1/2bias 1/2duty

Item	Symbol	Conditions	Terminal	Min	Typ	Max	Unit
Absolute Maximum Ratings	Ta = 25°C, V_{DD} = 0V						
Maximum supply voltage	V_{SS1}			−4.0		+0.3	V
	V_{SS2}	V_{SS2}=V_{SS3}		−4.0		+0.3	V
Maximum input voltage	V_{IN1}			V_{SS2} −0.3		+0.3	V
Maximum output voltage	V_{OUT1}			V_{SS2} −0.3		+0.3	V
Operating ambient temperature	Topr			−20		+70	°C
Storage ambient temperature	Tstg			−30		+125	°C
Allowable Operating Conditions	**Ta=−20 to +70°C , V_{DD} = 0V**						
Power supply voltage	V_{SS1}			−3.6		−1.3	V
	V_{SS2}	V_{SS2}=V_{SS3}		−3.6		−2.0	V
"H" level input voltage	V_{IH1}		RES	0.25× V_{SS2}		0	V
	V_{IH2}		Input terminals other than RES	0.3× V_{SS2}			V
"L" level input voltage	V_{IL1}		RES	V_{SS2}		0.75× V_{SS2}	V
	V_{IL2}		Input terminals other than RES	V_{SS2}		0.7× V_{SS2}	V
Operation frequency	fopg1	V_{SS2}=−2.0 to −3.6V	XIN/XOUT	32		33	kHz
	fopg2	V_{SS2}=−2.3 to −3.6V	CRIN/CROUT	17	33	50	kHz
Electrical Characteristics	**Ta=−20 to +70°C , V_{DD} = 0V**						
Input resistance	R_{IN1A}	V_{SS2}=−2.9V, V_{IN}=0.8V_{SS2}	"L" level hold Tr *1, Fig. 1	50		500	kohm
	R_{IN1B}	V_{SS2}=−2.9V, V_{IN}=V_{DD}	"L" level pull-in Tr *1, Fig. 1	200	500	2000	kohm
	R_{IN2A}	V_{SS2}=−2.9V, V_{IN}=0.8V_{SS2}	"L" level hold Tr *2, Fig. 1	50		500	kohm
	R_{IN2B}	V_{SS2}=−2.9V, V_{IN}=V_{DD}	"L" level pull-in Tr *2, Fig. 1	200		2000	kohm
	R_{IN3}	V_{SS2}=−2.9V	RES, TEST1, TEST2	10	80	400	kohm
"H" level output voltage	$V_{OH(1)}$	V_{SS2}=−2.4V, I_{OH}=−0.4mA	ALARM,LIGHT,CNT1, CNT2	−1	−0.3		V
"L" level output voltage	$V_{OL(1)}$	V_{SS2}=−2.4V, I_{OL}=0.4mA	ALARM,LIGHT,CNT1, CNT2		V_{SS2} +0.3	V_{SS2} +1	V
"H" level output voltage	$V_{OH(2)}$	V_{SS2}=−2.4V, I_{OH}=−90μA	Port M, port P	−1	−0.3		V
"H" level output voltage	$V_{OH(3)}$	V_{SS2}=−2.4V, I_{OH}=−50μA	Port M, port P	−0.6	−0.2		V
"L" level output voltage	$V_{OL(3)}$	V_{SS2}=−2.4V, I_{OL}=0.1mA	Port M, port P		V_{SS2} +0.3	V_{SS2} +1	V
"H" level output voltage	$V_{OH(4)}$	V_{SS2}=−2.4V, I_{OH}=−20μA	Segment	−1	−0.3		V
"H" level output voltage	$V_{OH(5)}$	V_{SS2}=−2.4V, I_{OH}=−0.4μA	PAD No. 13 to 21, 54 to 61 QIP 80 pin number 4 to 12, 42 to 49	−0.2			V
"L" level output voltage	$V_{OL(4)}$	V_{SS2}=−2.4V, I_{OL}=40μA			V_{SS2} +0.3	V_{SS2} +1	V
"L" level output voltage	$V_{OL(5)}$	V_{SS2}=−2.4V, I_{OL}=0.4μA				V_{SS3} +0.2	V

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Item	Symbol	Condition	Terminal	Min	Typ	Max	Unit
"H" level output voltage	$V_{OH(6)}$	V_{SS2}=−2.4V, I_{OH}=−5μA	Segment	−1	−0.3		V
"H" level output voltage	$V_{OH(7)}$	V_{SS2}=−2.4V, I_{OH}=−0.4μA	PAD No. 22 to 33, 62 to 74 QIP 80 pin number 13 to 24, 50 to 62	−0.2			V
"L" level output voltage	$V_{OL(6)}$	V_{SS2}=−2.4V, I_{OL}=20μA			V_{SS2} +0.3	V_{SS2} +1	V
"L" level output voltage	$V_{OL(7)}$	V_{SS2}=−2.4V, I_{OL}=0.4μA				V_{SS2} +0.2	V
"H" level output voltage	$V_{OH(8)}$	V_{SS2}=−2.4V, I_{OH}=−4μA	Common 1 – 2	−0.2			V
"M" level output voltage	V_{OM}	V_{SS2}=−2.4V, I_{OH}=−4μA I_{OL}=4μA	Common 1 – 2	$V_{SS2}/2$ −0.2		$V_{SS2}/2$ +0.2	V
"L" level output voltage	$V_{OL(8)}$	V_{SS2}=−2.4V, I_{OL}=4μA	Common 1 – 2			V_{SS2} +0.2	V
Output voltage	V_{SS1}	V_{SS2}=−2.9V	C1=C2=0.1μF fopg=32.768kHz			−1.35	V
Power supply current	$\|I_{DD}\|$	V_{SS2}=−2.9V Ta=25°C STOP	C1=C2=0.1μF CI=25kohms fopg=32.768kHz Co = Cg = 20pF Fig.2			5	μA
Oscillation start voltage	$\|V_{stt}\|$		Co = Cg = 20pF Fig.3			2.2	V
Oscillation hold voltage	$\|V_{HOLD}\|$		Co = Cg = 20pF Fig.3			2.0	V
Oscillation start time	tstt	V_{SS2}=−2.9V	Co = Cg = 20pF Fig.3			10	s
Oscillation correcting capacity	20P	V_{SS2}=−2.9V	XOUT pin	18	22	26	pF
CR oscillation characteristics	f_{CR}	V_{SS2}=−2.3V to −3.6V	R_{EXT}=510kohm C_{EXT}=30pF Fig. 4	16	33	50	kHz

LC5812

V_{DD}=0V 1/2bias 1/3duty

Item	Symbol	Conditions	Terminal	Min	Typ	Max	Unit
Absolute Maximum Ratings	Ta = 25°C, V_{DD} = 0V						
Maximum supply voltage	V_{SS1}			−4.0		+0.3	V
	V_{SS2}	V_{SS2}=V_{SS3}		−4.0		+0.3	V
Maximum input voltage	V_{IN1}			V_{SS2} −0.3		+0.3	V
Maximum output voltage	V_{OUT1}			V_{SS2} −0.3		+0.3	V
Operating ambient temperature	Topr			−20		+70	°C
Storage ambient temperature	Tstg			−30		+125	°C
Allowable Operating Conditions	**Ta=−20 to +70°C , V_{DD} = 0V**						
Power supply voltage	V_{SS1}			−3.6		−1.3	V
	V_{SS2}	V_{SS2}=V_{SS3}		−3.6		−2.0	V
				−5.0		−3.9	V
"H" level input voltage	V_{IH1}		RES	0.25× V_{SS2}		0	V
	V_{IH2}		Input terminals other than RES	0.3× V_{SS2}			V
"L" level input voltage	V_{IL1}		RES	V_{SS2}		0.75× V_{SS2}	V
	V_{IL2}		Input terminals other than RES	V_{SS2}		0.7× V_{SS2}	V
Operation frequency	fopg1	V_{SS2}=−2.0 to −3.6V	XIN/XOUT	32		33	kHz
	fopg2	V_{SS2}=−2.3 to −3.6V	CRIN/CROUT	16	33	50	kHz
Electrical Characteristics	**Ta=−20 to +70°C , V_{DD} = 0V**						
Input resistance	R_{IN1A}	V_{SS2}=−2.9V, V_{IN}=0.8V_{SS2}	"L" level hold Tr *1, Fig. 1	50		500	kohm
	R_{IN1B}	V_{SS2}=−2.9V, V_{IN}=V_{DD}	"L" level pull-in Tr *1, Fig. 1	200	500	2000	kohm
	R_{IN2A}	V_{SS2}=−2.9V, V_{IN}=0.8V_{SS2}	"L" level hold Tr *2, Fig. 1	50		500	kohm
	R_{IN2B}	V_{SS2}=−2.9V, V_{IN}=V_{DD}	"L" level pull-in Tr *2, Fig. 1	200		2000	kohm
	R_{IN3}	V_{SS2}=−2.9V	RES, TEST1, TEST2	10	80	400	kohm
"H" level output voltage	$V_{OH(1)}$	V_{SS2}=−2.4V, I_{OH}=−0.4mA	ALARM,LIGHT,CNT1, CNT2	−1	−0.3		V
"L" level output voltage	$V_{OL(1)}$	V_{SS2}=−2.4V, I_{OL}=0.4mA	ALARM,LIGHT,CNT1, CNT2		V_{SS2} +0.3	V_{SS2} +1	V
"H" level output voltage	$V_{OH(2)}$	V_{SS2}=−2.4V, I_{OH}=−90μA	Port M, port P	−1	−0.3		V
"H" level output voltage	$V_{OH(3)}$	V_{SS2}=−2.4V, I_{OH}=−50μA	Port M, port P	−0.6	−0.2		V
"L" level output voltage	$V_{OL(3)}$	V_{SS2}=−2.4V, I_{OL}=0.1mA	Port M, port P		V_{SS2} +0.3	V_{SS2} +1	V
"H" level output voltage	$V_{OH(4)}$	V_{SS2}=−2.4V, I_{OH}=−20μA	Segment	−1	−0.3		V
"H" level output voltage	$V_{OH(5)}$	V_{SS2}=−2.4V, I_{OH}=−0.4μA	PAD No. 13 to 21, 54 to 61 QIP 80 pin number 4 to 12, 42 to 49	−0.2			V
"L" level output voltage	$V_{OL(4)}$	V_{SS2}=−2.4V, I_{OL}=40μA			V_{SS2} +0.3	V_{SS2} +1	V
"L" level output voltage	$V_{OL(5)}$	V_{SS2}=−2.4V, I_{OL}=0.4μA				V_{SS3} +0.2	V

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Item	Symbol	Condition	Terminal	Min	Typ	Max	Unit
"H" level output voltage (at CMOS output port)	$V_{OH(6)}$	V_{SS2}=–2.4V, I_{OH}=–5μA	Segment	–1	–0.3		V
"H" level output voltage	$V_{OH(7)}$	V_{SS2}=–2.4V, I_{OH}=–0.4μA	PAD No. 22 to 33, 62 to 74 QIP 80 pin number 13 to 24, 50 to 62	–0.2			V
"L" level output voltage (at CMOS output port)	$V_{OL(6)}$	V_{SS2}=–2.4V, I_{OL}=20μA			V_{SS2} +0.3	V_{SS2} +1	V
"L" level output voltage	$V_{OL(7)}$	V_{SS2}=–2.4V, I_{OL}=0.4μA				V_{SS2} +0.2	V
"H" level output voltage	$V_{OH(8)}$	V_{SS2}=–2.4V, I_{OH}=–4μA	Common 1 – 3	–0.2			V
"M" level output voltage	V_{OM}	V_{SS2}=–2.4V, I_{OH}=–4μA I_{OL}=4μA	Common 1 – 3	$V_{SS2}/2$ –0.2		$V_{SS2}/2$ +0.2	V
"L" level output voltage	$V_{OL(8)}$	V_{SS2}=–2.4V, I_{OL}=4μA	Common 1 – 3			V_{SS3} +0.2	V
Output voltage	V_{SS1}	V_{SS2}=–2.9V	C1=C2=0.1μF fopg=32.768kHz			–1.35	V
Power supply current	$\|I_{DD}\|$	V_{SS2}=–2.9V Ta=25°C STOP	C1=C2=0.1μF Cl=25ohms fopg=32.768kHz Co = Cg = 20pF Fig.5			5	μA
Oscillation start voltage	|Vstt|		Co = Cg = 20pF Fig.3			2.2	V
Oscillation hold voltage	$\|V_{HOLD}\|$		Co = Cg = 20pF Fig.3			2.0	V
Oscillation start time	tstt	V_{SS2}=–2.9V	Co = Cg = 20pF Fig.3			10	s
Oscillation correcting capacity	20P	V_{SS2}=–2.9V	XOUT pin	18	22	26	pF
CR oscillation characteristics	f_{CR}	V_{SS2}=–2.3V to –3.6V	R_{EXT}=510kohm C_{EXT}=30pF Fig. 4	17	33	50	kHz

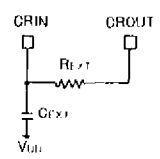


Fig. 1 Input Configuration of S1-4, M1-4, K1-4, P1-4

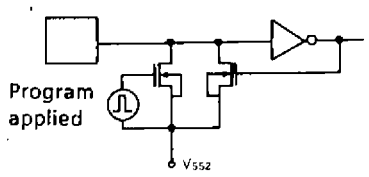


Fig. 2 Output Voltage, Supply Current, OSC HOLD Voltage Test Circuit

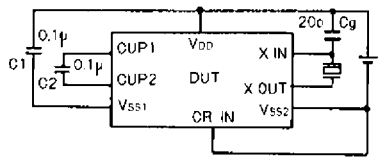


Fig. 3 OSC Start Voltage, OSC Start Time, Frequency Stability Test Circuit

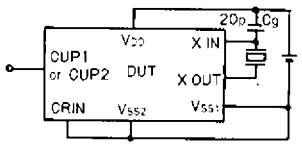


Fig. 4 CR OSC Circuit

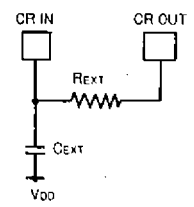
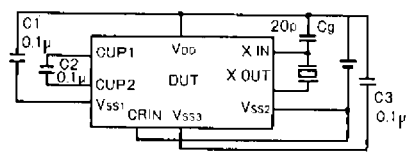


Fig. 5 Output Voltage, Supply Current, OSC Hold Voltage Test Circuit



Unit (capacitance: F)