

**SANYO****LA70100M****SECAM Chroma-Signal Processor IC for VCR****Overview**

LA70100M is a SECAM method chroma-signal processor for VCR applications, realizing reduction in external parts count and adjustment free due to integrated band-pass filter, SECAM discrimination circuit, and BELL filter.

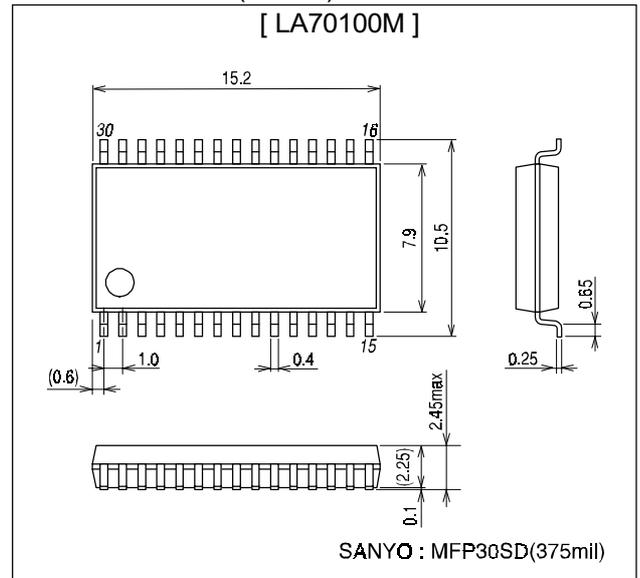
**Features**

- Integrates all filters required.
- Automatic adjustment BELL filter fo.
- Integrates SECAM discrimination circuit.

**Package Dimensions**

unit : mm

3073C-MFP30SD (375mil)

**Specifications****Absolute Maximum Ratings** at  $T_a = 25^\circ\text{C}$ 

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	$V_{CC\ max}$		7.0	V
Allowable power dissipation	$P_d\ max$	$T_a \leq 65^\circ\text{C}$	*440	mW
Operating temperature	$T_{opr}$		-10 to +65	$^\circ\text{C}$
Storage temperature	$T_{stg}$		-40 to +150	$^\circ\text{C}$

\* 114.3mm×76.1mm×1.6mm when mounted on a grass epoxy PCB.

■ Any and all SANYO products described or contained herein do not have specifications that can handle applications that require extremely high levels of reliability, such as life-support systems, aircraft's control systems, or other applications whose failure can be reasonably expected to result in serious physical and/or material damage. Consult with your SANYO representative nearest you before using any SANYO products described or contained herein in such applications.

■ SANYO assumes no responsibility for equipment failures that result from using products at values that exceed, even momentarily, rated values (such as maximum ratings, operating condition ranges, or other parameters) listed in products specifications of any and all SANYO products described or contained herein.

**SANYO Electric Co.,Ltd. Semiconductor Company**

TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

# LA70100M

## Recommended Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V <sub>CC</sub>		5.0	V
Allowable operating voltage range	V <sub>CCOP</sub>		4.8 to 5.2	V

## Electrical Characteristics at Ta = 25°C, V<sub>CC</sub> = 5V

Parameter	Symbol	In	Out	Conditions	Ratings			Unit
					min	typ	max	
Recording mode ( T2 = 4.43MHz, 400mVp-p T29 = Comp.Sync T17 = 0V T4 = OPEN )								
REC mode current drain	ICCR	T16	T23 T24	T16 = 4.286MHz, 200mVp-p	40	50	60	mA
4.3MHz BPF Characteristics-1	VF4C	T16	T18	T9 = 5V T16 = 4.286MHz, 200mVp-p	145	180	215	mVp-p
4.3MHz BPF Characteristics-2	GF4L1	T16	T18	Same condition as above. However, frequency of T16 is 1.1MHz Measure T18 ratio to V4FC.		-30	-20	dB
4.3MHz BPF Characteristics-3	GF4L2	T16	T18	Same condition as above. However, frequency of T16 = 2.2MHz		-10	-5	dB
4.3MHz BPF Characteristics-4	GF4H	T16	T18	Same condition as above. However, frequency of T16 = 7.5MHz		-24	-18	dB
4.3MHz BELL Center frequency	FBLR	T18	T20	T18 = 4 to 5MHz, 200mVp-p SW20 = ON (3.9K pull-down) ( see notes-1 ) Measure during other timing than V-sync	4.243	4.286	4.329	MHz
4.3MHz BELL Characteristics-1	VBLRC	T18	T20	T18 = 4.286MHz, 200mVp-p, BIAS = 4.6V SW20 = ON (3.9K pull-down) Measure during other timing than V-sync	92	110	132	mVp-p
4.3MHz BELL Characteristics-2	GBLRL	T18	T20	Same condition as above. However, frequency of T18 is FBLR-250kHz Measure T18 ratio to VBLRC	-7.5	-6.5	-5.5	dB
4.3MHz BELL Characteristics-3	GBLRH	T18	T20	Same condition as above. However, frequency of T18 is FBLR+250kHz	-7.5	-6.5	-5.5	dB
Anti-BELL Center frequency	FEQR	T12	T11	SW11 = ON (3.9K pull-down) ( see notes-3 ) T12 = 1 to 2MHz, 200mVp-p, BIAS = 4.6V Measure during other timing than V-sync	1.0608	1.0715	1.0822	MHz
Anti-BELL Characteristics-1	VEQRC	T12	T11	Same condition as above. However, frequency of T12 is 1.0715MHz	14	18	22	mVp-p
Anti-BELL Characteristics-2	GEQRL	T12	T11	Same condition as above. However, frequency of T12 is FEQR-62.5kHz Measure T12 ratio to VEQRC	5.0	6.0	7.0	dB
Anti-BELL Characteristics-3	GEQRH	T12	T11	Same condition as above. However, frequency of T12 is FEQR+62.5kHz	5.0	6.0	7.0	dB
REC Chroma signal output level	VOR	T16	T12	T1 = 5V, T16 = 4.4MHz, 200mVp-p	144	180	220	mVp-p
Chroma spurious spectrum-1	GSR1	T16	T12	Same condition as above. Measure 2.2MHz ratio to VOR at T12		-40	-30	dB
Chroma spurious spectrum-2	GSR2	T16	T12	Same condition as above. Measure 3.3MHz ratio to VOR at T12		-36	-30	dB
Sync gate start time	TRGB	T16	T12	T1 = 5V, T9 = 5V ( see notes-7 )	1.1	1.6	2.1	μs
Sync gate release time	TRGE	T16	T12	T16 = 4.286MHz, 200mVp-p	3.6	4.1	4.6	μs
BGP-1 start time	TBGB1	T29	T28	T9 = 5V ( see notes-10 )	5.7	6.2	6.7	μs
BGP-2 start time	TBGB2	T29	T28	Same condition as above. However, T4 = 5V	6.1	6.6	7.1	μs
BGP-3 start time	TBGB3	T29	T28	Same condition as above. However, T4 = 0V	5.3	5.8	6.3	μs
BGP width	TBGW	T29	T28	( see notes-10 )	2.3	2.8	3.3	μs
SECAM DET outout resistance	R26		T28	T27 = 5V ( see notes-11 )	7	10	13	kΩ
SECAM DET characteristics-1	VSCMR1	T16	T28	T16 = SECAM color-bar ( see notes-12 )	4.5			V
SECAM DET characteristics-2	VSCMR2	T16	T28	T16 = PAL color-bar ( see notes-13 )			0.5	V
Regulator voltage	VREG		T13		3.8	4.0	4.2	V

Continued on next page.

# LA70100M

Continued from preceding page.

Parameter	Symbol	In	Out	Conditions	Ratings			Unit
					min	typ	max	
Forced SECAM mode control voltage range	VTHSM	T1 T16	T12	T27 = 3V T16 = 4.286MHz, 200mVp-p Measure voltage range of T1 when signal output from T12.	4.0	4.2	V <sub>CC</sub>	V
Forced Except-SECAM mode control voltage range	VTHMM	T1 T16	T12	T27 = 4V T16 = 4.286MHz, 200mVp-p Measure voltage range of T1 when T12 is mute.	0	0.5	1.0	V
Playback mode ( T2 = 4.43MHz, 400mVp-p T29 = Comp.Sync T17 = 5V, T10/T4 = OPEN )								
PB mode current drain	ICCP	T14	T23 T24	T14 = 1.0715MHz, 50mVp-p	48	60	72	mA
AGC characteristics-1	VAGC	T14	T12	T14 = 1.0715MHz, 50mVp-p T9=5V, T1=5V Voltage of T15 is V15R.	90	120	150	mVp-p
AGC characteristics-2	GAGC1	T14	T12	Same condition as above. However, level of T14 is 100mVp-p Measure T14 ratio to VAGC	-1	0	1	dB
AGC characteristics-3	GAGC2	T14	T12	Same condition as above. However, level of T14 is 25mVp-p	-1	0	1	dB
1.1MHz BPF Characteristics-1	GF1L	T14	T12	V15 = V15R ( see notes-4 ) T14 = 500kHz, 50mVp-p Measure T14 ratio to VAGC	-3	0	3	dB
1.1MHz BPF Characteristics-2	GF1H1	T14	T12	Same condition as above. However, frequency of T14 is 2.2MHz		-30	-20	dB
1.1MHz BPF Characteristics-3	GF1H2	T14	T12	Same condition as above. However, frequency of T14 is 3.3MHz		-35	-25	dB
1.1MHz BELL Center frequency	FEQP	T14	T11	T15 = V15R ( see notes-4 ) T14 = 1 to 1.2MHz, 50mVp-p ( see notes-5 ) SW11 = ON (3.9K pull-down) Measure during other timing than V-sync	1.0608	1.0715	1.0822	MHz
1.1MHz BELL Characteristics-1	VEQPC	T14	T11	Same condition as above. However, frequency of T14 is 1.0715MHz	80	100	120	mVp-p
1.1MHz BELL Characteristics-2	GEQPL	T14	T11	Same condition as above. However, frequency of T14 is FEQP-62.5kHz Measure T14 ratio to VEQPC	-6.5	-5.5	-4.5	dB
1.1MHz BELL Characteristics-3	GEQPH	T14	T11	Same condition as above. However, frequency of T14 is FEQP+62.5kHz	-6.5	-5.5	-4.5	dB
Anti-BELL Center frequency-1	FBLP1	T18	T20	( see notes-6 ) T18 = 4 to 5MHz, 200mVp-p, BIAS = 4.6V	4.243	4.286	4.329	MHz
Anti-BELL Center frequency-2	FBLP2	T18	T20	Same condition as above. However, T10 = 0V	4.283	4.326	4.619	MHz
Anti-BELL Center frequency-3	FBLP3	T18	T20	Same condition as above. However, T10 = 5V	4.323	4.366	4.659	MHz
Anti-BELL characteristics-1	VBLPC	T18	T20	T18 = 4.286MHz, 200mVp-p, BIAS = 4.6V	32	40	48	mVp-p
Anti-BELL characteristics-2	GBLPL	T18	T20	Same condition as above. However, frequency of T18 is FBLP1-250kHz Measure T18 ratio to VBLPC	5.0	6.0	7.0	dB
Anti-BELL characteristics-3	GBLPH	T18	T20	Same condition as above. However, frequency of T18 is FBLP1+250kHz Measure T18 ratio to VBLPC	5.0	6.0	7.0	dB
PB Chroma signal output level	VOP	T14	T18	T1 = 5 V, T14 = 1.0715MHz, 50mVp-p	105	130	160	mVp-p
Chroma spurious spectrum-1	GSP1	T14	T18	Same condition as above. However, measure 2.2MHz ratio to VOP at T18		-45	-35	dB
Chroma spurious spectrum-2	GSP2	T14	T18	Same condition as above. However, measure 3.3MHz ratio to VOP at T18		-28	-20	dB
Sync gate start time	TPGB	T14	T18	T1 = 5V, T9 = 5V ( see notes-9 )	1.2	1.7	2.3	μs
Sync gate release time	TPGE	T14	T18	T14 = 1.0715MHz, 50mVp-p	4.7	5.2	5.7	μs
Phase Det output voltage-1	VSCPD1	T14	T25 T26	T14 = 1.0625/1.1016MHz, 50mVp-p ( see notes-14 )	150	180		mV
Phase Det output voltage-2	VSCPD2	T14	T25 T26	T14 = 627kHz, 50mVp-p. (see notes-14)			100	mV

Continued on next page.

# LA70100M

Continued from preceding page.

Parameter	Symbol	In	Out	Conditions	Ratings			Unit
					min	typ	max	
SECAM detection characteristics-1	VSCMP1	V25 V26	T28	( see notes-15 )	4.5			V
SECAM detection characteristics-2	VSCMP2	V25 V26	T28	( see notes-15 )			0.5	V
R/P control threshold voltage	VTRP	T17		Minimum voltage of T16 under normal PB condition	2.3	2.5	2.7	V
Clock input level	VCLK	T2	T9	T2 = Sign Wave (4.433619MHz), SW9 = ON Minimum voltage of T9 at phase locked T2 with T8.	100	200	800	mVp-p
Sync signal input threshold level	VTHS	T29	T28	Minimum voltage of T29 at BGP outputs normally from T28. T9 = 5V	1.8	2.0	2.2	Vp-p
SECAM DET comparator threshold voltage	VTCOMP	T27	T28	Minimum applied voltage of T27 at T28 = H.	3.2	3.5	3.8	V

## Supplemental Description

(Note 1) REC mode BELL center frequency (FBLR1, FBLR2, FBLR3) :

Input a sine wave (200mVpp, 4 to 5MHz) to T16 and measure the amplitude at T20. Assign to FBLR1 (T10=OPEN), FBLR2 (T10=0V), FBLR3 (T10=5V) the frequency at T16 where the amplitude is maximized.

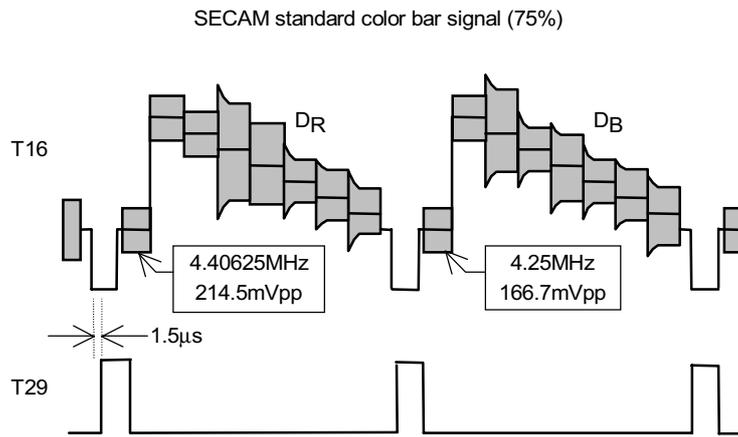


Fig.1

(Note 3) REC EQ (1.1MHz A-BELL) center frequency (FEQR) :

Observe the waveform at T11 when T12=sine wave (200mVpp, 4 to 5MHz, BIAS=4V) is input and assign to FEQR the frequency at T11 where the amplitude is minimized.

(Note 4) Assign to V15R the voltage of T15 at the time of VAGC measurement.

(Note 5) PB EQ (1.1MHz BELL) center frequency (FEQP) :

Input a sine wave (50mVpp, 1 to 1.2MHz) to T14 and assign to FEQP the frequency at T14 where the signal level of T11 is maximized.

(Note 6) PB 4.3MHz A-BELL center frequency (1 FBLP1) / (2 FBLP2) / (3 FBLP3) :

Input a sine wave (200mVpp, 1 to 1.2MHz, BIAS=4V) to T18 and assign to FBQP1 (T10=OPEN), FBQP2 (T10=0V), FBQP3 (T10=5V) the frequency at T18 where the signal level at T20 is minimized.

# LA70100M

(Note 7) REC mode sync gate start time, release time (TRGB, TRGE) :

Input Copm. Sync to T29 and assume the sync gate start time (TRGB) as the time from which the signal at T12 attenuates until the signal at T29 rises and assume the sync gate release time (TRGE) as the time from which the horizontal sync signal rises till the signal at T12 increases (Fig. 2).

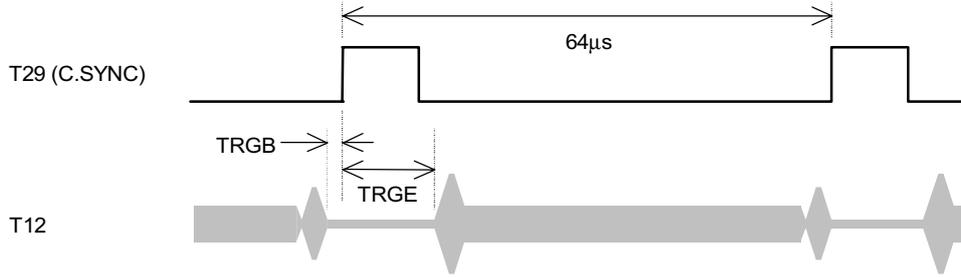


Fig.2 REC mode sync gate timing

(Note 9) PB mode sync gate start time, release time (TRGB, TPGE) :

Input Comp.sync to T29 and assume the sync gate start time (TRGB) as the time from which the signal at T18 attenuates until the horizontal sync signal rises and assume the sync gate release time (TPGE) as the time from which the horizontal sync signal rises until the signal at T18 starts increasing.

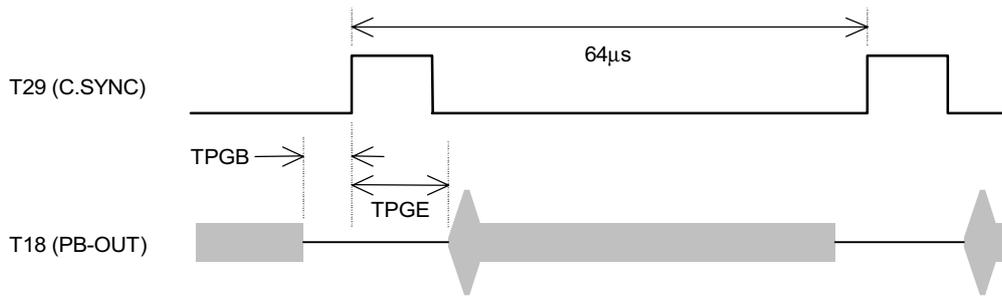


Fig.3 PB mode sync gate timing

(Note 10) BGP start time, BGP width (Fig. 4) T9=5V (TEST MODE)

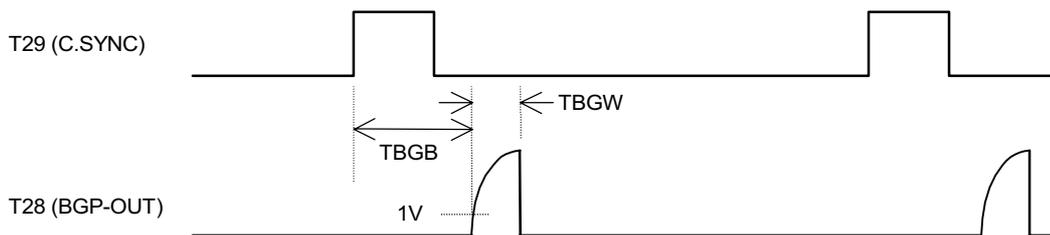


Fig.4 BGP timing

# LA70100M

(Note 11) Output impedance of SECAM DET (R28)

Assign to V28 as when generating 100µA from pin 28 by adding 5V to pin 27 and take “H”, and calculate R28.

$$R28 = \frac{5(V) - V28}{100\mu A}$$

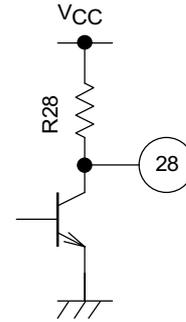


Fig.5

(Note 12) The sync signal at T29 must lag behind the SECAM color bar signal synchronization by 1.5µs (Fig. 1).

(Note 13) The sync signal at T29 must lag behind the PAL color bar signal synchronization by 1.5µs (Fig. 6).

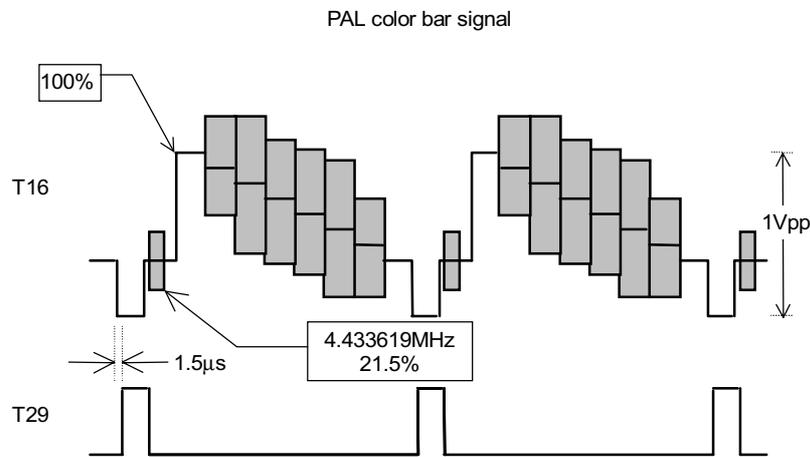


Fig.6

(Note 14) PB mode phase detection output differential voltage :

VSAPD1 : Assign to VPD1 the DC voltage at T25 when a sine wave of 1.0625MHz is input to T14 and VPD2 the DC voltage at T26 when a sine wave of 1.1016MHz is input.  $VSCPD1 = VPD2 - VPD1$

VSAPD2 : Assign to VPD3 and VPD4 the voltage at T25 and T26, respectively, when a sine wave of 627kHz is input to T14.  $VSCPD2 = VPD4 - VPD3$

(Note 15) PB mode SECAM detection characteristics VSCMP1 / VSCMP2 :

VSCMP1 : Apply the above-mentioned VPD1 and VPD2 to T25 and T26, respectively and measure the voltage at T28.

VSCMP2 : Apply the above-mentioned VPD3 and VPD4 to T25 and T26, respectively and measure the voltage at T28.

Functional Description

(1) REC mode

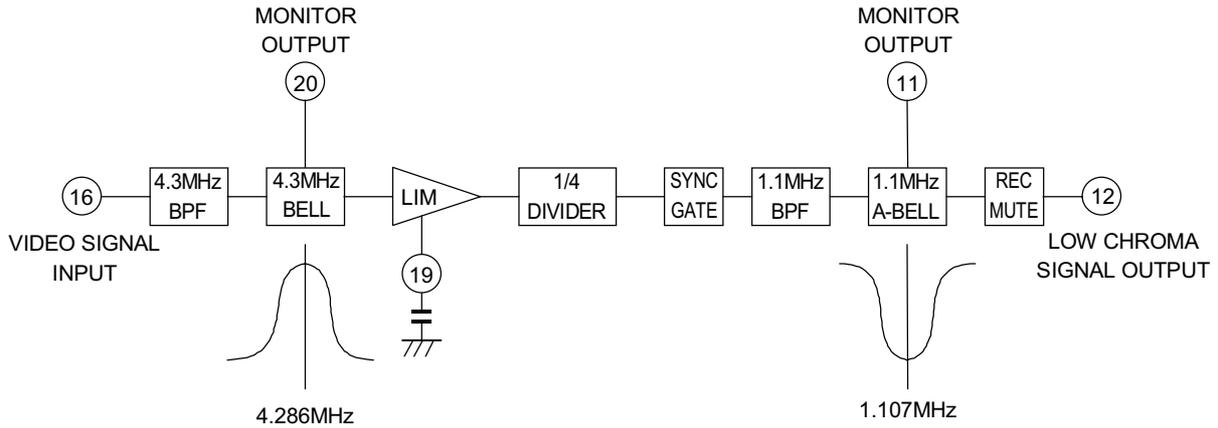


Fig.1 Signal flow in REC mode

Video signals which have been input to Pin 16, pass through the 4.3MHz BPF with unnecessary component (ex. sync signal) removed, and the component of chroma signal is extracted. And the characteristics during transmission are made flat through a 4.3MHz-BELL filter. The center frequency of this filter has automatically been adjusted to be 4.286MHz. After that, the limiter amplifier limits the amplitude, and the chroma signal frequency is converted to 1/4 by a divide-by-four circuit. Though the limiter amplifier amplifies the noise of non-signal parts of the converted signal during synchronization, the sync gate circuit cleans the peripherals of the sync signal. Still more, since this signal has rectangle waveforms, it contains unnecessary component of frequency. To remove it, the signal passes through a 1.1MHz BPF and then is input to 1.1MHz-A-BELL filter. The center frequency of this filter is automatically adjusted to 1.0715MHz, and has opposite characteristics to BELL characteristics. Afterwards, unnecessary components around the sync signal are muted, low-band chroma signal is output to Pin 12 through a buffer.

(2) PB mode

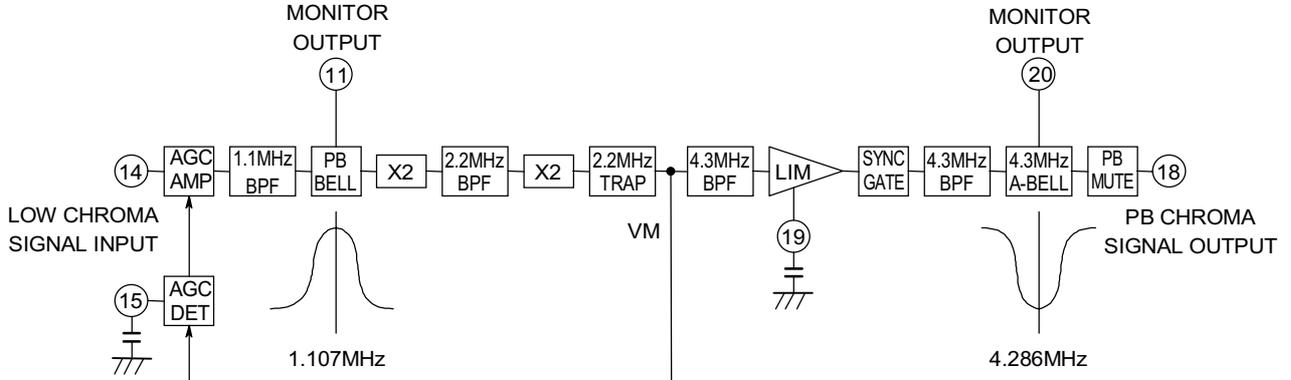


Fig.2 Signal flow in PB mode

The low chroma signal that has been input from Pin 14 enters AGC amplifier and is controlled so that the output level of 4 times multiplier be constant. Then it passes through the 1.1MHz BPF with unnecessary components removed before input to 1.1MHz-BELL filter. The center frequency of this filter has automatically been adjusted to be 1.0715MHz. Next, this signal passes through the 4 times multiplier composed of a 2× multiplier + 2.2 MHz BPF + 2× multiplier + 2.2MHz TRAP + 4.3MHz BPF with unnecessary component of frequency generated in multiplier removed. The first 2× multiplier has auto carrier leak balancer allowing beat obstruction reduced. Next, this signal is limited pulse amplitude by limiting amplifier, then noises around the sync signal owing to limited amplifier are cleaned by the sync gate circuit. This signal has a rectangle waveform and contains unnecessary components of frequency. To remove it, the signal passes through a 4.3MHz BPF before input to 4.3MHz-BELL filter. The center frequency of this filter is automatically adjusted to 4.286MHz, allowing the BELL characteristics to the state during transmission. Afterwards, unnecessary components around the sync signal are muted, low-band chroma signal is output to Pin 18 through a buffer.

(3) CLK INPUT, AFC

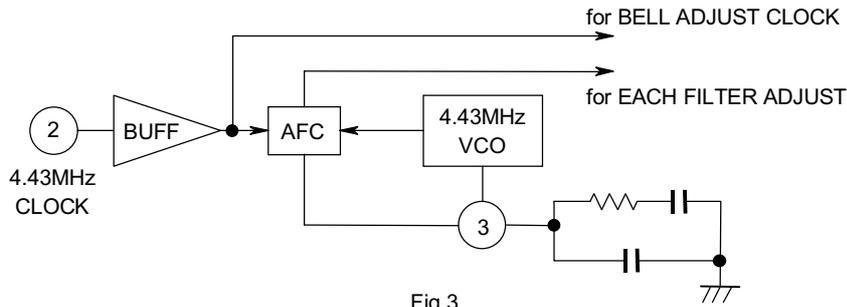


Fig.3

Input a frequency of 4.433619MHz sine wave or rectangle waveform signal of PAL fsc to CLK input terminal. This signal is used for automatically adjusting the BELL filter and generating timing pulse for AFC and for sync gate. AFC circuit automatically adjusts the frequency characteristics for each BPF.

(4) SYNC GATE CIRCUIT

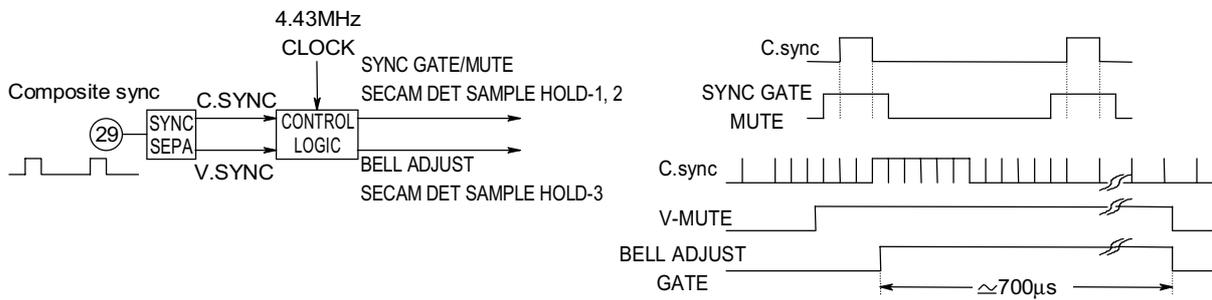


Fig.4

Vertical sync signal is extracted by a synchronous separate circuit from Composite Sync signal that has been input from Pin 29, and is conducted to BELL/A-BELL filter automatic adjusting circuit. Additionally, SYNC GATE pulse and sample hold pulse are generated by the logic circuit.

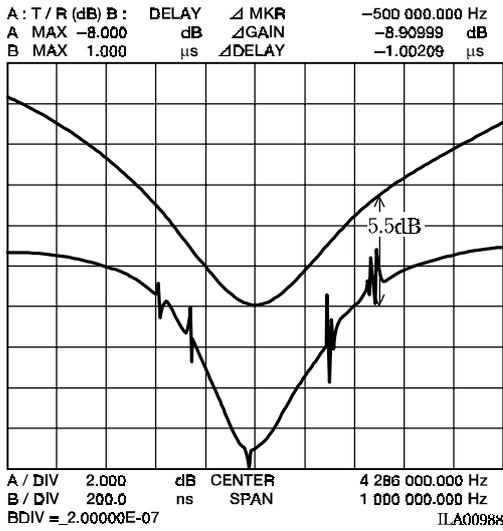
(5) BGP generator circuit

BGP is used for killer circuit in REC Mode, AGC circuit in PB Mode, and SECAM discrimination circuit. In BP Mode, AGC circuit detects the scale of the signal of BGP duration (ID) so that the output of 4 times multiplier circuit be constant. In SECAM discrimination circuit, BGP is used for making the S/H pulse (SP9, SP2 in Figure 9) mentioned later.

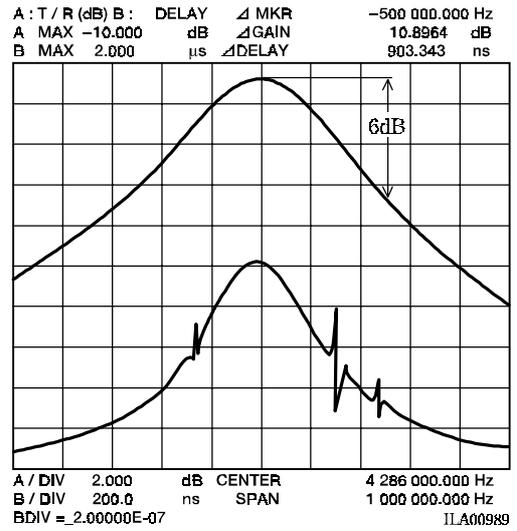
Controlling Pin 4 can convert the timing for Composite Sync that is input to Pin 27. The width of BGP is determined by the constant of the inside of IC to about 2.5 µs. And BGP timing can be monitored by Pin 28 in test mode (Pin 9 voltage = 5V).

(6) REC-BELL filter, PB-A-BELL filter

4.3MHz A-BELL FILTER CHARACTERISTICS



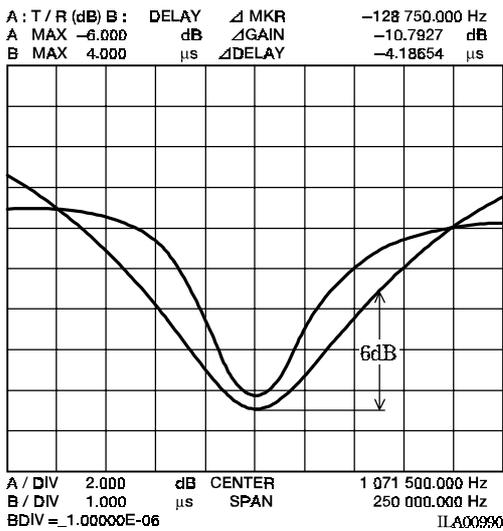
4.3MHz BELL FILTER CHARACTERISTICS



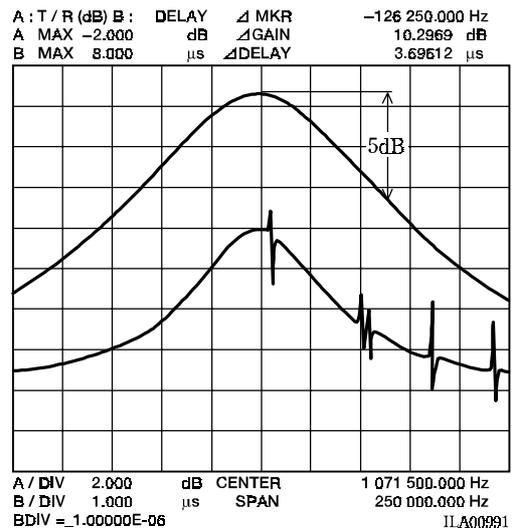
It is an internal filter of which center frequency is fitted to 4.286MHz by automatic adjusting circuit (described later) that uses input frequency (fsc), thus prevents this filter from affected by external components.

(7) REC-A-BELL filter, PB-BELL filter

1.1MHz A-BELL CHARACTERISTICS



1.1MHz BELL CHARACTERISTICS



It is an internal filter of which center frequency is fitted to 1.0715MHz by automatic adjusting circuit (described later) that uses input frequency (fsc), thus prevents this filter from affected by external components.

(8) BELL/A-BELL filter frequency automatic adjustment

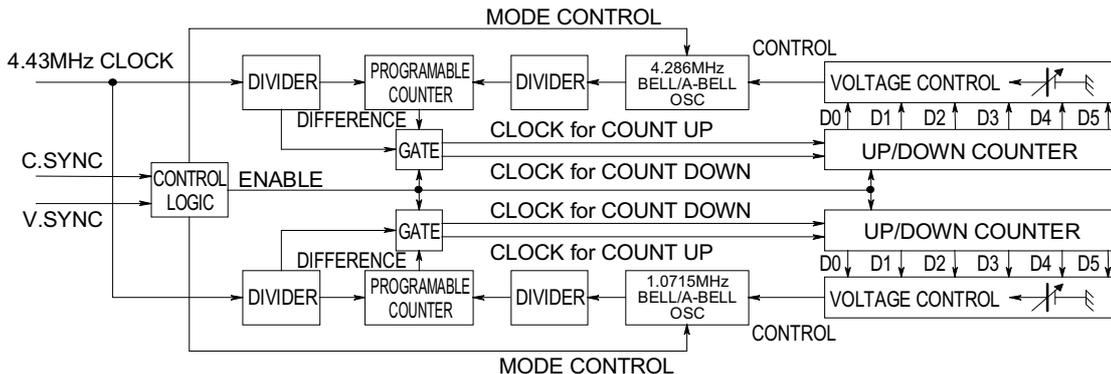


Fig.8 (a)





# LA70100M

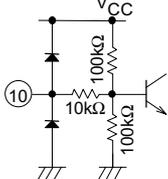
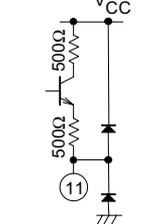
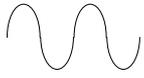
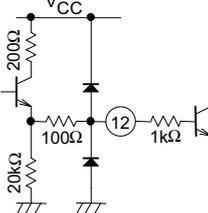
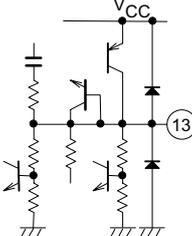
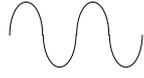
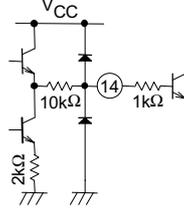
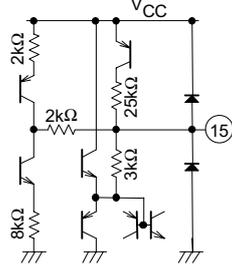
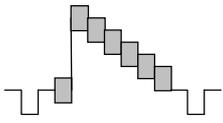
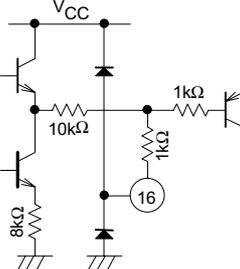
## Pin Description

Pin No.	Pin Name	DC voltage	Signal waveform	Input/output form	Note
1	MODE CTL	2.5V	DC		
2	CLK IN	2.5V	4.43MHz, 400mVp-p 		
3	AFC FILTER	3.5V	DC		
4	BGP DELAY	1 to 5V	DC		
5	No Connect				
6	BAL ( Balancer )	1.2V	DC		
7	GND2	0V			
8	GND	0V			
9	TEST MODE ( VCO MONITOR )	2.1V	Normal : DC  VCO monitor : CW (4.43MHz, 450mVp-p)		Normal : open  VCO monitor : insert resistor to GND  TEST mode ON : pull-up to VCC

Continued on next page.

# LA70100M

Continued from preceding page.

Pin No.	Pin Name	DC voltage	Signal waveform	Input/output form	Note
10	F0 CTL (4.3MHz BELL OFFSET)	2.5V	DC		
11	BELL MONIT 1 (1.1MHz BELL MONIT)	2.7V	Normal : DC  BELL monitor : CW (1.1MHz, 300mVp-p)		Normal : open  BELL monitor : insert resistor to GND
12	REC OUT (TEST SIG I/O)	REC : 2.2V PB : GND	1.1MHz, 700mVp-p 		TEST input : signal with 4V bias
13	REG	4.0V	DC		
14	PB IN	2.5V	1.1MHz, 50mVp-p 		
15	AGC FILTER	$V_{CC}/2 \pm V_{BE}$	DC		
16	REC IN	2.5V	Composite VIDEO 1.0Vp-p 		

Continued on next page.

# LA70100M

Continued from preceding page.

Pin No.	Pin Name	DC voltage	Signal waveform	Input/output form	Note
17	R/P CTL	0 to $V_{CC}$	DC		$V_{TH} = V_{CC}/2$
18	PB OUT (TEST SIG I/O)	PB : 1.95V REC : GND	 4.3MHz, 400mVp-p		TEST input : signal with 4V bias
19	LIM EXC	2.3V	DC		
20	BELL MONIT 4 (4.3MHz BELL MONIT)	2.7V	Normal : DC  BELL monitor : CW (4.3MHz, 400mVp-p)		Normal : open  BELL monitor : insert resistor to GND
21	S/H C3	2.5V	DC (when connecting capacitor)		
22	No Connect				
23	$V_{CC}$	5V	DC		
24	$V_{CC}^2$	5V	DC		
25	S/H C1	2.5V	DC (when connecting capacitor)		

Continued on next page.

# LA70100M

Continued from preceding page.

Pin No.	Pin Name	DC voltage	Signal waveform	Input/output form	Note
26	S/H C2	2.5V	DC (when connecting capacitor)		
27	DET C	2 to 5V	DC		
28	SECAM DET OUT	0V/5V	DC (0V or 5V)		Normal mode
	(BGP MONITOR)		BGP pulse 		At TEST mode
29	SYNC IN	Threshold voltage 2.0V	 Composite sync		
30	SECAM DET SENS	2.0V	DC		

- Specifications of any and all SANYO products described or contained herein stipulate the performance, characteristics, and functions of the described products in the independent state, and are not guarantees of the performance, characteristics, and functions of the described products as mounted in the customer's products or equipment. To verify symptoms and states that cannot be evaluated in an independent device, the customer should always evaluate and test devices mounted in the customer's products or equipment.
- SANYO Electric Co., Ltd. strives to supply high-quality high-reliability products. However, any and all semiconductor products fail with some probability. It is possible that these probabilistic failures could give rise to accidents or events that could endanger human lives, that could give rise to smoke or fire, or that could cause damage to other property. When designing equipment, adopt safety measures so that these kinds of accidents or events cannot occur. Such measures include but are not limited to protective circuits and error prevention circuits for safe design, redundant design, and structural design.
- In the event that any or all SANYO products (including technical data, services) described or contained herein are controlled under any of applicable local export control laws and regulations, such products must not be exported without obtaining the export license from the authorities concerned in accordance with the above law.
- No part of this publication may be reproduced or transmitted in any form or by any means, electronic or mechanical, including photocopying and recording, or any information storage or retrieval system, or otherwise, without the prior written permission of SANYO Electric Co., Ltd.
- Any and all information described or contained herein are subject to change without notice due to product/technology improvement, etc. When designing equipment, refer to the "Delivery Specification" for the SANYO product that you intend to use.
- Information (including circuit diagrams and circuit parameters) herein is for example only ; it is not guaranteed for volume production. SANYO believes information herein is accurate and reliable, but no guarantees are made or implied regarding its use or any infringements of intellectual property rights or other rights of third parties.

This catalog provides information as of September, 2002. Specifications and information herein are subject to change without notice.