

PHASE LOCKED FREQUENCY CONTROLLER

ADVANCE DATA

- PRECISION PHASE LOCKED FREQUENCY CONTROL SYSTEM
- XTAL OSCILLATOR
- PROGRAMMABLE REFERENCE FREQUENCY DIVIDERS
- PHASE DETECTOR WITH ABSOLUTE FREQUENCY STEERING
- DIGITAL LOCK INDICATOR
- DOUBLE EDGE OPTION ON THE FREQUENCY FEEDBACK SENSE AMPLIFIER
- TWO HIGH CURRENT OP-AMPS
- 5V REFERENCE OUTPUT

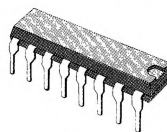
The L6233 is designed for use in phase locked frequency control loops. While optimized for precision speed control of DC motors, these device is universal enough for most applications that require phase locked control. A precise reference frequency can be generated using the device's high frequency oscillator and programmable frequency dividers. The oscillator operates using a broad range of crystals, or, can function as a buffer stage to an external frequency source.

The phase detector on these integrated circuit compares the reference frequency with a frequency/phase feedback signal. In the case of a motor, feedback is obtained at a hall output or other speed detection device. This signal is buffered by a sense amplifier that squares up the

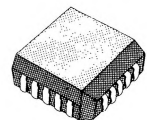
signal as it goes into the digital phase detector. The phase detector responds proportionally to the phase error between the reference and the sense amplifier output. This phase detector includes absolute frequency steering to provide maximum drive signals when any frequency error exists. This feature allows optimum start-up and lock times to be realized.

Two op-amps are included that can be configured to provide necessary loop filtering. The outputs of these op-amps will source or sink in excess of 16mA, so they can provide a low impedance control signal to driving circuits.

Additional features include a double edge option on the sense amplifier that can be used to double the loop reference frequency for increased loop bandwidths. A digital lock signal is provided that indicates when there is zero frequency error and a 5V reference output allows DC operating levels to be accurately set.



DIP-16 Plastic (0.25)

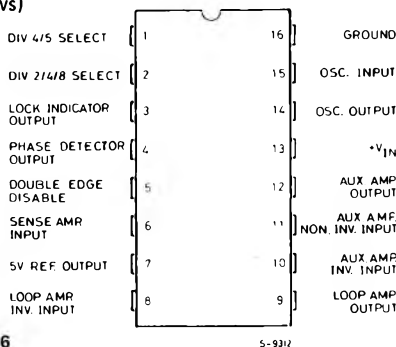


20 PLCC

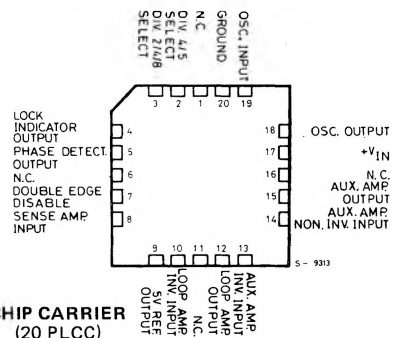
ORDERING NUMBERS: L6233 (DIP-16)
L6233P (20 PLCC)

CONNECTION DIAGRAMS

(Top views)



DIP-16

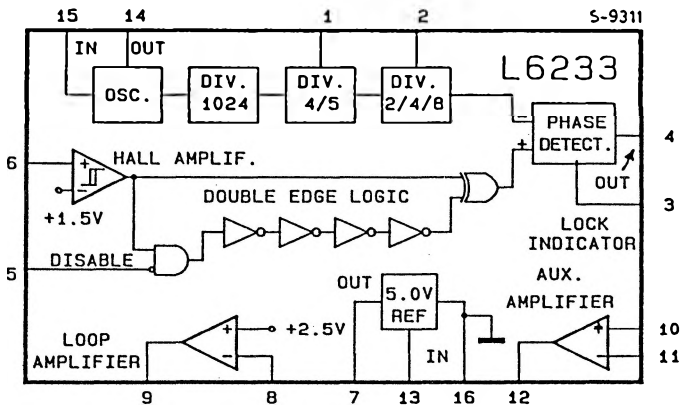


**CHIP CARRIER
(20 PLCC)**

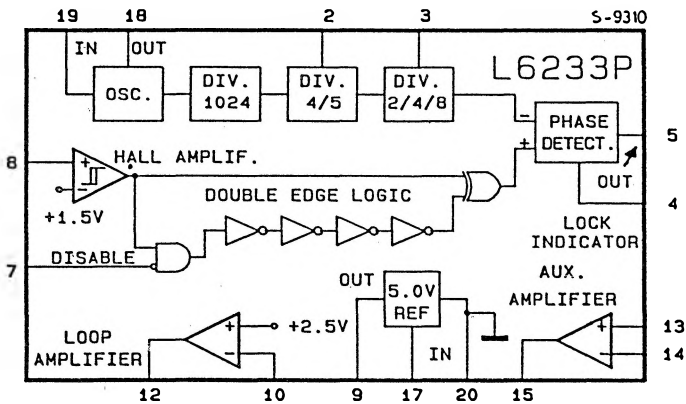
ABSOLUTE MAXIMUM RATINGS

| | | | |
|-----------|---|------------|--------------------|
| V_s | Supply voltage | 14 | V |
| P_{tot} | Power dissipation ($T_{amb} \leq 70^{\circ}\text{C}$) | 1 | W |
| T_{op} | Operating temperature range | 0 to 70 | $^{\circ}\text{C}$ |
| T_{stg} | Storage temperature | -65 to 150 | $^{\circ}\text{C}$ |

BLOCK DIAGRAMS
(DIP-16)



(PLCC PACKAGE)



ELECTRICAL CHARACTERISTICS (Unless otherwise stated, specifications hold for $T_{amb} = 0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$; $+V_{IN} = 12\text{V}$)

| Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|----------------------|-----------------|------|------|------|------|
| I_S Supply current | | | 20 | | mA |

REFERENCE

| | | | | | |
|----------------------------------|-------------------------------|------|-----|------|----|
| V_{REF} Output voltage | | 4.75 | 5.0 | 5.25 | V |
| ΔV_{REF} Load Regulation | $I_{OUT} = 0$ to 7mA | | 5.0 | 20 | mV |
| ΔV_{REF} Line regulation | $+V_{IN} = 8$ to 12V | | 2.0 | 20 | mV |
| I_{SC} Short circuit current | $V_{OUT} = 0\text{V}$ | | 35 | | mA |

OSCILLATOR

| | | | | | |
|--|--|----|-----|--|------------------|
| G_V DC voltage gain | Oscillator input to oscillator output | | 16 | | dB |
| V_{IB} Input DC level | Oscillator input pin open, $T_J = 25^{\circ}\text{C}$ | | 1.3 | | V |
| Z_{IN}^* Input impedance | $V_{IN} = V_{IB} \pm 0.5\text{V}$, $T_J = 25^{\circ}\text{C}$ | | 1.6 | | $\text{K}\Omega$ |
| V_O Output DC level | Oscillator input pin open $T_J = 25^{\circ}\text{C}$ | | 1.4 | | V |
| f_{oMAX} Maximum operating frequency | | 10 | | | MHz |

DIVIDERS

| | | | | | |
|------------------------------------|--|------|------|-----|---------------|
| f_{oMAX} Maximum input frequency | Input = $1V_{pp}$ at oscillator input | 10 | | | MHz |
| Div. 4/5 input current | Input = 5V (Div. by 4) | | 150 | 500 | μA |
| | Input = 0V (Div. by 5) | -5.0 | 0.0 | 5.0 | μA |
| V_{TH} Div. 4/5 threshold | | 0.5 | 1.6 | 2.2 | V |
| Div. 2/4/8 input current | Input = 5V (Div. by 8) | | 150 | 500 | μA |
| | Input = 0V (Div. by 2) | -500 | -150 | | μA |
| Div. 2/4/8 open circuit voltage | Input current = $0\mu\text{A}$ (Div. by 4) | 1.5 | 2.5 | 3.5 | V |
| Div. by 2 threshold | | 0.35 | 0.8 | | V |
| Div. by 4 threshold | | 1.5 | | 3.5 | V |
| Div. by 8 threshold | Volts below V_{REF} | 0.35 | 0.8 | | V |

SENSE AMPLIFIER

| | | | | | |
|----------------------------|-----------------------|--|------|--|---------------|
| V_T Threshold voltage | Percent of V_{REF} | | 30 | | % |
| H_T Threshold hysteresis | | | 10 | | mV |
| I_b Input bias current | Input = 1.5V | | -0.2 | | μA |

DOUBLE EDGE DISABLE INPUT

| | | | | | |
|-------------------------|--------------------------------|------|-----|-----|---------------|
| V_I Input current | Input = 5V (Disabled) | | 150 | 500 | μA |
| | Input = 0V (Enabled) | -5.0 | 0.0 | 5.0 | μA |
| V_T Threshold voltage | | 0.5 | 1.6 | 2.2 | V |

ELECTRICAL CHARACTERISTICS (continued)

| Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|-----------|-----------------|------|------|------|------|
|-----------|-----------------|------|------|------|------|

PHASE DETECTOR

| | | | | | | |
|-----------------|-------------------------------------|--|-----|-----|-----|----|
| V _{OH} | High output level | Positive Phase/Freq. Error, Volts Below V _{REF} | | 0.2 | 0.5 | V |
| V _{OL} | Low output level | Negative Phase/Freq. Error | | 0.2 | 0.5 | V |
| V _{OM} | Mid output level | Zero Phase/Freq. Error, Percent of V _{REF} | 47 | 50 | 53 | % |
| | High level maximum source current | V _{OUT} = 4.3V | 2.0 | 8.0 | | mA |
| | Low level maximum sink curr. | V _{OUT} = 0.7V | 2.0 | 5.0 | | mA |
| | Mid level output impedance (Note 2) | I _{OUT} = -200 to +200μA T _j = 25°C | | 6.0 | | KΩ |

LOCK INDICATOR OUTPUT

| | | | | | | |
|------------------|--------------------|--|--|-----|------|----|
| V _{sat} | Saturation voltage | Freq. Error, I _{OUT} = 5mA | | 0.3 | 0.45 | V |
| | Leakage current | Zero Freq. Error V _{OUT} = 12V | | 0.1 | 1.0 | μA |

LOOP AMPLIFIER

| | | | | | | |
|-----------------|----------------------------|------------------------------------|------|------|----|----|
| | NON INV. reference voltage | Percent of V _{REF} | 47 | 50 | 53 | % |
| I _b | Input bias current | Input = 2.5V | -0.8 | -0.2 | | μA |
| G _v | Open loop gain | | 60 | 75 | | dB |
| SVR | Supply voltage rejection | +V _{IN} = 8 to 12V | 70 | 100 | | dB |
| I _{SH} | Short circuit current | Source, V _{OUT} = 0V | 16 | 35 | | mA |
| | | Sink, V _{OUT} = 5V | 16 | 30 | | mA |

AUXILIARY OP-AMP

| | | | | | | |
|-----------------|--------------------------|------------------------------------|----|-----|---|----|
| V _{OS} | Input offset voltage | V _{CM} = 2.5V | | | 8 | mV |
| I _b | Input bias current | V _{CM} = 2.5V | | 200 | | mA |
| I _{os} | Input offset current | V _{CM} = 2.5V | | 10 | | mA |
| G _v | Open loop gain | | 70 | 120 | | dB |
| SVR | Supply voltage rejection | +V _{IN} = 8 to 12V | 70 | 100 | | dB |
| CMR | Common mode rejection | V _{CM} = 0 to 10V | 70 | 100 | | dB |
| I _{SH} | Short circuit current | Source, V _{OUT} = 0V | | 35 | | mA |
| | | Sink, V _{OUT} = 5V | | 30 | | mA |

* These impedance levels will vary with T_j at about 1700ppm/°C

THERMAL DATA

| | | | | |
|-----------------------|-------------------------------------|-----|-----|------|
| R _{th j-amb} | Thermal resistance junction-ambient | max | 100 | °C/W |
|-----------------------|-------------------------------------|-----|-----|------|

APPLICATION INFORMATION

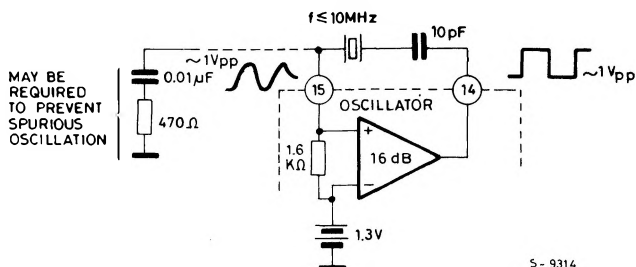
Determining the Oscillator Frequency

The frequency at the oscillator is determined by: the desired RPM of the motor, the divide ratio selected, the number of poles in the motor, and the state of the double edge select pin.

$$f_{osc}(\text{Hz}) = (\text{Divide Ratio}) \cdot (\text{Motor RPM}) \cdot (1/60 \text{ SEC/MIN}) \cdot (\text{No. of Rotor Poles}/2) \cdot (\times 2 \text{ if Pin 5 Low})$$

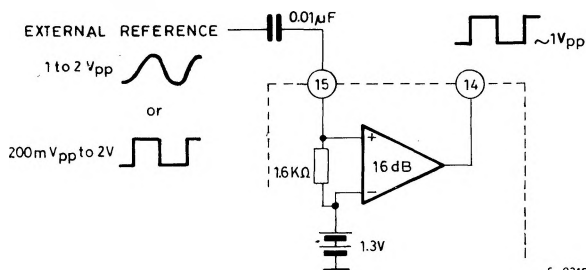
The resulting reference frequency appearing at the phase detector inputs is equal to the oscillator frequency divided by the selected divide ratio. If the double edge option is used, (Pin 5 low), the frequency of the sense amplifier input signal is doubled by responding to both the rising and falling edges of the input signal. Using this option the loop reference frequency can be doubled for a given motor RPM.

Fig. 1 - Recommended Oscillator Configuration Using AT Cut Quartz XTAL



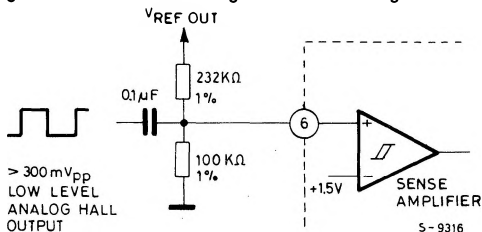
S-9314

Fig. 2 - External Reference Frequency Input



S-9315

Fig. 3 - Method for Deriving Rotation Feedback Signal From Analog Hall Effect Device



S-9316

* This signal may require filtering if chopped mode drive scheme is used.

APPLICATION INFORMATION (continued)

Phase detector operation

The phase detector on these devices is a digital circuit that responds to the rising edges of the detector's two inputs. The phase detector output has three states: a high, 5V state, a low, 0V state, and a middle, 2.5V state. In the high and low states the output impedance of the detector is low, the middle state output impedance is high, typically $6.0K\Omega$. When there is any static frequency difference between the inputs the detector output is fixed at its high level if the +input (the sense amplifier signal) is greater in frequency, and fixed at its low level if the -input (the reference frequency signal) is greater in frequency.

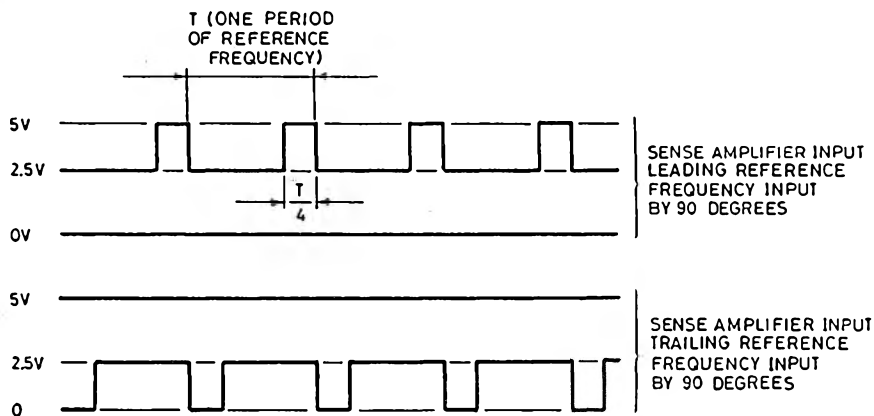
When the frequencies of the two inputs to the detector are equal the phase detector switches between its middle state and either the high or low states, depending on the relative phase of the two signals. If the +input is leading in phase then, during each period of the input frequency, the detector output will be high for a time equal to the time difference between the rising edges of the inputs, and will be at its middle level the remainder of the period. If the phase relationship is reversed then the detector will go low for a time proportional to the phase difference of the inputs. The resulting gain of the

phase detector, $K\phi$, is $5V/4\pi$ radians, or about $0.4V/\text{radian}$. The dynamic range of the detector is $\pm 2\pi$ radians.

The operation of the phase detector is illustrated in the figures below. The upper figure shows typical voltage waveforms seen at the detector output for leading and lagging phase conditions. The lower figure is a state diagram of the phase detector logic. In this figure, the circles represent the 10 possible states of the logic and the connecting arrows the transition events/paths to and from these states. Transition arrows that have a clockwise rotation are the result of a rising edge on the +input, and conversely, those with counter-clockwise rotation are tied to the rising edge on the -input signal.

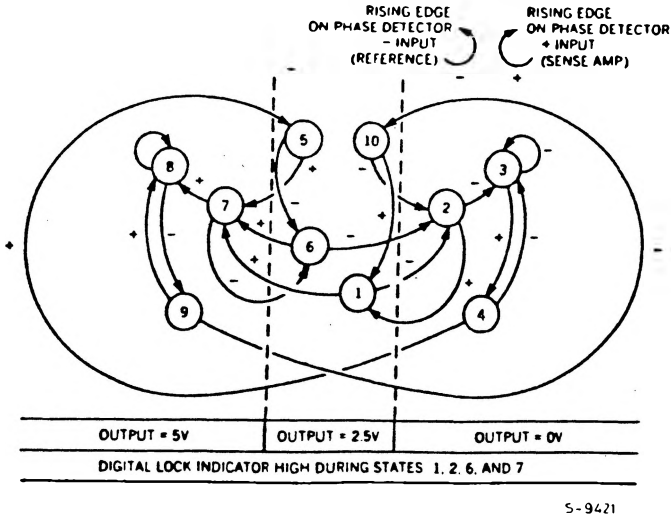
The normal operational states of the logic are 6 and 7 for positive phase error, 1 and 2 for a negative phase error. States 8 and 9 occur during positive frequency error, 3 and 4 during negative frequency error. States 5 and 10 occur only as the inputs cross over from a frequency error to a normal phase error only condition. The level of the phase detector output is determined by the logic state as defined in the state diagram figure. The lock indicator output is high, off, when the detector is in states 1, 2, 6 or 7.

Fig. 4 - Typical Phase Detector Output Waveforms



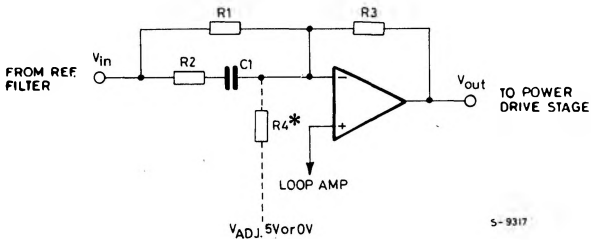
S-9319

Fig. 5 - Phase Detector State Diagram



S-9421

Fig. 6 - Suggested Loop Filter Configuration



S-9317

$$\frac{V_{OUT}}{V_{IN}}(S) = \frac{R3}{R1} \cdot \frac{1 + S/\omega Z}{1 + S/\omega P}$$

$$\omega P = \frac{1}{R2 C1}$$

$$\omega Z = \frac{1}{(R1 + R2) C1}$$

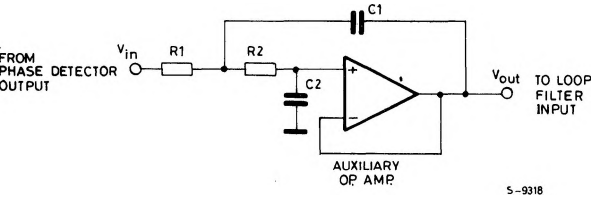
- * The statistic phase error of the loop is easily adjusted by adding resistor, $R4$, as shown. To lock at zero phase error $R4$ is determined by:

$$R4 = \frac{2.5V \cdot R3}{|\Delta V_{OUT}|}$$

Where: $|\Delta V_{OUT}| = |V_{OUT} - 2.5V|$
and V_{OUT} = DC Operating Voltage At Loop Amplifier Output During Phase Lock

$(V_{OUT} - 2.5) > 0$ $R4$ Goes to 0V
 $(V_{OUT} - 2.5) < 0$ $R4$ Goes to 5.0V

Fig. 7 - Reference Filter Configuration



$$\frac{V_{OUT}}{V_{IN}}(S) = \frac{1}{1 + \frac{S^2}{\omega_N^2} + \frac{S^2}{\omega_N^2}}$$

$$\omega_N = \frac{1}{\sqrt{R_1 R_2 C_1 C_2}}$$

$$\delta = \frac{1}{2Q} = \frac{1}{2} \sqrt{\frac{C_2}{C_1}} \frac{R_1 + R_2}{\sqrt{R_1 R_2}}$$

Note: with $R_1 = R_2$ $\delta = \sqrt{\frac{C_2}{C_1}}$

Fig. 8 - Reference Filter Design Aid - Gain Response

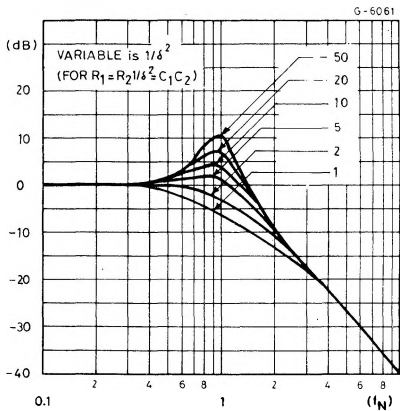


Fig. 9 - Reference Filter Design Aid - Phase Response

