

100 V DMOS SWITCHES

ADVANCE DATA

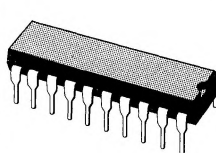
- OUTPUT VOLTAGE TO 100 V
- $0.5 \Omega R_{DS(on)}$
- SUPPLY VOLTAGE UP TO 60 V
- LOW INPUT CURRENT
- TTL/CMOS COMPATIBLE INPUTS
- HIGH SWITCHING FREQUENCY (200 KHz)

DESCRIPTION

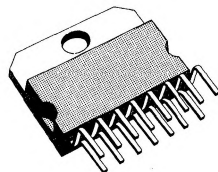
Realized with the Multipower-BCD mixed bipolar/CMOS/DMOS process, the L6122/23 monolithic three DMOS switch is designed for high current, high voltage switching applications. Each of the three switches is controlled by a logic input and all three are controlled by a common enable input. All inputs are TTL/CMOS compatible for direct connection to logic circuits. Each source is available for the insertion of the sense resistors in current control applications.

Two versions are available : the L6122 mounted in a Powerdip 14 + 3 + 3 package and the L6123 in a 15-lead Multiwatt package.

Multipower BCD Technology



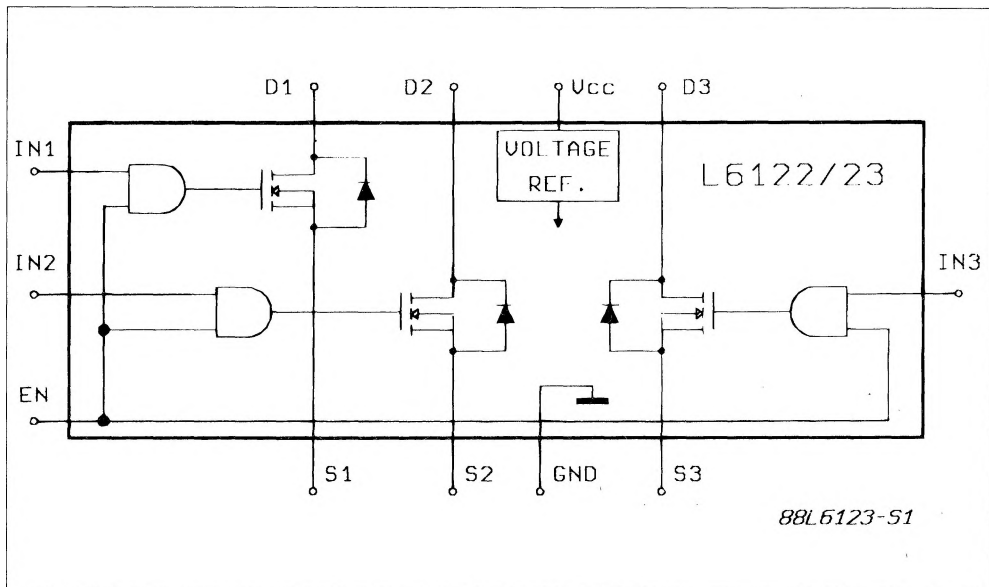
Powerdip
14+3+3



Multiwatt-15

ORDER CODES : L6122
L6123

BLOCK DIAGRAM

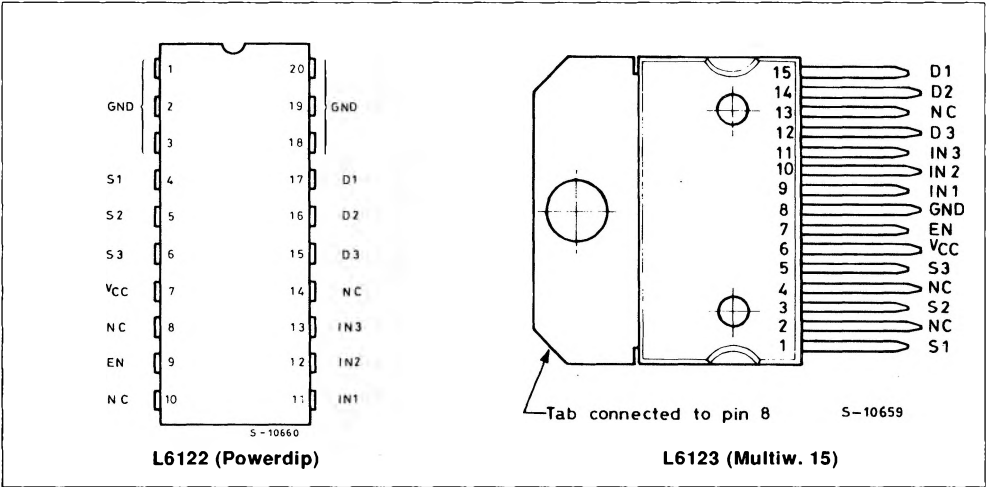


ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{DS}	Drain-source Voltage		100	V
V_{CC}	Supply Voltage		60	V
I_D	Continuous Drain Current	@ $T_{pins} = 90\text{ }^{\circ}\text{C}$ Powerdip	1.5	A
		@ $T_{case} = 90\text{ }^{\circ}\text{C}$ Multiwatt -15	3	A
$I_{DM} (*)$	Pulsed Drain Current	Powerdip	5	A
		Multiwatt -15	8	A
I_{SD}	Continuous Source-drain Diode Current	@ $T_{pins} = 90\text{ }^{\circ}\text{C}$ Powerdip	1.5	A
		@ $T_{case} = 90\text{ }^{\circ}\text{C}$ Multiwatt -15	3	A
I_{SDM}	Pulsed Source Drain Diode Current	Powerdip	5	A
		Multiwatt -15	8	A
V_{IN}	Input Voltage		7	V
V_{EN}	Enable Voltage		7	V
V_S	Source Voltage		- 1 to + 4	V
P_{Tot}	Total Power Dissipation	@ $T_{pins} = 90\text{ }^{\circ}\text{C}$ Powerdip	4.3	W
		@ $T_{case} = 90\text{ }^{\circ}\text{C}$ Multiwatt -15	20	W
		@ $T_{amb} = 70\text{ }^{\circ}\text{C}$ Powerdip	1.3	W
		@ $T_{amb} = 70\text{ }^{\circ}\text{C}$ Multiwatt -15	2.3	W
T_{stg}, T_j	Storage and Junction Temperature Range		- 40 to + 150	$^{\circ}\text{C}$

(*) Pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 10\text{ }\%$.
NOTE : $I_D, I_{DM}, I_{SD}, I_{SDM}$ are given per channel.

CONNECTION DIAGRAMS (top view)



THERMAL DATA

			Powerdip	Multiwatt -15
$R_{th j-pins}$	Thermal Resistance Junction-pins	Max	14 $^{\circ}\text{C/W}$	-
$R_{th j-case}$	Thermal Resistance Junction-case	Max	-	3 $^{\circ}\text{C/W}$
$R_{th j-amb}$	Thermal Resistance Junction-ambient	Max	65 $^{\circ}\text{C/W}$	35 $^{\circ}\text{C/W}$

ELECTRICAL CHARACTERISTICS (T_j = 25 °C, V_{CC} = 40 V, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{CC}	Supply Voltage		14		48	V
I _{CC}	Supply Current	All V _{IN} = H V _{EN} = Square Wave (200 KHz, 50 % DC)		9		mA
I _Q	Quiescent Current	V _{EN} = L		2	3	mA
BV _{DSS}	Drain Source Breakdown Voltage	I _D = 1 mA V _{EN} = L	100			V
I _{DSS}	Output Leakage Current	V _{EN} = L			1	mA
		V _{DS} = 100 V V _{DS} = 80 V T _j = 125 °C		1		mA
R _{DS (on)} (*)	Static Drain-source on Resistance	V _{CC} ≥ 14 V V _{EN} , V _{IN} = H I _D = 1.5 A		0.7		Ω
V _{INL} , V _{ENL}	Input Low Voltage		- 0.3		0.8	V
V _{INH} , V _{ENH}	Input High Voltage		2		7	V
I _{INL} , I _{ENL}	Input Low Current	V _{IN} , V _{EN} = L			- 100	μA
I _{INH} , I _{ENH}	Input High Current	V _{IN} , V _{EN} = H			10	μA
t _{d (on)}	Turn on Delay Time			300		ns
t _r	Rise Time	I _D = 1.5 A		100		ns
t _{d (off)}	Turn off Delay Time	See Test Circuit and Waveforms		400		ns
t _f	Fall Time			100		ns
V _{SD} (*)	Source Drain Diode Forward Voltage	I _{SD} = 1.5 A V _{EN} = L			1.5	V
V _{SD (on)} (*)	Source Drain Forward Voltage	I _{SD} = 1.5 A V _{IN} , V _{EN} = H			1.2	V

(*) Pulse test : pulse width = 300 μs, duty cycle = 2 %.

SWITCHING TIMES RESISTIVE LOAD

Figure 1 : Test Circuit.

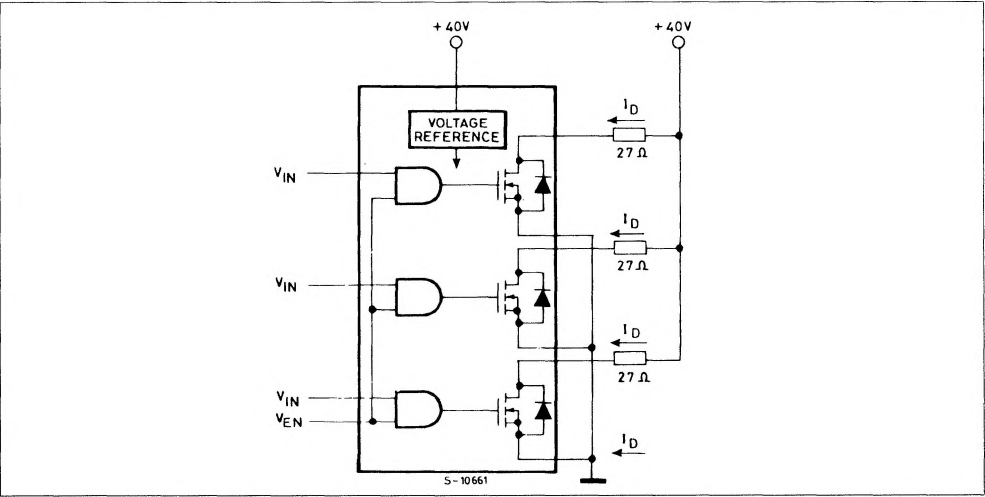


Figure 2 : Waveforms.

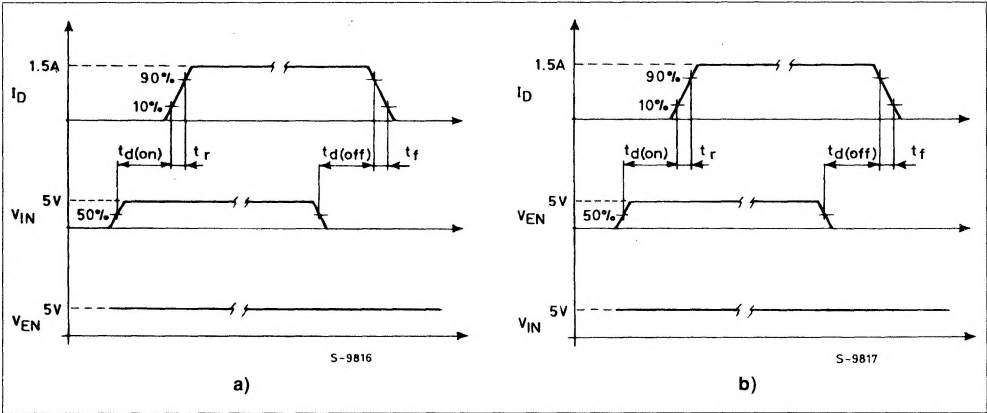


Figure 3 : Static Drain-source on Resistance.

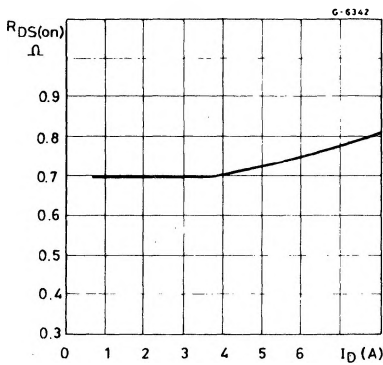


Figure 5 : Normalized on Resistance vs. Temperature.

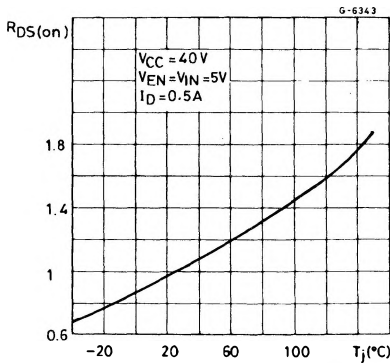


Figure 4 : Normalized Breakdown Voltage vs. Temperature.

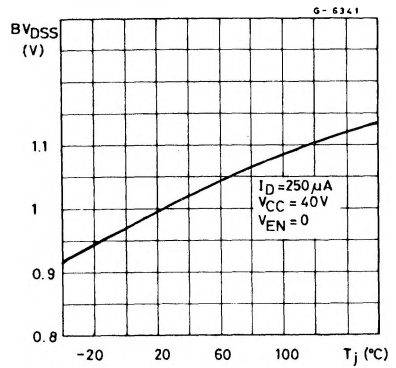


Figure 6 : Typical Source-drain Diode Forward Voltage.

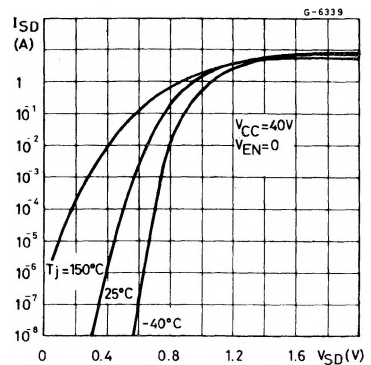


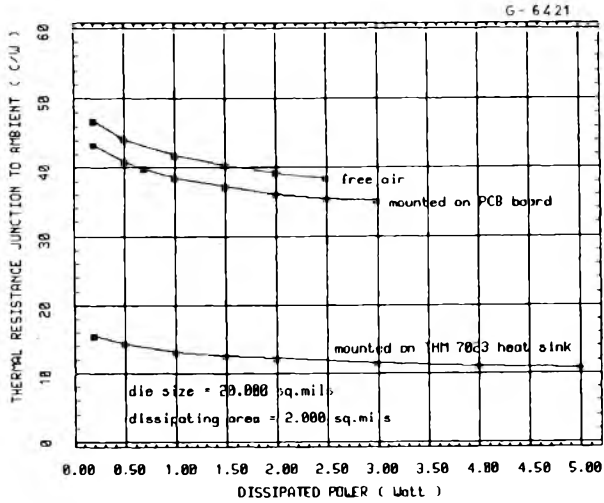
Figure 7 : $R_{thj-amb}$ vs. Dissipated Power (Multiwatt).(*) $R_{th} = 9^{\circ}\text{C/W}$

Figure 8 : Transient Thermal Resistance for Single Pulses (Multiwatt).

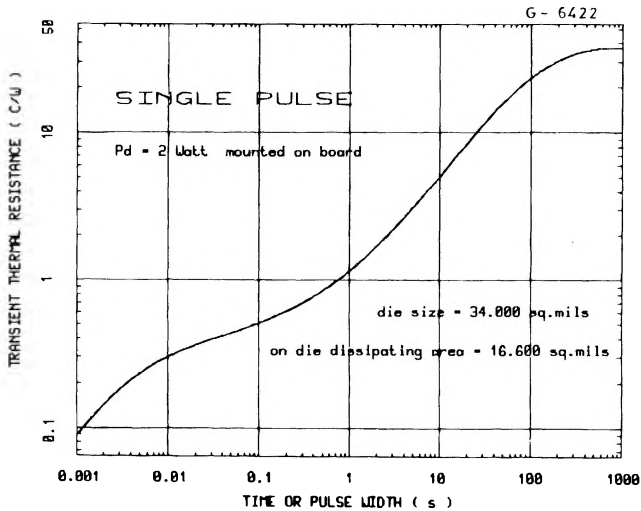


Figure 9 : Peak Transient Thermal Resistance vs. Pulse Width and Duty Cycle (Multiwatt).

