1 PRODUCT OVERVIEW

The KS57C21408/P21408 is a SAM47 core-based 4-bit CMOS single-chip microcontroller. It has a timer/counter and LCD drivers.

The KS57P21408 is especially suited for use in data bank, telephone and LCD general purpose.

It is built around the SAM47 core CPU and contains ROM, RAM, 39 I/O lines, programmable timer/counter, buzzer output, enough LCD dot matrix, and segment drive pins.

The KS57C21408/P21408 can be used for dedicated control functions in a variety of applications, and is especially designed for multi data bank, telephone and LCD game.

OTP

The KS57C21408 microcontroller is also available in OTP (One Time Programmable) version, KS57P21408. KS57P21408 microcontroller has an on-chip 8 K-byte one-time-programable EPROM instead of masked ROM. The KS57P21408 is comparable to KS57C21408, both in function and in pin configuration.

FEATURES SUMMARY

Memory

- 8192 × 8 bit program memory
- 5120 × 4 bit data memory
  108 × 5 bit display memory

39 I/O Pins

- Input: 6 pins
- I/O: 17 pins
- Output: maximum 16 pins for 1-bit level output (sharing with segment driver outputs)

8-Bit Timer

- Four internal timer functions

8-Bit Timer/Counter

- Programmable 8-bit timer
- External event counter
- Arbitrary clock output

Watch Timer

- 2/4/8/16 kHz Selective output for buzzer

Interrupts

- Three external vectored interrupts: INT0, INT1, INTP0
- Two internal vectored interrupts: INTB, INTT0
- Two quasi-interrupts: INTW, INT2

Memory Mapped I/O Structure

LCD Display

- 12 characters dot matrix display (5 x 7)
- 12 digit display (8 segments)
- 60 segments and 9 common pins

Power-Down Modes

- Idle: only CPU clock stops.
- Stop: Main–System clock and CPU clock stops.

Oscillation Sources

- Crystal, ceramic, or External RC for system clock
- Main system clock frequency: 0.4 MHz – 6MHz
- 32.768 kHz crystal oscillation circuit for subsystem clock.

Instruction Execution Times

- Various instruction cycle times for power saving.
- Main system clocks:
  0.95, 1.91, 15.3 µs at 4.19 MHz
  0.67, 1.33, 10.7 µs at 6 MHz
- Subsystem clocks: 122 µs at 32.768 kHz

Operating Voltage Range

- 2.0 V to 5.5 V

Package Type

- 100-pin QFP Package

BLOCK DIAGRAM

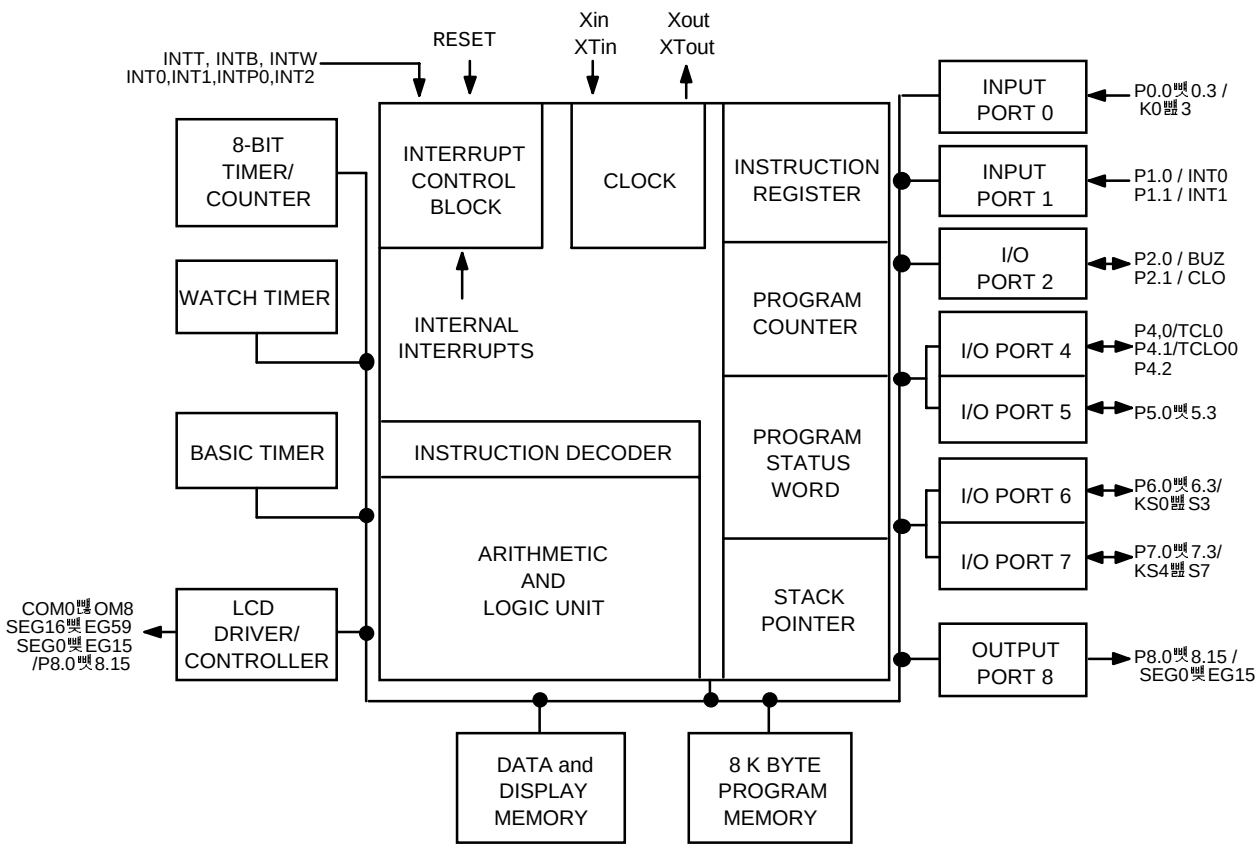

Figure 1-1. KS57C21408/P21408 Specified Block Diagram

PIN ASSIGNMENTS

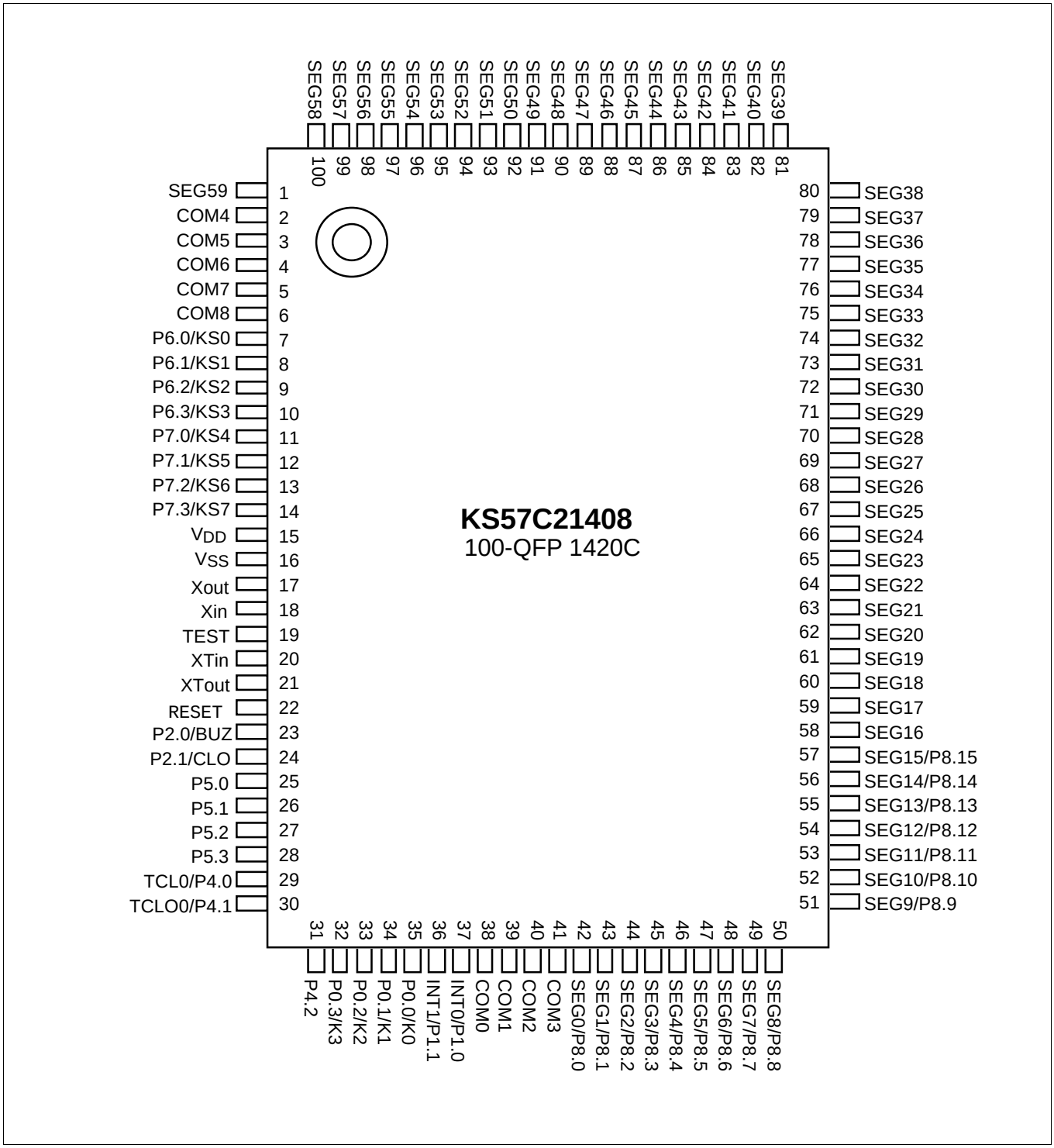

Figure 1-2. KS57C21408 Pin Assignment Diagram

PIN DESCRIPTIONS

Table 1-1. Pin Descriptions

Pin Name	Pin Type	Description	Circuit Type	Pin Number	Share Pin
P0.0 – P0.3	I	4-bit input port. 1 or 4-bit read/test possible. Pull-up register.	A-1	35–32	K0–K3
P1.0 P1.1	I	2-bit Input port. 1 or 2-bit read/test is possible, 2-bit unit pull-up resistor selectable by software.	A-3	37 36	INT0 INT1
P2.0 P2.1	I/O	2-bit I/O port. 1 or 2-bit read/write/test is possible. Each individual pin can be specified as input or output. 2-bit unit pull-up resistors selectable by software. Pull-up resistors are automatically disabled for output pins.	D	23 24	BUZ CLO
P4.0 P4.1 P4.2 P5.0–P5.3	I/O	4-bit I/O port. 1, 4 or 8-bit read/write/test possible. 4-pin unit can be specified as input or output. 4-bit unit pull-up resistors are selectable by software. Pull-up resistors are automatically disabled for output pins. Individual pins are software configurable as open-drain or push-pull output.	E E-1 E	29 30 31 25–28	TCL0 TCLO0
P6.0 – P6.3	I/O	4-bit I/O port. 1, 4 or 8-bit read/write/test possible. Each individual pin can be specified as input or output. 4-bit unit pull-up resistors selectable by software. Pull-up resistors are automatically disabled for output pins.	D-1	7–10	KS0 – KS3
P7.0 – P7.3		4-bit I/O port. 1, 4 or 8-bit read/write/test possible. 4-pin unit can be specified as input or output. 4-bit unit pull-up resistors are selectable by software. Pull-up resistors are automatically disabled for output pins.		11–14	KS4 – KS7
P8.0 – P8.15	O	4-bit controllable output. (Dual function as segment output pins)	H-9	42–57	SEG0 – SEG15
SEG16– SEG59		LCD segment display signal output.	H-10	58–100 ,1	–
SEG0 – SEG15		LCD segment display signal output.	H-9	42–57	P8.0 – P8.15
COM0 – COM8		LCD common signal output.	H-11	38–41 2–6	–
INT0 – INT1	I	Rising or falling edge detection selectable.		37–36	P1.0 –P1.1
KS0 – KS7	I/O	Quasi-interrupt input for falling edge detection.		7–14	P6.0 – P7.3
K0 – K3	I	Vector interrupt input K0 – K3: falling edge detection		35–32	P0.0 – P0.3

Table 1-1. Pin Descriptions (Continued)

Pin Name	Pin Type	Description	Circuit Type	Pin Num.	Share Pin
BUZ	I/O	2/4/8/16 kHz clock output for buzzer sound.	–	23	P2.0
CLO		Clock output	–	24	P2.1
X_{in}, X_{out}	–	Crystal, ceramic or RC oscillator pins for main system clock.	–	18, 17	–
XT_{in}, XT_{out}	–	Crystal oscillator pins for sub-system clock.	–	20, 21	–
TCL0	I/O	Timer0 clock input	–	29	P4.0
TCLO0	I/O	Timer0 clock output	–	30	P4.1
RESET	I	Reset input (active low).	B	22	–
V_{DD}	–	Power supply.	–	15	–
V_{SS}	–	Ground.	–	16	–
TEST	I	Test input: it must be connected to V_{SS}	–	19	–