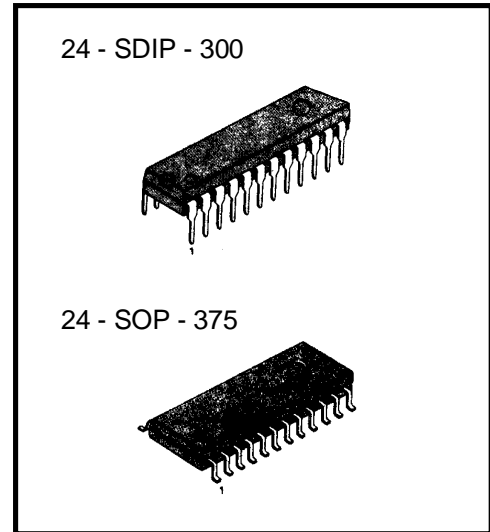


1. OUTLINE OF PRODUCT

The KS5520 is a single chip VLSI device which performs the on screen display function with sync separation of video composite signal and AFC is proposed.

It can choose total 256 characters and display up to 360 characters in a screen.

It can also select various built-in functions such as character color select, inverse, etc. These functions are compatible with all video systems including NTSC, PAL, SECAM.



2. FUNCTIONS

- On screen display
- Sync separator and sync detector
- AFC

3. FEATURES

- Screen structure : 360 (30 columns × 12 rows)
- Character structure : 12 × 18 dots
- Character types : 256 kinds of color characters
- Display position : 62 horizontal position
64 vertical position

4.2 ORDERING INFORMATION

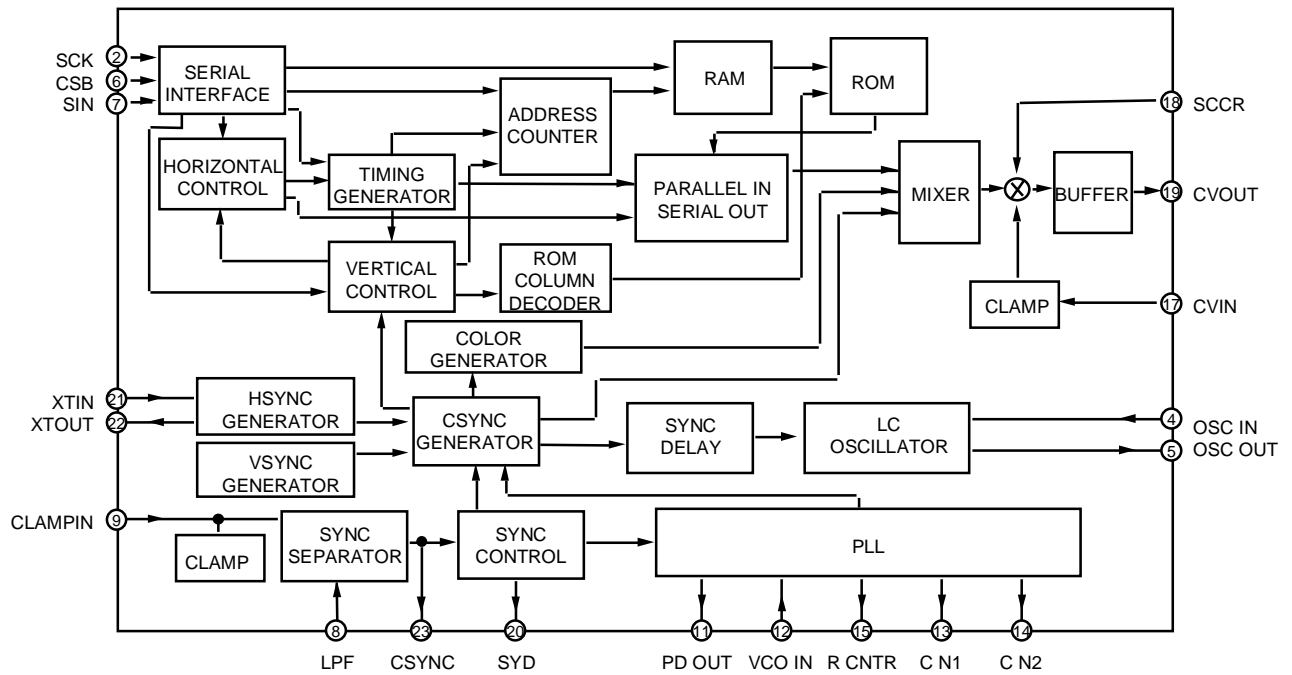
Device	Package	Operating Temperature
KS5520-XX	24-SDIP-300	- 20 ~ + 70°C
KS5520D-XX	24-SOP-375	- 20 ~ + 70°C

- Character size : 4 × 4 times of normal in both vertical and horizontal directions
- Blinking : controllable in character unit, blinking time also controllable
- Blanking : controllable in line units, blanking mode change possible
Blank color fill possible in character units (8 colors)
- Background coloring : 8 colors
- Character coloring : coloring of characters possible in blank mode
- Inverse character display : controllable in character units
- Synchronous ways : automatic selection of internal or external synchronization via MICOM control
- Built-in clamp, horizontal/vertical sync separator & sync detector circuit
- Sync detection sensitivity can be adjusted via MICOM control.
- Built-in analog horizontal/vertical sync PLL circuit
- Scroll & Box Drawing ability
- Half-Tone function ability
- NTSC / PAL / SECAM mode via MICOM control

4.1 OPTION CODE

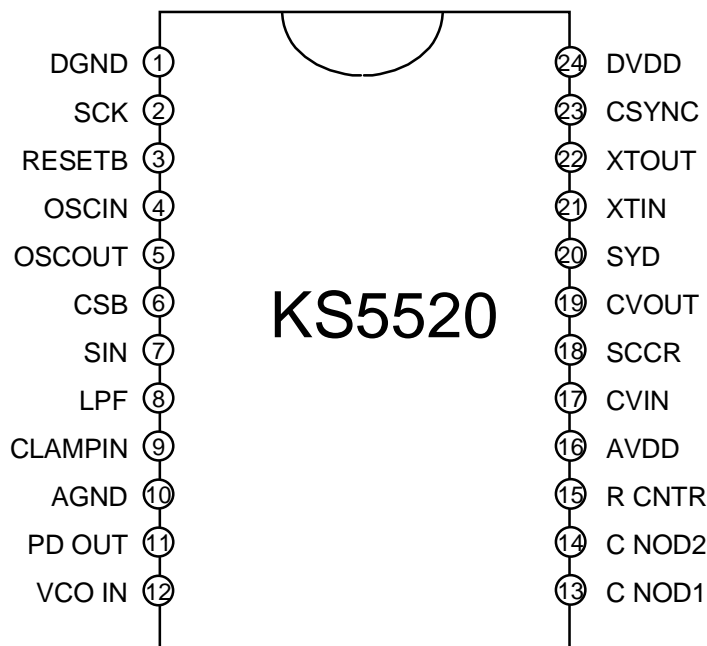
Code No.	Remark
KS5520-01	English, Russian, German, French, Spanish, Italian, Polish, Portuguese, Swedish Denish, Dutch, Esperanto, Vietnamese, Indonesian, Czechoslovak
KS5520D-04	English, Russian, German, French, Spanish, Italian, Polish, Portuguese, Swedish Denish, Dutch, Esperanto, Vietnamese, Indonesian, Czechoslovak, Greek

5. BLOCK DIAGRAM



6. PIN CONFIGURATION & DESCRIPTION

6.1 PIN CONFIGURATION



6.2 PIN DESCRIPTION

Pin No.	Symbol	I/O	Function
1	DGND	-	Digital Ground
2	SCK	I	Serial clock input. When CSB pin is low, then 16-bit serial data is inputted by controlling micom. Built-in pull-up resistor.
3	RESETB	I	Auto clear pin. If low, then all circuit is reset. Built-in pull-up resistor.
4	OSCIN	I	LC oscillation pin. Standard frequency is 9MHz & the horizontal start position and the horizontal size are controlled by the clock of oscillation block.
5	OSCOU	O	
6	CSB	I	While pin 6 is low, serial data input is active. Built - in pull-up resistor
7	SIN	I	Serial data input pin. Built-in pull-up resistor
8	LPF	I	LPF gets rid of the color signal in a video input signal.
9	CLAMPIN	I	Clamp input pin of composite video signal of 2Vpp
10	AGND	-	Analog ground
11	PD OUT	O	Phase detect output of analog PLL. Loop filter is formed by PD OUT and VCO IN.
12	VCO IN	I	VCO input pin of PLL
13	C NOD1	O	Capacitor node 1 of PLL VCO
14	C NOD2	O	Capacitor node 2 of PLL VCO
15	R CNTR	O	Resistor node of PLL VCO
16	AVDD	-	5V Analog VDD
17	CVIN	I	Composite video input pin
18	SCCR	I	When SECAM mode, color signal is mixed in the character level.
19	CVOUT	O	Composite video output pin

6.2 PIN DESCRIPTION (Continued)

Pin No.	Symbol	I/O	Function
20	SYD	O	H-sync detect output pin. If sync exists, then high if not, low
21	XTIN	I	X-tal input / output pin NTSC : 14.31818 MHz, PAL : 17.734475MHz
22	XTOUT	O	
23	CSYNC	O	When external, C-sync separator output is out, when internal, then internal C-sync is outputted.
24	DVDD	-	5V Digital VDD

7. ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

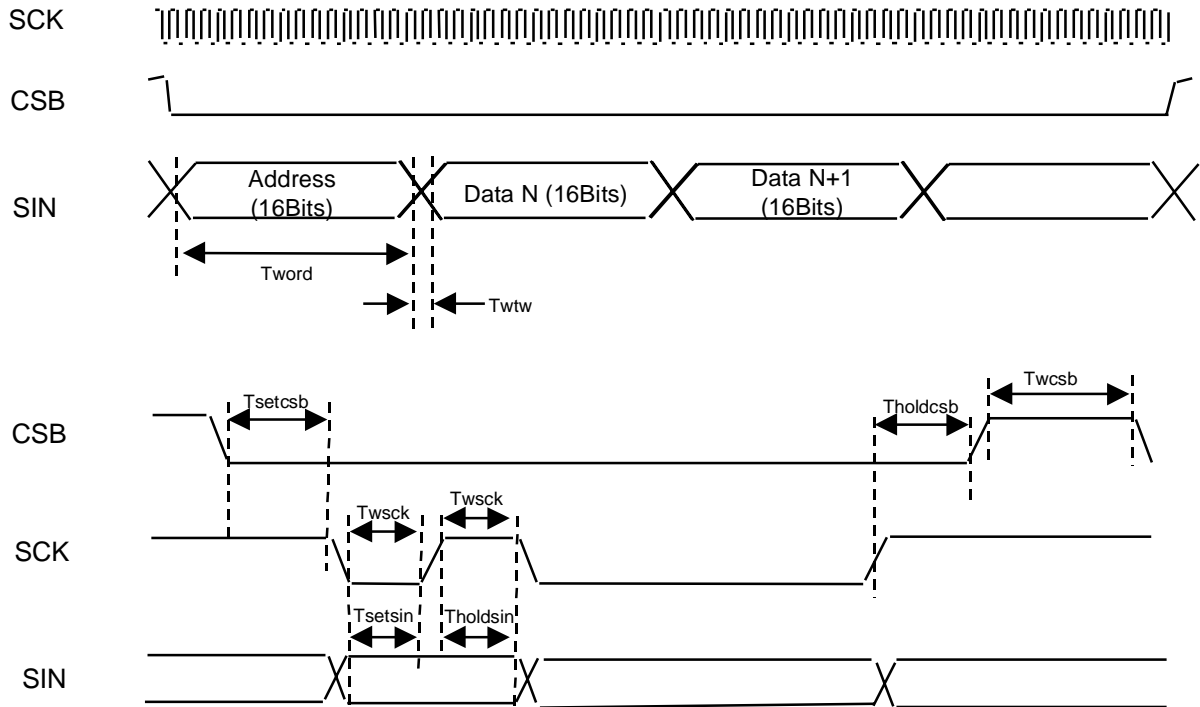
Characteristics	Symbol	Value	Unit
Supply Voltage	VDD	3.0 ~ 7.0	V
Input Voltage	VIN	$V_{SS} - 0.3 \leq V_{IN} \leq V_{DD} + 0.3$	V
Power Dissipation	PD	200	mW
Operating Temperature	Topr	- 20 ~ + 70	°C
Storage Temperature	Tstg	- 40 ~ + 125	°C

8. ELECTRICAL CHARACTERISTICS (Ta = 25°C, AVDD = DVDD = 5V)

Characteristics	Symbol	Min	Typ	Max	Unit
Operating Voltage	VDD	4.75	5.00	5.25	V
Operating Current	Icc	20	40	60	mA
Input High Voltage	VIH	0.8VDD	-	-	V
Input Low Voltage	VIL	-	-	0.2VDD	V
Output High Voltage (2mA drive)	VOH	0.7VDD	-	-	V
Output Low Voltage (2mA drive)	VOL	-	-	0.3VDD	V
Pin8 LPF Voltage	Vp8	2.15	2.35	2.55	V
Pin9 Clamp Voltage	Vp9	1.25	1.45	1.65	V
Pin15 R_CNTR Voltage	Vp15	2.35	2.50	2.65	V
Pin17 Clamp Voltage	Vp17	0.60	0.80	1.00	V
Buffer Gain	Vp19G	1.80	2.00	2.20	V
LC Oscillation Frequency	Fosc	8.0	9.0	10.0	MHz
Hsync Duty	Fh_duty	250	550	850	nS
Hsync Frequency	H_fre	15.5	15.7	15.9	KHz
X-tal Oscillation Frequency	Fp22	14.1	14.3	14.5	MHz
Sync Separation Voltage	Vse	0.10	0.25	0.40	V
Blueback Sync Tip Level	Vbst	0.50	0.80	1.10	V
Blueback Pedestal Level	Vbpd	1.10	1.40	1.70	V
Blueback Color Burst Level High	Vcbh	1.40	1.70	2.00	V
Blueback Color Burst Level Low	Vcbl	0.80	1.10	1.40	V
Blueback Color Level High	Vbch	2.30	2.60	2.90	V
Blueback Color Level Low	Vbcl	1.30	1.60	1.90	V
Blueback Blank Level High	Vblkh	1.40	1.70	2.00	V
Blueback Blank Level Low	Vblk1	1.10	1.40	1.70	V
Blueback Character Level High	Vchh	2.40	2.70	3.00	V
Blank Color Off Level	Vbcof	1.10	1.40	1.70	V
Box White Level	Vbwl	2.20	2.50	2.80	V
Box Black Level	Vbbl	1.10	1.40	1.70	V
HalfTone Level	Vhalf	1.80	2.10	2.40	V
VCO Input Voltage	Vvco	2.30	2.50	2.70	V
AFC Freerun Frequency	Ffr	15.5	15.7	15.9	KHz
AFC Lock Range High	Falh	200	300	400	Hz
AFC Lock Range Low	Fall	-	-	-500	Hz

Note 1 : Specifications are subject to change without notice.

9. TIMING DIAGRAM



ITEM	SYMBOL	LIMITS			UNIT
		MIN	TYP	MAX	
SCK Width	Twsck	200	-	-	nsec
CSB Width	Twcsb	1	-	-	usec
CSB Setup Time	Tsetcsb	200	-	-	nsec
CSB Hold Time	Tholdcsb	2	-	-	usec
SIN Setup Time	Tsetsin	200	-	-	nsec
SIN Hold Time	Tholdsin	200	-	-	nsec
1 Word Write Time	Tword	10	-	-	usec
Word To Word Time	Twtw	1	-	-	usec

10. MEMORY STRUCTURE

It consists of 360*16 bits SRAM, 256 font ROM and 5 mode control register.

	DAF	DAE	DAD	DAC	DAB	DAA	DA9	DA8	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0
0	Box_Inv	Box_1	Box_0	R	G	B	Invert	Blink	C7	C6	C5	C4	C3	C2	C1	C0
1	* (Note)	* (Note)	* (Note)	* (Note)	* (Note)	* (Note)	* (Note)	* (Note)	Character Code (ROM Address)							
2																
3																
.																
.																
.																
.																
.																
.																
.																
.																
.																
.																
.																
.																
357																
358																
359	Box_Inv	Box_1	Box_0	R	G	B	Invert	Blink	C7	C6	C5	C4	C3	C2	C1	C0
360	0	0	Half_Tone	Blink_1	Blink_0	Blink_Time	HZ_21	HZ_20	HZ_11	HZ_10	HP_5	HP_4	HP_3	HP_2	HP_1	HP_0
361	0	Ext_fsc	Blank_Level	Scroll_Time	Scroll_On	Inter_nal	VZ_21	VZ_20	VZ_11	VZ_10	VP_5	VP_4	VP_3	VP_2	VP_1	VP_0
362	0	RAM_Erase	Disp_On	P626/P628	Inlace/Non-	Secam	NTSC/PAL	Blk_1	Blk_0	Blk_Col	C_Lev1	R_Lev0	R_Lev0	R_Cntr2	R_Cntr1	R_Cntr0
363	0	0	0	All_Blank	DSP_B	DSP_A	DSP_9	DSP_8	DSP_7	DSP_6	DSP_5	DSP_4	DSP_3	DSP_2	DSP_1	DSP_0
364	0	Fil2	Fil1	Fil0	Fih3	Fih2	Fih1	Fih0	Fcl3	Fcl2	Fcl1	Fcl0	Fch3	Fch2	Fch1	Fch0

* (Note) : same as above.

< Raster Color Level Control > (Control Register 362 (16AH))

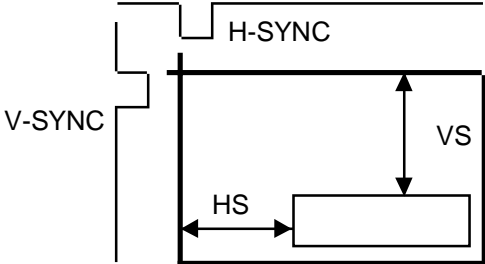
DA4(Lev 1)	DA3(Lev 0)	Raster Color Level `H`	Raster Color Level `L`	Remark
0	0	2.6V	1.6V	Level 0
0	1	2.2V	1.4V	Level 1
1	0	2.2V	1.4V	Level 1
1	1	2.0V	1.3V	Level 2

CONTROL REGISTER

1) Register 360 (168H)

DA0 ~ DAD	Register	ContentSs		Remark																			
		State	Functions																				
0	HP0	0	$HS = Tc * \{ 4 * \sum_{n=0}^5 (HPn * 2^n) + N \}$ $Tc : \text{osc. period (} 1/9 \text{ MHz = 111 nsec)}$ <table border="1" style="margin: 10px auto;"> <tr> <td>HSZ11</td> <td>HSZ10</td> <td rowspan="2">N</td> </tr> <tr> <td>HSZ21</td> <td>HSZ20</td> </tr> <tr> <td>0</td> <td>0</td> <td>9</td> </tr> <tr> <td>0</td> <td>1</td> <td>10</td> </tr> <tr> <td>1</td> <td>0</td> <td>11</td> </tr> <tr> <td>1</td> <td>1</td> <td>12</td> </tr> </table>	HSZ11	HSZ10	N	HSZ21	HSZ20	0	0	9	0	1	10	1	0	11	1	1	12	Horizontal Start Position		
		HSZ11		HSZ10	N																		
HSZ21	HSZ20																						
0	0	9																					
0	1	10																					
1	0	11																					
1	1	12																					
1	1																						
2	HP2	0		<table border="1" style="margin: 10px auto;"> <tr> <td>HSZ11</td> <td>HSZ10</td> <td rowspan="2">N</td> </tr> <tr> <td>HSZ21</td> <td>HSZ20</td> </tr> <tr> <td>0</td> <td>0</td> <td>9</td> </tr> <tr> <td>0</td> <td>1</td> <td>10</td> </tr> <tr> <td>1</td> <td>0</td> <td>11</td> </tr> <tr> <td>1</td> <td>1</td> <td>12</td> </tr> </table>	HSZ11	HSZ10	N	HSZ21	HSZ20	0	0	9	0	1	10	1	0	11	1	1	12		
		HSZ11			HSZ10	N																	
HSZ21	HSZ20																						
0	0	9																					
0	1	10																					
1	0	11																					
1	1	12																					
1	1																						
3	HP3	0	<table border="1" style="margin: 10px auto;"> <tr> <td>HSZ11</td> <td>HSZ10</td> <td rowspan="2">N</td> </tr> <tr> <td>HSZ21</td> <td>HSZ20</td> </tr> <tr> <td>0</td> <td>0</td> <td>9</td> </tr> <tr> <td>0</td> <td>1</td> <td>10</td> </tr> <tr> <td>1</td> <td>0</td> <td>11</td> </tr> <tr> <td>1</td> <td>1</td> <td>12</td> </tr> </table>		HSZ11	HSZ10	N	HSZ21	HSZ20	0	0	9	0	1	10	1	0	11	1	1	12		
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HSZ21	HSZ20																						
0	0	9																					
0	1	10																					
1	0	11																					
1	1	12																					
1	1																						
4	HP4	0		<table border="1" style="margin: 10px auto;"> <tr> <td>HSZ11</td> <td>HSZ10</td> <td rowspan="2">N</td> </tr> <tr> <td>HSZ21</td> <td>HSZ20</td> </tr> <tr> <td>0</td> <td>0</td> <td>9</td> </tr> <tr> <td>0</td> <td>1</td> <td>10</td> </tr> <tr> <td>1</td> <td>0</td> <td>11</td> </tr> <tr> <td>1</td> <td>1</td> <td>12</td> </tr> </table>	HSZ11	HSZ10	N	HSZ21	HSZ20	0	0	9	0	1	10	1	0	11	1	1	12		
		HSZ11			HSZ10	N																	
HSZ21	HSZ20																						
0	0	9																					
0	1	10																					
1	0	11																					
1	1	12																					
1	1																						
5	HP5	0	<table border="1" style="margin: 10px auto;"> <tr> <td>HSZ11</td> <td>HSZ10</td> <td rowspan="2">N</td> </tr> <tr> <td>HSZ21</td> <td>HSZ20</td> </tr> <tr> <td>0</td> <td>0</td> <td>9</td> </tr> <tr> <td>0</td> <td>1</td> <td>10</td> </tr> <tr> <td>1</td> <td>0</td> <td>11</td> </tr> <tr> <td>1</td> <td>1</td> <td>12</td> </tr> </table>		HSZ11	HSZ10	N	HSZ21	HSZ20	0	0	9	0	1	10	1	0	11	1	1	12		
		HSZ11			HSZ10	N																	
HSZ21	HSZ20																						
0	0	9																					
0	1	10																					
1	0	11																					
1	1	12																					
1	1																						
6	HZ10	0		<table border="1" style="margin: 10px auto;"> <tr> <td>HZ10 / HZ11</td> <td>0</td> <td>1</td> </tr> <tr> <td>0</td> <td>1X</td> <td>2X</td> </tr> <tr> <td>1</td> <td>3X</td> <td>4X</td> </tr> </table>	HZ10 / HZ11	0	1	0	1X	2X	1	3X	4X	1st line horizontal character size control									
		HZ10 / HZ11			0	1																	
0	1X	2X																					
1	3X	4X																					
1	1																						
7	HZ11	0			<table border="1" style="margin: 10px auto;"> <tr> <td>HZ10 / HZ11</td> <td>0</td> <td>1</td> </tr> <tr> <td>0</td> <td>1X</td> <td>2X</td> </tr> <tr> <td>1</td> <td>3X</td> <td>4X</td> </tr> </table>	HZ10 / HZ11	0	1	0	1X	2X	1	3X		4X	1st line horizontal character size control							
		HZ10 / HZ11				0	1																
0	1X	2X																					
1	3X	4X																					
1	1																						
8	HZ20	0	<table border="1" style="margin: 10px auto;"> <tr> <td>HZ20 / HZ21</td> <td>0</td> <td>1</td> </tr> <tr> <td>0</td> <td>1X</td> <td>2X</td> </tr> <tr> <td>1</td> <td>3X</td> <td>4X</td> </tr> </table>	HZ20 / HZ21		0	1	0	1X	2X	1	3X	4X	2nd ~ 12th line horizontal character size control									
		HZ20 / HZ21		0		1																	
0	1X	2X																					
1	3X	4X																					
1	1																						
9	HZ21	0		<table border="1" style="margin: 10px auto;"> <tr> <td>HZ20 / HZ21</td> <td>0</td> <td>1</td> </tr> <tr> <td>0</td> <td>1X</td> <td>2X</td> </tr> <tr> <td>1</td> <td>3X</td> <td>4X</td> </tr> </table>	HZ20 / HZ21	0	1	0	1X	2X	1	3X	4X		2nd ~ 12th line horizontal character size control								
		HZ20 / HZ21			0	1																	
0	1X	2X																					
1	3X	4X																					
1	1																						
A	Blink Time	0	Blink Time = 1 sec		Blink Time Control																		
		1	Blink Time = 0.5 sec																				
B	Blink 0	0	<table border="1" style="margin: 10px auto;"> <tr> <td>Blink0 / Blink1</td> <td>0</td> <td>1</td> </tr> <tr> <td>0</td> <td>Off</td> <td>Duty 25%</td> </tr> <tr> <td>1</td> <td>Duty 50%</td> <td>Duty 75%</td> </tr> </table>		Blink0 / Blink1	0	1	0	Off	Duty 25%	1	Duty 50%	Duty 75%	Blinking Duty Control									
		Blink0 / Blink1		0	1																		
0	Off	Duty 25%																					
1	Duty 50%	Duty 75%																					
1	1																						
C	Blink 1	0	<table border="1" style="margin: 10px auto;"> <tr> <td>Blink0 / Blink1</td> <td>0</td> <td>1</td> </tr> <tr> <td>0</td> <td>Off</td> <td>Duty 25%</td> </tr> <tr> <td>1</td> <td>Duty 50%</td> <td>Duty 75%</td> </tr> </table>	Blink0 / Blink1	0	1	0	Off	Duty 25%	1	Duty 50%	Duty 75%	Blinking Duty Control										
		Blink0 / Blink1		0	1																		
0	Off	Duty 25%																					
1	Duty 50%	Duty 75%																					
1	1																						
D	Half-tone	0	Half-tone Off	Half-tone On/Off																			
		1	Half-tone On																				

2) Register 361(169H)

DA0 ~ DAE	Register	Contents		Remark									
		State	Functions										
0	VP0	0	$VS = H * \{ 4 * \sum_{n=0}^5 (VPn * 2^n) + 3 \}$ H : horizontal synchronous pulse time 	Vertical Start Position									
		1											
1	VP1	0											
		1											
2	VP2	0											
		1											
3	VP3	0											
		1											
4	VP4	0											
		1											
5	VP5	0											
		1											
6	VZ10	0	<table border="1" data-bbox="651 1102 1149 1258"> <tr> <td>VZ11 \ VZ10</td> <td>0</td> <td>1</td> </tr> <tr> <td>0</td> <td>1X</td> <td>2X</td> </tr> <tr> <td>1</td> <td>3X</td> <td>4X</td> </tr> </table>	VZ11 \ VZ10	0	1	0	1X	2X	1	3X	4X	1st line vertical character size control
		VZ11 \ VZ10		0	1								
0	1X	2X											
1	3X	4X											
1													
7	VZ11	0											
		1											
8	VZ20	0	<table border="1" data-bbox="651 1310 1149 1467"> <tr> <td>VZ21 \ VZ20</td> <td>0</td> <td>1</td> </tr> <tr> <td>0</td> <td>1X</td> <td>2X</td> </tr> <tr> <td>1</td> <td>3X</td> <td>4X</td> </tr> </table>	VZ21 \ VZ20	0	1	0	1X	2X	1	3X	4X	2nd ~ 12th line vertical character size control
		VZ21 \ VZ20		0	1								
0	1X	2X											
1	3X	4X											
1													
9	VZ21	0											
		1											
A	Internal	0	External SYNC	External / Internal Mode									
		1	Internal SYNC										
B	Scroll On	0	Scroll Off	Scroll Display Control									
		1	Scroll On										
C	Scroll Time	0	Scroll Time 0.5 sec	Scroll Time Control									
		1	Scroll Time 1 sec										
D	Blank L Level	0	Blank Low Level 0 (1.4V)	Blank Color Low Level Control									
		1	Blank Low Level 1 (1.8V)										
E	Ext fsc	0	External 4fsc X-TAL (Pin 21,22)	External fsc Clock Input									
		1	External fsc input to Pin 21(*Only for IC Test)										

3) Register 362 (16AH)

DA0 ~ DAE	Register	Contents				Remark				
		State	Functions							
0	R_cntr0	0	Cntr2	Cntr1	Cntr0	NTSC	PAL	Raster Color Control		
		1	0	0	0	Red	Red			
			0	0	1	Blue	G + Y			
1	R_cntr1	0	0	1	0	B + G	B + G		Raster Color Control	
		1	0	1	1	Yellow	Blue			
			1	0	0	Orange	Magenta			
2	R_cntr2	0	1	0	1	Magenta	Yellow			Raster Color Control
		1	1	1	0	Cyan	Green			
			1	1	1	Gray	Gray			
3	R_lev0	0	Lev 0		0	1	Raster Color Level Control			
		1	Lev 1		0	1				
4	R_lev1	0	0	Level 0	Level 1	Level 1				
		1	1	Level 1	Level 2					
5	C_level	0	Character Level 1 (2.7V)				Character Level Control			
		1	Character Level 2 (2.5V)							
6	Blank Color	0	Blank Color Off				When SECAM, Blank Color Off is not used.			
		1	Blank Color On							
7	BLK0	0	Blank Mode Select by Controlling the Data of Register 363 (16BH)							
		1								
8	BLK1	0								
		1								
9	NTSC /PAL	0	NTSC				Color System Select			
		1	PAL							
A	SECAM	0	NTSC or PAL							
		1	SECAM							
B	Interlace /Non-I	0	Interlace				Scanning Type Control			
		1	Non-Interlace							
C	P626/ P628	0	PAL 1 Field = 626H				PAL Mode 1 Field Control			
		1	PAL 1 Field = 628H							
D	DSP ON	0	Display Off				Character Display Control			
		1	Display On							
E	RAM ERS	0	RAM is not erased.							
		1	RAM is erased.							

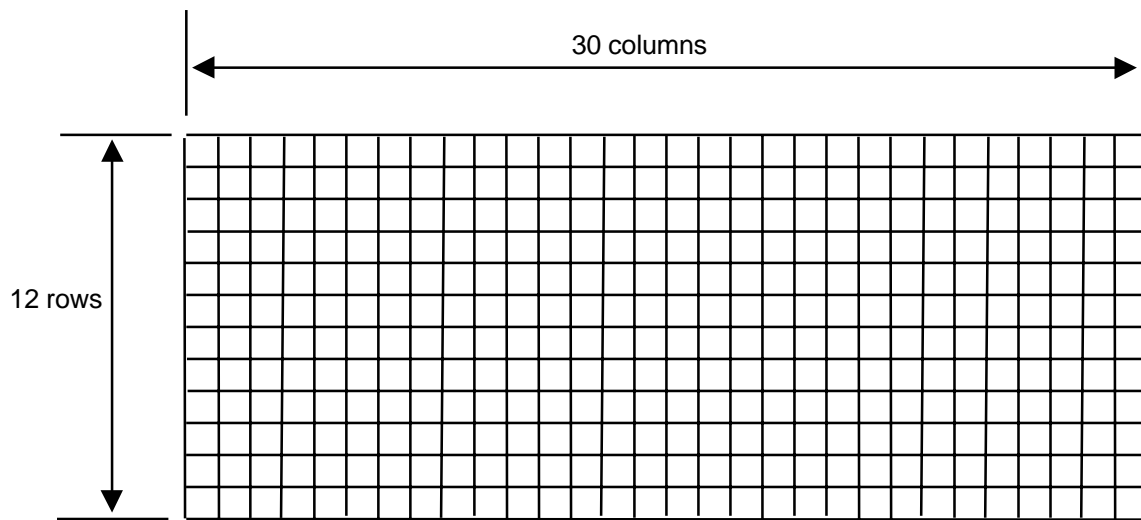
4) Register 363 (16BH)

DA0 ~ DAC	Register	Contents		Remark																																				
		State	Functions																																					
0	DSP0	0	1st line BLANK mode select	<table border="1"> <thead> <tr> <th>BLK1</th> <th>BLK0</th> <th>DSP</th> <th>Blank Mode</th> </tr> </thead> <tbody> <tr> <td rowspan="4">0</td> <td rowspan="2">0</td> <td>0</td> <td>Blank Off</td> </tr> <tr> <td>1</td> <td>O*</td> </tr> <tr> <td rowspan="2">1</td> <td>0</td> <td>C*</td> </tr> <tr> <td>1</td> <td>O*</td> </tr> <tr> <td rowspan="4">1</td> <td rowspan="2">0</td> <td>0</td> <td>O*</td> </tr> <tr> <td>1</td> <td>R*</td> </tr> <tr> <td rowspan="2">1</td> <td>0</td> <td>R*</td> </tr> <tr> <td>1</td> <td>C*</td> </tr> <tr> <td colspan="3">ALL BLK = 1</td> <td>All Blank</td> </tr> </tbody> </table> <table border="1"> <tbody> <tr> <td>C*</td> <td>Character Blank</td> </tr> <tr> <td>O*</td> <td>Outline Blank</td> </tr> <tr> <td>R*</td> <td>Raster Blank</td> </tr> </tbody> </table>	BLK1	BLK0	DSP	Blank Mode	0	0	0	Blank Off	1	O*	1	0	C*	1	O*	1	0	0	O*	1	R*	1	0	R*	1	C*	ALL BLK = 1			All Blank	C*	Character Blank	O*	Outline Blank	R*	Raster Blank
		BLK1			BLK0	DSP	Blank Mode																																	
0	0	0	Blank Off																																					
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		1																																						
2	DSP2	0	3rd line BLANK mode select																																					
		1																																						
3	DSP3	0	4th line BLANK mode select																																					
		1																																						
4	DSP4	0	5th line BLANK mode select																																					
		1																																						
5	DSP5	0	6th line BLANK mode select																																					
		1																																						
6	DSP6	0	7th line BLANK mode select																																					
		1																																						
7	DSP7	0	8th line BLANK mode select																																					
		1																																						
8	DSP8	0	9th line BLANK mode select																																					
		1																																						
9	DSP9	0	10th line BLANK mode select																																					
		1																																						
A	DSPA	0	11th line BLANK mode select																																					
		1																																						
B	DSPB	0	12th line BLANK mode select																																					
		1																																						
C	All	0	Depend on BLK0, BLK1																																					
	BLK	1	All screen blank except character																																					

5) Register 364 (16CH)

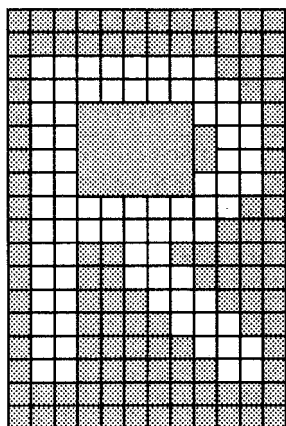
DA0 ~ DAE	Register	Contents		Remark		
		State	Functions			
0	Fch0	0	$Fch = 30 * \left\{ \sum_{n=0}^3 Fchn * 512 * 2^n \right\} \text{ Hz}$ Capture Range `H` = 15.36 kHz ~ 230.4 kHz	Sync Detect Capture Range High Sensitivity Control		
		1				
1	Fch1	0				
		1				
2	Fch2	0				
		1				
3	Fch3	0				
		1				
4	Fcl0	0			$Fcl = 30 * \left\{ \sum_{n=0}^3 Fchn * 64 * 2^n \right\} \text{ Hz}$ Capture Range `L` = 1.92 kHz ~ 28.8 kHz	Sync Detect Capture Range Low Sensitivity Control
		1				
5	Fcl1	0				
		1				
6	Fcl2	0				
		1				
7	Fcl3	0				
		1				
8	Flh0	0	$Flh = 30 * \left\{ \sum_{n=0}^3 Fchn * 512 * 2^n \right\} \text{ Hz}$ Locking Range `H` = 15.36 kHz ~ 230.4 kHz	Sync Detect Locking Range High Sensitivity Control		
		1				
9	Flh1	0				
		1				
A	Flh2	0				
		1				
B	Flh3	0				
		1				
C	FI0	0			$FI = 30 * \left\{ \sum_{n=0}^2 Fchn * 64 * 2^n \right\} \text{ Hz}$ Locking Range `L` = 1.92 kHz ~ 13.44 kHz	Sync Detect Locking Range Low Sensitivity Control
		1				
D	FI1	0				
		1				
E	FI2	0				
		1				

11. SCREEN STRUCTURE

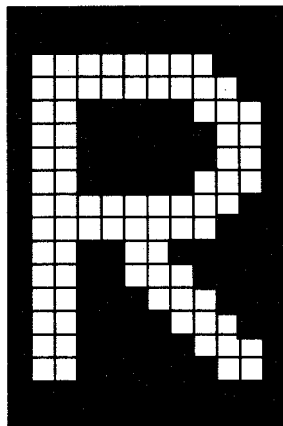


TV Screen

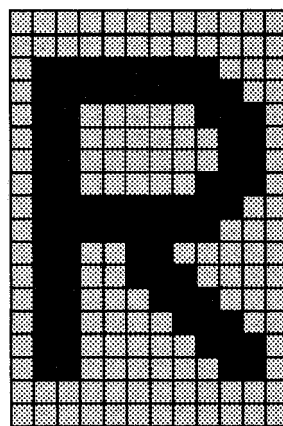
12. BLANK MODE



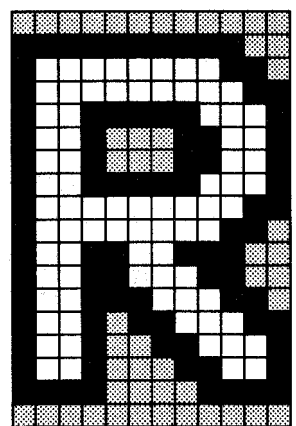
Blank Off



Raster Blank

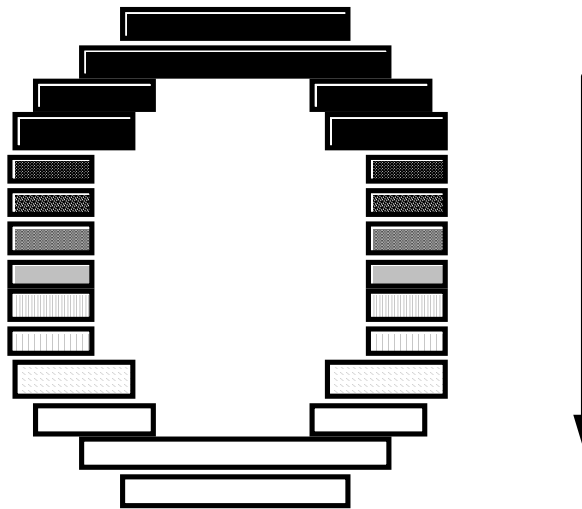


Character Blank



Outline Blank

13. SCROLL FUNCTION



When control register 361, scroll bit (DAB bit) is high, character display on/off from top to down slowly about 0.5 sec or 1 sec. (also controlled by register setting)

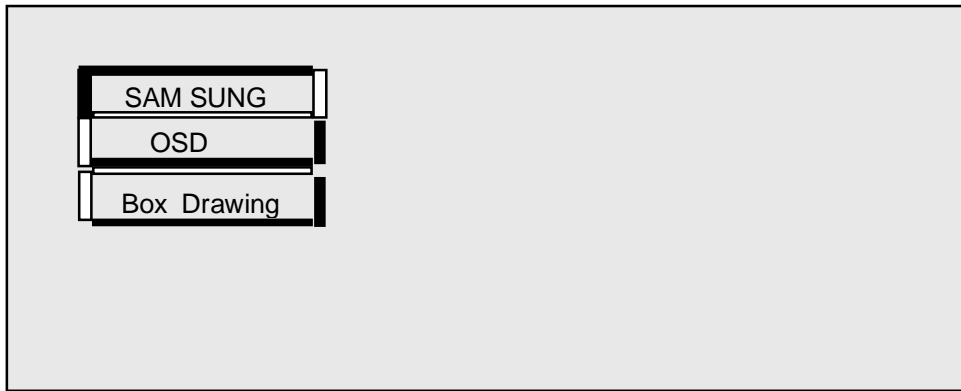
14. HALF-TONE FUNCTION



TV Screen

When control register 360, half tone bit (DAD bit) is high, character display with half luminance level and also display background screen.

15. BOX DRAWING FUNCTION



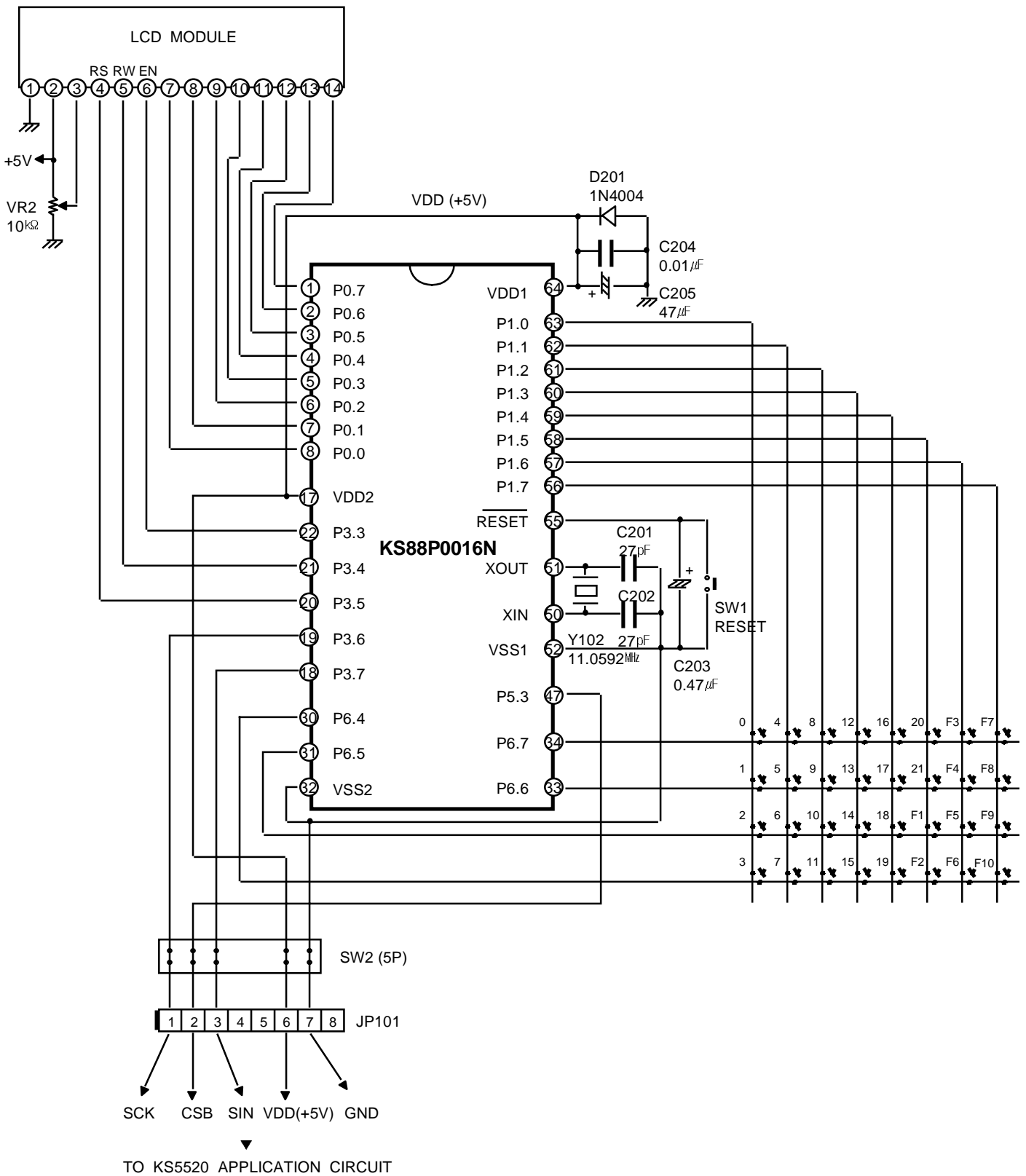
TV Screen

It can draw rectangle box. If you want to concave display, top and left side of characters are drawn black color, bottom and right side of characters are drawn white color and also want to convex display, character colors are vice versa.

It is all controlled by each RAM attribution bit, that is box1 (DAE), box0 (DAD) and box_inv (DAF).

		box0	
		0	1
box1	0	BOX OFF	
	1		

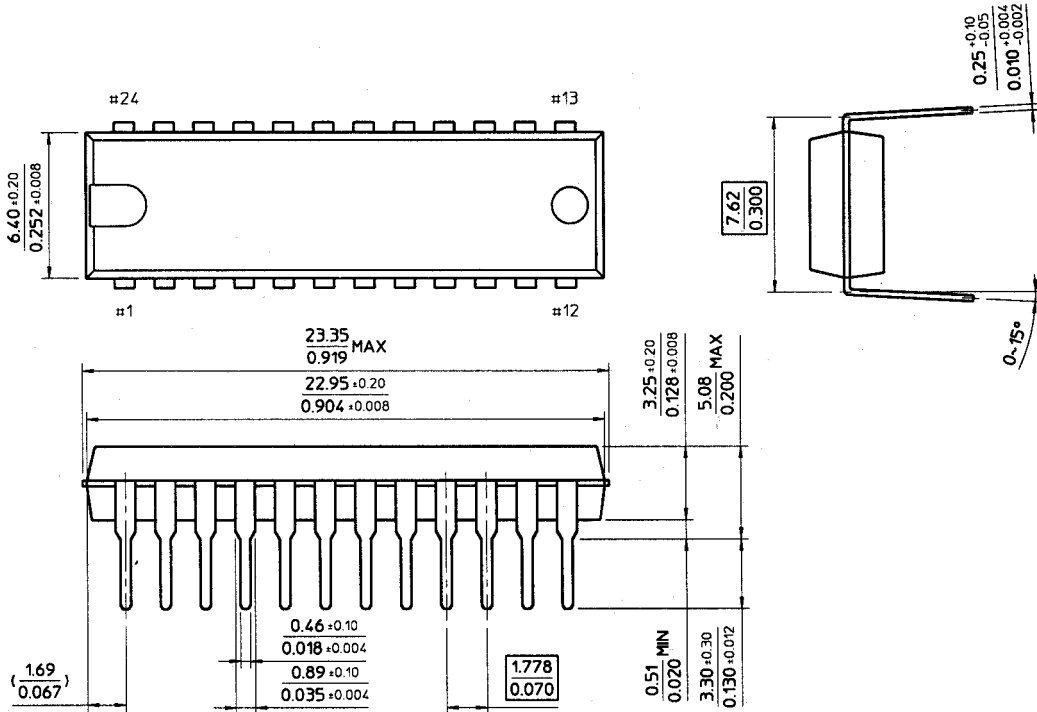
16-2. APPLICATION CIRCUIT (CONTROLLER BLOCK)



17. PACKAGE DIMENSIONS

24-SDIP-300

Dimensions in Millimeters



MEMO

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