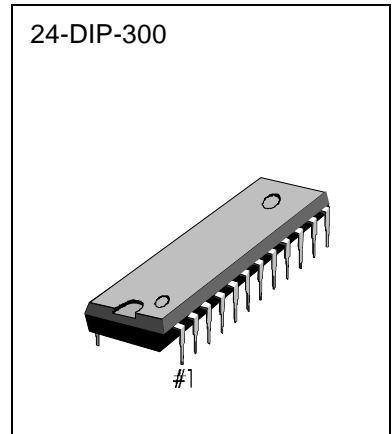


OVERVIEW

The KS2501 is used to display some characters or symbols on a screen of monitor. Basically, the operation is to control the internal memory on chip and generate the R,G,B signals for some characters or symbols. The R,G,B signals are synchronized with the horizontal sync. Then the R,G,B signals are mixed with the main video signal in the Video Amp IC.

The font data for characters or symbols are stored in the internal ROM. This stored data are accessed and controlled by the control data from a micro controller. The control data are transmitted through the I²C bus. All timing control signals including the system clock are synchronized with the horizontal sync. Therefore there is a PLL circuitry on chip.



FEATURES

- 464 ROM fonts (448 standard fonts + 16 Multi-color fonts)
- Full Screen Memory Architecture
- Wide range PLL available (15 kHz ~ 120 kHz)
- Programmable vertical height of character
- Programmable vertical and horizontal positioning
- Character color selection up to 16 different colors
- Programmable background color (Up to 16 colors)
- Character blinking, bordering and shadowing
- Color blinking
- Character scrolling
- Fade-in and fade-out
- Row to row spacing control
- Window outline and shadowing
- Box drawing
- Character sizing up to four times
- 8 PWM DAC channels with 8-bit resolution
- 96 MHz pixel frequency from on-chip PLL

ORDERING INFORMATION

Device	Package	Operating Temperature
KS2501	24-DIP-300	0°C ~ 70°C

BLOCK DIAGRAM

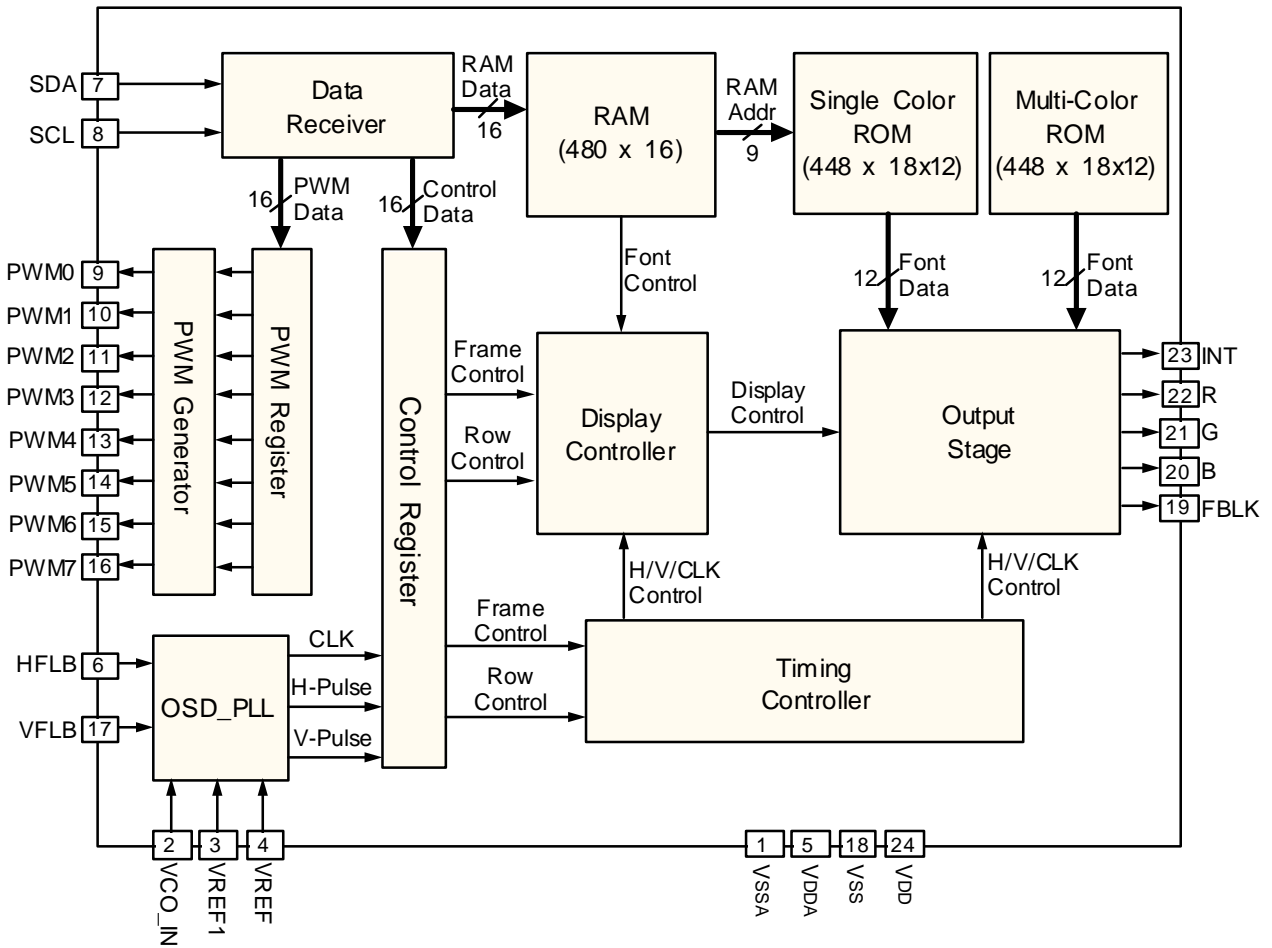


Figure 1. Functional Block Diagram

PIN CONFIGURATIONS

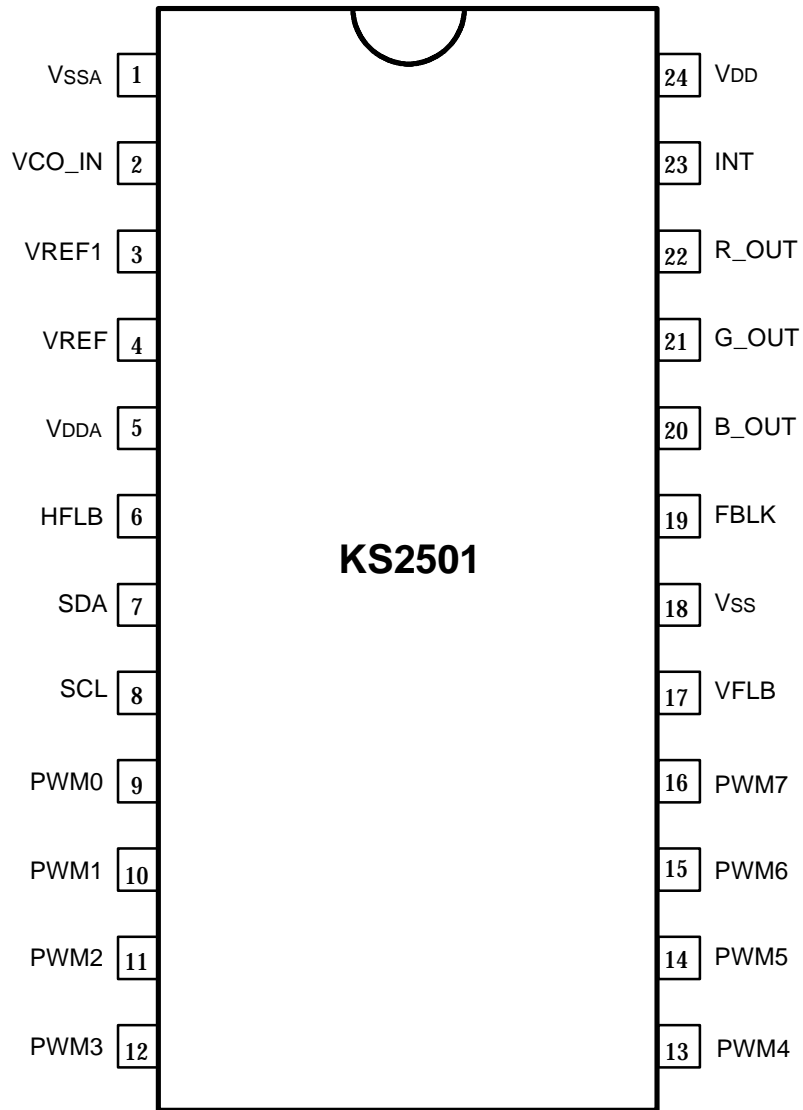


Figure 2. Pin Configurations

PIN DESCRIPTIONS

Table 1. Pin Descriptions

Pin No.	Signal	Active	I/O	Description
1	V _{SSA}	-	-	Ground (Analog Part)
2	VCO_IN	-	Input	This voltage is generated at the external loop filter and goes into the input stage of the VCO.
3	VREF1	-	Input	1.26 V DC Voltage from the Bandgap Reference. Connected to ground through a resistor to make internal reference current (Typical 36 K Ω for 27 μ A)
4	VREF	-	Input	Bandgap Reference Voltage (Typical 1.26 V)
5	V _{DDA}	-	-	+5 V Supply Voltage for Analog Part
6	HFLB	Low	Input	Horizontal Flyback Signal
7	SDA	-	In/Out	Serial Data (I ² C)
8	SCL	-	In/Out	Serial Clock (I ² C)
9	PWM 0	-	Output	PWM DAC 0 Output
10	PWM 1	-	Output	PWM DAC 1 Output
11	PWM 2	-	Output	PWM DAC 2 Output
12	PWM 3	-	Output	PWM DAC 3 Output
13	PWM 4	-	Output	PWM DAC 4 Output
14	PWM 5	-	Output	PWM DAC 5 Output
15	PWM 6	-	Output	PWM DAC 6 Output
16	PWM 7	-	Output	PWM DAC 7 Output
17	VFLB	Low	Input	Vertical Flyback Signal
18	V _{SS}	-	-	Ground for Digital Part
19	FBLK	-	Output	Fast Blank Signal
20	B_OUT	-	Output	Video Signal Output (B)
21	G_OUT	-	Output	Video Signal Output (G)
22	R_OUT	-	Output	Video Signal Output (R)
23	INT	-	Output	Intensity Signal Output
24	V _{DD}	-	-	+5 V Supply Voltage for Digital Part

ABSOLUTE MAXIMUM RATINGS

Parameters	Symbol	Value	Unit
Supply Voltage	V_{DD}	-0.3 ~ 7.0	V
Input Voltage	V_I	-0.3 ~ 7.0	V
Power Dissipation	P_D	1200	mW
Operating Temperature Range	T_{OPR}	-20 ~ 70	°C
Storage Temperature Range	T_{STG}	-40 ~ 125	°C

NOTE: PKG Thermal Resistance : 64.2 °C/W

ELECTRICAL CHARACTERISTICS**DC Electrical Characteristics**

($T_a = 25\text{ °C}$, $V_{DDA} = V_{DD} = 5\text{ V}$)

Table 2. DC Electrical Characteristics

Parameters (Conditions)	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{DD}	4.75	5.00	5.25	V
Supply Current (No load on any output)	I_{DD}	-	-	25	mA
Input Voltage	V_{IH}	$0.8V_{DD}$	-	-	V
	V_{IL}	-	-	$V_{SS} + 0.4$	V
Output Voltage ($I_{out} = 1\text{ mA}$)	V_{OH}	$0.8V_{DD}$	-	-	V
	V_{OL}	-	-	$V_{SS} + 0.4$	V
Input Leakage Current	I_{IL}	-10	-	10	μA
VCO Input Voltage	V_{VCO}		2.5		V

OPERATION TIMINGS

Table 3. Operation Timings

Parameters (Conditions)	Symbol	Min.	Typ.	Max.	Unit
Output Signal R/G/B_OUT, INT, FBLK (Ta = 25°C V _{DDA} = V _{DD} = 5 V , C _{LOAD} = 30pF)					
Rise Time	t _R	-	-	6	nsec
Fall Time	t _F	-	-	6	nsec
Input Signal HFLB, VFLB					
Horizontal Flyback Signal Frequency	f _{HFLB}	-	-	120	kHz
Vertical Flyback Signal Frequency	f _{VFLB}	-	-	200	Hz
I²C Interface SDA, SCL (Refer to Figure 3)					
SCL Clock Frequency	f _{SCL}	-	-	300	kHz
Hold Time for start condition	t _{hs}	500	-	-	ns
Set Up Time for stop condition	t _{sus}	500	-	-	ns
Low Duration of clock	t _{low}	400	-	-	ns
High Duration of clock	t _{high}	400	-	-	ns
Hold Time for data	t _{hd}	0	-	-	ns
Set Up Time for data	t _{sud}	500	-	-	ns
Time between 2 access	t _{ss}	500	-	-	ns
Fall Time of SDA	t _{rSDA}	-	-	20	ns
Rise Time of both SCL and SDA	t _{rSDA}	-	-	-	ns

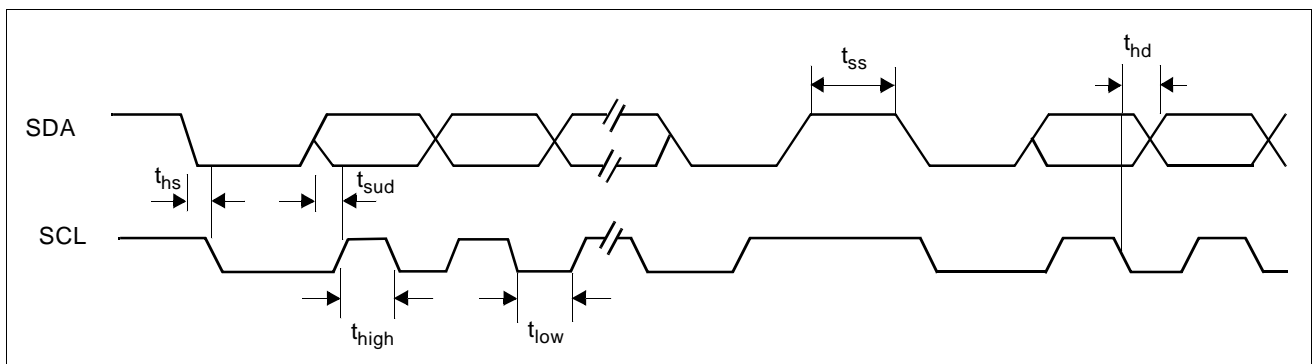


Figure 3. I²C Bus Timing Diagram

FUNCTIONAL DESCRIPTIONS

Data Transmission to the KS2501

According to the I²C protocol, the KS2501 receives the data from a micro controller. The SDA line and the SCL line are shown in Figure 4. As shown in Figure 4, after the starting pulse, the slave address with R/W* bit and an acknowledge are transmitted in sequence, an internal register address of the KS2501 is followed. The first 8-bit byte is the upper 8bits of the register address. The lower 8bits of the register address are followed after the second acknowledge. There is a data transmission format and are two address bit patterns in the KS2501 as following. The slave address of the KS2501 is BAH(in hexadecimal).

Data Transmission Format

Row Address -> Column Address -> Data Byte N -> Data Byte N+1 -> Data Byte N+2 ->

Address Bit Pattern for Display Registers Data

(a) Row Address Bit Pattern R3 - R0: Valid Data for Row Address

A15	A14	A13	A12	A11	A10	A9	A8
X	X	X	X	R3	R2	R1	R0

(b) Column Address Bit Pattern C4 - C0: Valid Data for Column Address

A7	A6	A5	A4	A3	A2	A1	A0
X	X	X	C4	C3	C2	C1	C0

After addressing, data bytes are followed as the above data transmission format. The Figure 4 describes the data transmission with the I²C bus protocol.

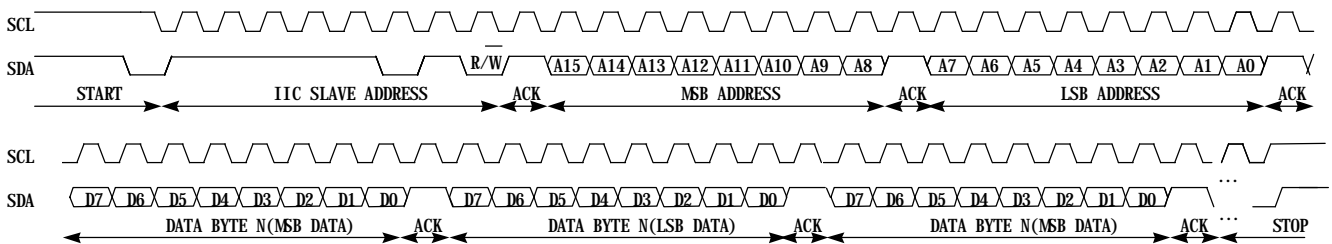


Figure 4. SDA line and SCL line (Write Operation)

Memory Map

The display RAM is addressed with the row and column number in sequence. The display RAM consists of four register groups: Character & Attribute Registers, Row Attribute Registers, Frame Control Registers and PWM Control Registers. As the display area in a monitor screen is 30 columns by 15 rows, the related Character & Attribute Registers are also 30 columns by 15 rows. Each register contains a character address and an attribute corresponding to display location on a monitor screen. And one register is composed of 16 bits. The lower 9 bits select characters out of 464 ROM fonts. The upper 7 bits are assigned to give a character attribute to a selected font. Row Attribute Registers occupy the 31th column of Display RAM and provide the row attribute of a blank mode, raster color, raster color intensity, character color intensity, horizontal character size, vertical character size. Frame Control Registers and PWM Control Registers are located at the 16th row.

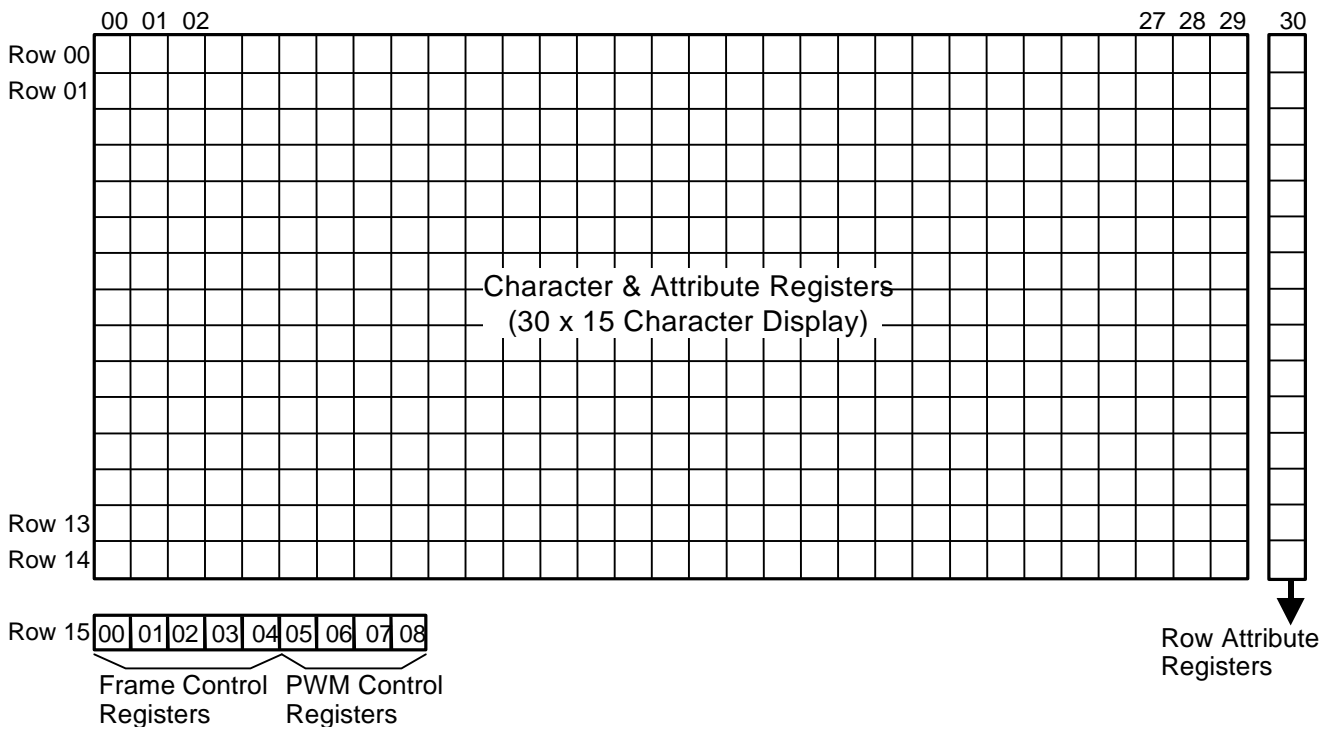


Figure 5. Memory Map of Display Registers

ROM Fonts

KS2501 is able to supply 464 ROM fonts for describing an OSD icon. So a multi-language OSD icon can be generated. 448 fonts of 464 ROM fonts are standard fonts and 16 fonts are multi-color fonts as following figure. The standard font \$000 is reserved for blank data. Each multi-color font consists of 4-color attribute ROM fonts as following figure.

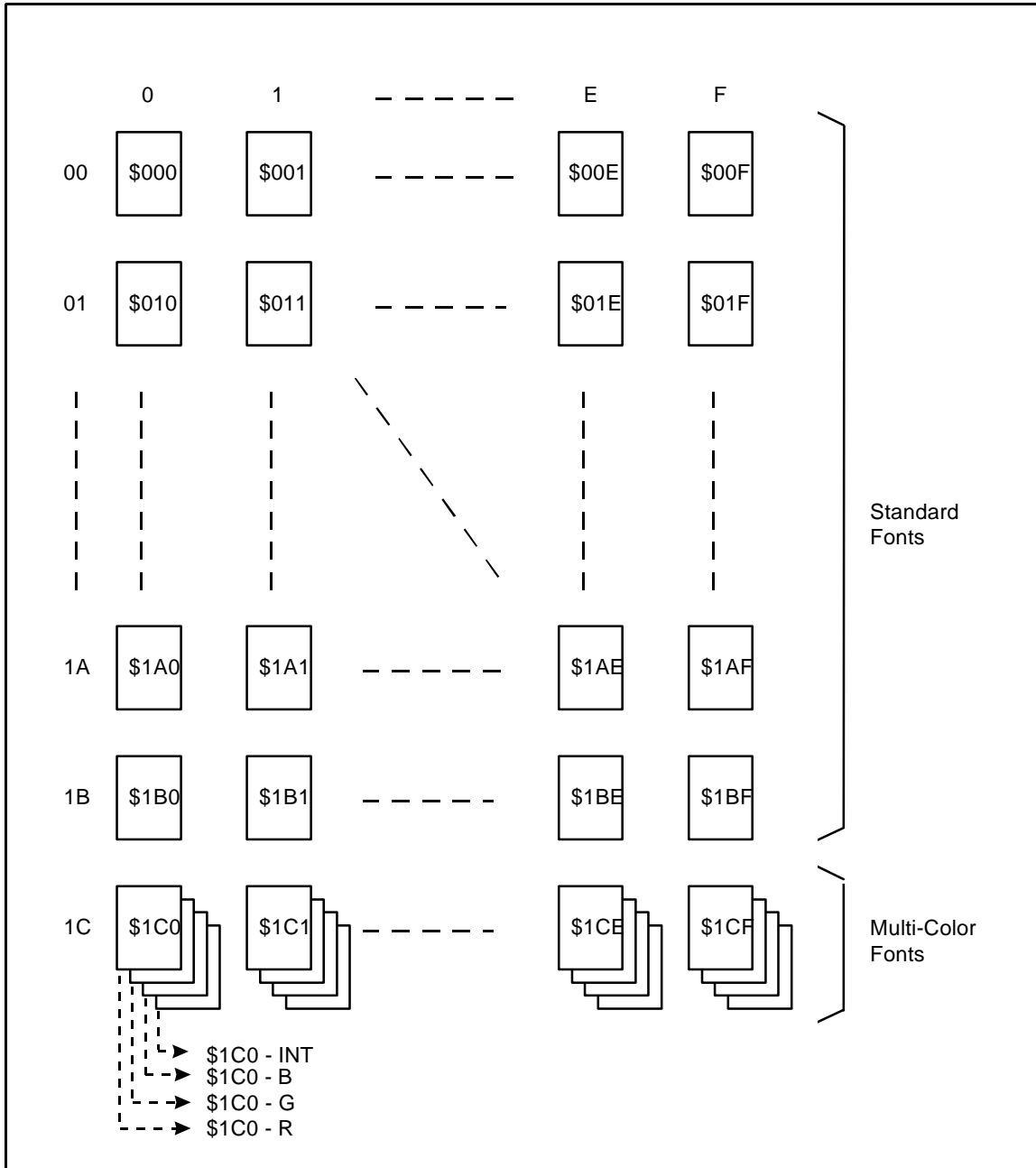
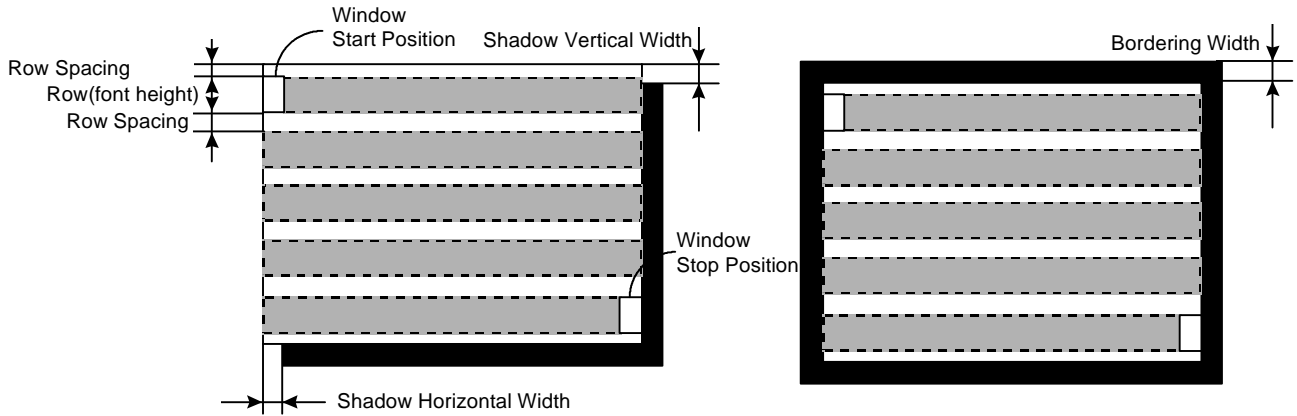


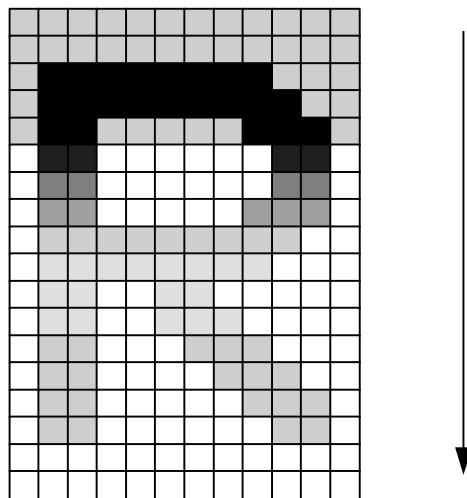
Figure 6. Array of ROM Fonts

Window , Window Shadowing and Bordering



Scroll

The scrolling function is to display or erase a character slowly from the top line to the bottom. The scrolling time is controlled by 'ScrT' bit of the frame control registers. If 'ScrT' bit is high, then the time is 0.5 sec. Otherwise, 1 sec.



Character Height Control

Two examples of the height-controlled character are shown in the following figure. The height control is performed by repeating some lines. The repeating line-number comes from the equation below.

$$\begin{aligned} &[\# \text{ of the repeating lines} = 2 + N \times M], \\ &\text{where } N = 1, 2, 3, \dots \text{ and } M = \text{round}\{14 \div (\text{CH}[5:0] - 18)\}. \end{aligned}$$

If the M value is less than or equal to 1, all the lines of the standard font are repeated once or more. This is described as following.

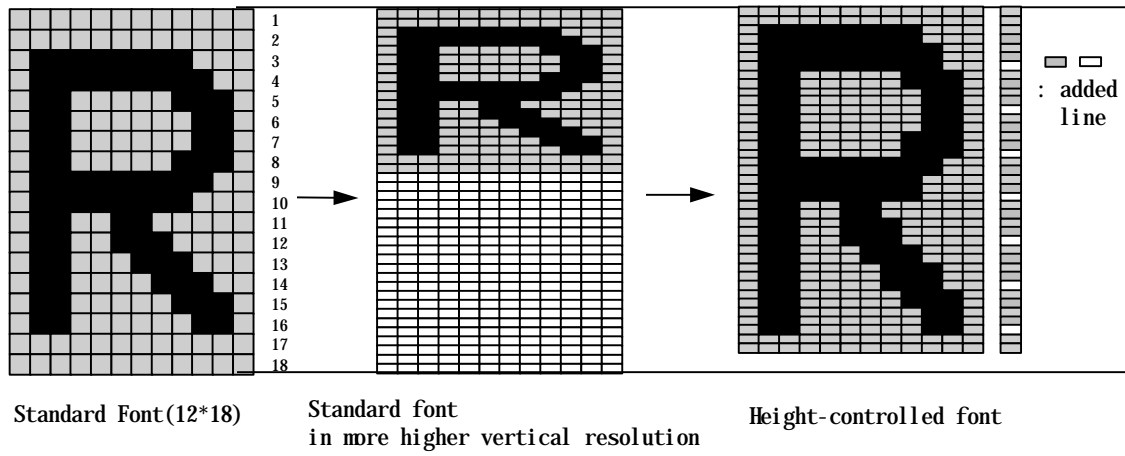
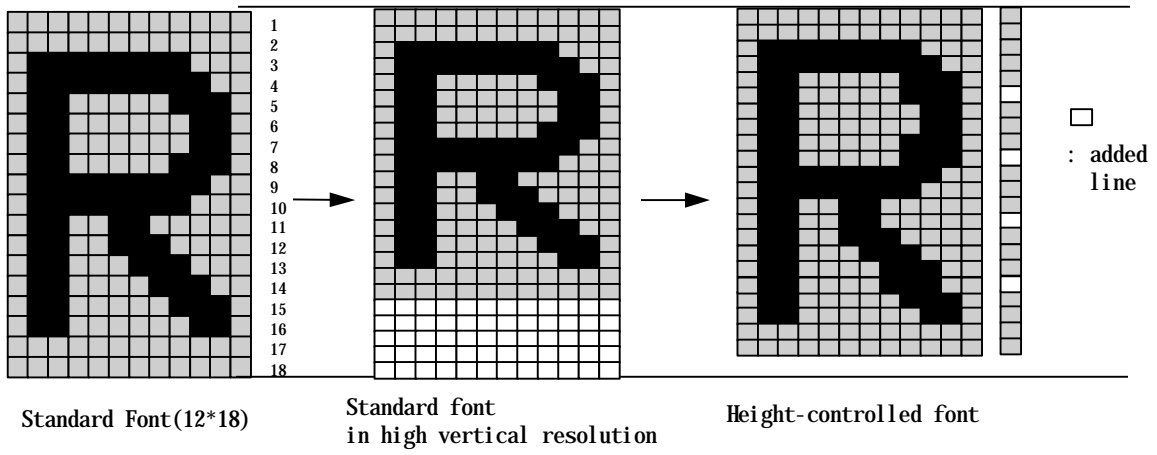
- (i) If CH[5:0] is greater than 32, and less than or equal to 46 ($32 < \text{CH}[5:0] \leq 46$), then all lines are repeated once or twice. The lines repeated twice are selected by the following equation.

$$[\# \text{ of the repeating lines} = 2 + N \times M],$$
 where $N = 1, 2, 3, \dots$ and $M = \text{round}\{14 \div (\text{CH}[5:0] - 32)\}$.
- (ii) If CH[5:0] is greater than 46, and less than or equal to 60 ($46 < \text{CH}[5:0] \leq 60$), then all lines are repeated twice or three times. The lines repeated three times are selected by the following equation.

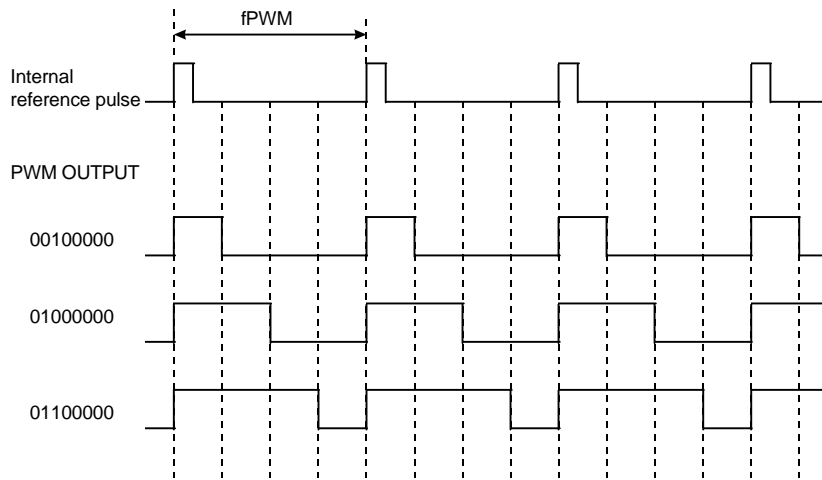
$$[\# \text{ of the repeating lines} = 2 + N \times M],$$
 where $N = 1, 2, 3, \dots$ and $M = \text{round}\{14 \div (\text{CH}[5:0] - 46)\}$.
- (iii) If CH[5:0] is greater than 60, and less than or equal to 64 ($60 < \text{CH}[5:0] \leq 64$), then all lines are repeated three or four times. The lines repeated four times are selected by the following equation.

$$[\# \text{ of the repeating lines} = 2 + N \times M],$$
 where $N = 1, 2, 3, \dots$ and $M = \text{round}\{14 \div (\text{CH}[5:0] - 60)\}$.

The repeating line-number is limited to 16.



PWM OUTPUT



The frequency of PWM signal (f_{PWM}) is dependent on the horizontal flyback signal frequency and horizontal mode (320dots/line, ...) as shown in the following table.

Horizontal Mode	320 dots/line (f_{PWM})	480 dots/line (f_{PWM})	640 dots/line (f_{PWM})	800 dots/line (f_{PWM})
15kHz < H_f < 20kHz	$(320/256) * H_f$	$(480/256) * H_f$	$(640/256) * H_f$	$(800/256) * H_f$
20kHz < H_f < 35kHz			$(640/256) * (H_f/2)$	$(800/256) * (H_f/2)$
35kHz < H_f < 50kHz		$(480/256) * (H_f/2)$		$(640/256) * (H_f/4)$
50kHz < H_f < 65kHz				
65kHz < H_f < 80kHz	$(320/256) * (H_f/2)$			
80kHz < H_f < 95kHz				
95kHz < H_f < 110kHz				
110kHz < H_f < 120kHz				

FRAME CONTROL & TIMING

Figure 7 shows the composition of display frame with the OSD characters.

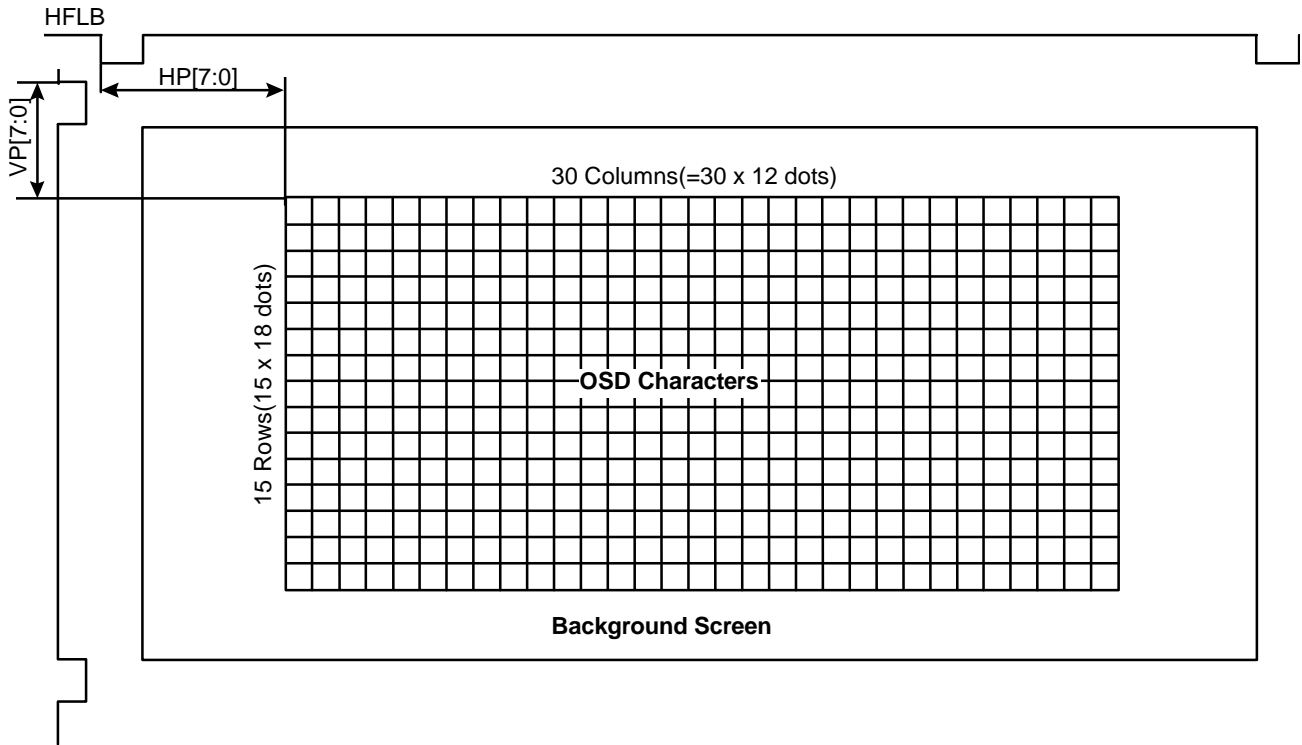


Figure 7. Frame Composition with the OSD Characters

You can determine the dot frequency by the equation of H freq. x the number of horizontal resolution. And the number of horizontal resolution is determined by the bit9 - 8 (dot 1, dot 0) of the frame Control registers-1. If dot 0 = "0", dot 1 = "0", then the dot frequency is calculated by the equation of H freq. \times 320. If the H freq. = 15 kHz, then the dot frequency is $15 \text{ kHz} \times 320 = 4.8 \text{ MHz}$. If dot 0 = "1", dot 1 = "1" and the horizontal frequency is 120 kHz, then the dot frequency is $120 \text{ kHz} \times 800 = 96 \text{ MHz}$. 96 MHz is the maximum clock frequency in this processor.

REGISTER DESCRIPTION

Character & Attribute Registers : Row00~14, Column00~29

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
BINV	BOX1	BOX0	B	G	R	Blink	C8	C7	C6	C5	C4	C3	C2	C1	C0
← Character Attribute →							← Character Code(464 Fonts) →								

Row Attribute Registers : Row00~14, Column30

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
-	-	-	CBli	BOXE	BORD	SHA	RB	RG	RR	BINT	CINT	HZ1	HZ0	VZ1	VZ0
							← Raster Color →			← Intensity →		← Character Size →			

Frame Control Registers-0 : Row15, Column00

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
-	Fde	FdeT	VPOL	HPOL	WC	WBOR	WSHA	-	Erase	EN	ScrI	ScrT	Bli1	Bli0	BliT

Frame Control Registers-1 : Row15, Column01

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
CP1	CP0	Fpll	HF2	HF1	HF0	dot1	dot0	FBLK	BREN	CH5	CH4	CH3	CH2	CH1	CH0
← PLL Control →							← Character Height Control →								

Frame Control Registers-2 : Row15, Column02

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
HP7	HP6	HP5	HP4	HP3	HP2	HP1	HP0	VP7	VP6	VP5	VP4	VP3	VP2	VP1	VP0
← Horizontal Start Position →								← Vertical Start Position →							

Frame Control Registers-3 : Row15, Column03

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
RS2	RS1	RS0	RSB	RSG	RSR	RSI	STR3	STR2	STR1	STR0	STC4	STC3	STC2	STC1	STC0
← Row Space →			← Row Space Color →				← Window Start Position →								

Frame Control Registers-4 : Row15, Column04

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
-	BW1	BW0	HW1	HW0	VW1	VW0	SPR3	SPR2	SPR1	SPR0	SPC4	SPC3	SPC2	SPC1	SPC0
							← Window Stop Position →								

PWM Registers : Row15, Column05~08

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
MSB							LSB	MSB							LSB
← Channel 2/4/6/8 →								← Channel 1/3/5/7 →							

Table 4. Register Description



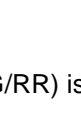




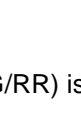
Registers	Bits	Description								
Character & Attribute Registers (Row 00~14, Column 00~29)	C8~C0 (Bit 8~0)	Character Code Address of 464 ROM Fonts.								
	Blink (Bit 9)	Character Blinking. Set this bit to activate the blinking effect. The blinking period is set by the 'Bli T' bit and the duty is selected by the 'Bli 0' and 'Bli 1' bits.								
	B,G,R (Bit C~A)	Character Color is determined by these bits. 8 colors can be selected and the color intensity of a character is given by 'CINT' bit of Row Attribute Registers. So you can select up to 16 colors. If a multi-color font is selected, this bits must be set to all 0's.								
	BOX 1, BOX0 (Bit E, D)	Character Box Drawing. The combinations of this two bits generate four different box drawing modes as following. The following example is the case that box drawing is activated with the font 'A'. <table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <td style="border: none;">BOX0 BOX1</td> <td style="border: none;">0</td> <td style="border: none;">1</td> </tr> <tr> <td style="border: none;">0</td> <td style="text-align: center;">BOX OFF</td> <td style="text-align: center;"></td> </tr> <tr> <td style="border: none;">1</td> <td style="text-align: center;"></td> <td style="text-align: center;"></td> </tr> </table> <p>* Bit F ~ D (RB/RG/RR) is also used for raster color by setting the 'BOXE' bit low. Raster color of a font is determined by this bits if the 'BOXE' bit is low. Priority of raster color selected here is higher than that of row attribute.</p>	BOX0 BOX1	0	1	0	BOX OFF		1	
BOX0 BOX1	0	1								
0	BOX OFF									
1										
BINV (Bit F)	Box Inversion. The box drawing activated by the bit E and D is changed to white box from black and conversely.									

Table 4. Register Description(Continued)

Registers	Bits	Description															
Row Attribute Registers (Row 00 ~ 14, Column 30)	VZ1,VZ0 (Bit 1, 0)	Vertical Character Size Control. Vertical character size is determined by the combinations of this two bits as following table. <table border="1" style="margin: 10px auto;"> <thead> <tr> <th>VZ1</th> <th>VZ0</th> <th>Vertical Character Size</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>1X</td> </tr> <tr> <td>0</td> <td>1</td> <td>2X</td> </tr> <tr> <td>1</td> <td>0</td> <td>3X</td> </tr> <tr> <td>1</td> <td>1</td> <td>4X</td> </tr> </tbody> </table>	VZ1	VZ0	Vertical Character Size	0	0	1X	0	1	2X	1	0	3X	1	1	4X
	VZ1	VZ0	Vertical Character Size														
	0	0	1X														
	0	1	2X														
	1	0	3X														
	1	1	4X														
	HZ1,HZ0 (Bit 3, 2)	Horizontal Character Size Control. The horizontal character size is determined by the combinations of this two bits as following table. <table border="1" style="margin: 10px auto;"> <thead> <tr> <th>HZ1</th> <th>HZ0</th> <th>Horizontal Character Size</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>1X</td> </tr> <tr> <td>0</td> <td>1</td> <td>2X</td> </tr> <tr> <td>1</td> <td>0</td> <td>3X</td> </tr> <tr> <td>1</td> <td>1</td> <td>4X</td> </tr> </tbody> </table>	HZ1	HZ0	Horizontal Character Size	0	0	1X	0	1	2X	1	0	3X	1	1	4X
HZ1	HZ0	Horizontal Character Size															
0	0	1X															
0	1	2X															
1	0	3X															
1	1	4X															
CINT (Bit 4)	Character Color Intensity. If this bit is set, the color intensity of characters in the same row is high.																
RINT (Bit 5)	Raster Color Intensity. If this bit is set, the color intensity of rasters in the same row is high																
RB,RG,RR (Bit 8~6)	Raster Color is determined by these bits. 8 colors can be selected and the color intensity of a character is given by 'RINT' bit of Row Attribute Registers. So you can select up to 16 colors.																
SHA	Character Shadowing. Set this bit to activate characters shadowing.																
BORD	Character Bordering. Set this bit to activate characters shadowing.																
BOXE (Bit B)	BOX Enable. If this bit is set, Bit F-D in the Character & Attribute Registers are used for the box-drawing function. Otherwise,those are used for raster color of a font. Even though the raster color attribute is given by Bit 8-6 in the row attribute registers, the priority of Bit F-D in the character & attribute registers is higher.																
Row Attribute Registers (Row 00 ~ 14, Column 30)	CBli (Bit C)	Color Blink Enable. If this bit is high, color blinking effect is activated. The color effect is to repeat color inversion between character and raster. Color blinking time and the duty is controlled by Bil T, Bil 1 and Bli 0.															
	Bit D-F	Reserved															

Table 4. Register Description(Continued)

Registers	Bits	Description															
Frame Control Registers-0 (Row 15, Column 00)	Bli T (Bit 0)	Blink Time Control. If this bit is high, the blink time is 0.5 sec. Otherwise, 1 sec.															
	Bli 1,Bli 0 (Bit 2,1)	Blinking Duty Control. The blinking duty is controlled by the combination of this two bits as following. <table border="1" data-bbox="655 555 1300 797"> <thead> <tr> <th>Bli 1</th> <th>Bli 0</th> <th>Blinking Duty</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Blink Off</td> </tr> <tr> <td>0</td> <td>1</td> <td>Duty 25%</td> </tr> <tr> <td>1</td> <td>0</td> <td>Duty 50%</td> </tr> <tr> <td>1</td> <td>1</td> <td>Duty 75%</td> </tr> </tbody> </table>	Bli 1	Bli 0	Blinking Duty	0	0	Blink Off	0	1	Duty 25%	1	0	Duty 50%	1	1	Duty 75%
	Bli 1	Bli 0	Blinking Duty														
	0	0	Blink Off														
	0	1	Duty 25%														
	1	0	Duty 50%														
	1	1	Duty 75%														
	ScrT (Bit 3)	Scroll Time Control. If this bit is high, the scroll time is 0.5 sec. Otherwise, 1 sec.															
	Scrl (Bit 4)	Scroll Enable. The scroll display is activated by setting this bit high.															
	EN (Bit 5)	OSD Enable. The character display is controlled by this bit. If this bit is high, OSD is enable. Otherwise, disable.															
	Erase (Bit 6)	RAM Erasing. RAM data are erased by setting this bit.															
	WSHA (Bit 8)	Window Shadowing. Set this bit to activate window shadowing.															
	WBOR (Bit 9)	Window Bordering. Set this bit to activate window bordering.															
WC (Bit A)	White/black selection of window border and shadow. If this bit is high, the color of window border and shadow is white. Otherwise, black.																
HPOL (Bit B)	Polarity of Horizontal Fly Back Signal. Positive 1, Negative 0																
VPOL (Bit C)	Polarity of Vertical Fly Back Signal. Positive 1, Negative 0																
FdeT (Bit D)	Fade-in and fade-out Time Control. If this bit is high, the time is 0.5 sec. Otherwise, 1 sec.																
Fde (Bit E)	Fade-in and fade-out Enable. The fade-in and fade-out effect is activated by setting this bit high.																
Bit F	Reserved.																

Table 4. Register Description(Continued)

Registers	Bits	Description																																			
Frame Control Registers-1 (Row 15, Column 01)	CH 5~CH 0 (Bit 5~0)	Character Height Control. The vertical character size is determined by the bit 'VZ1' and 'VZ0'. This six bits are available to get a proper character height by setting a binary value. According to the value made by this six bits, the character height is determined. If the value is 32, the number of vertical pixel of character font is 32. Eventually, the character height is expanded from 18 to 63. The binary value must be greater than 18.																																			
	BREN	Back Raster Blank Enable. If this bit is high and the raster color is black, then the raster is transparent.																																			
	FBLK (Bit 7)	It determines the configuration of FBLK output pin. When it is clear, FBLK pin outputs high during displaying characters or rasters. Otherwise, FBLK pin outputs high only during displaying characters.																																			
	dot 1, dot 0 (Bit 9,8)	This two bits determine the number of dots per horizontal line. Refer to following table. <table border="1" style="margin: 10px auto;"> <thead> <tr> <th>dot 1</th> <th>dot 0</th> <th>No. of Dots</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>320 dots/line</td> </tr> <tr> <td>0</td> <td>1</td> <td>480 dots/line</td> </tr> <tr> <td>1</td> <td>0</td> <td>640 dots/line</td> </tr> <tr> <td>1</td> <td>1</td> <td>800 dots/line</td> </tr> </tbody> </table>	dot 1	dot 0	No. of Dots	0	0	320 dots/line	0	1	480 dots/line	1	0	640 dots/line	1	1	800 dots/line																				
	dot 1	dot 0	No. of Dots																																		
0	0	320 dots/line																																			
0	1	480 dots/line																																			
1	0	640 dots/line																																			
1	1	800 dots/line																																			
HF 2~HF 0 (Bit C~A)	The horizontal frequency information is transferred by this two bits as following tables. <table border="1" style="margin: 10px auto;"> <thead> <tr> <th>HF2</th> <th>HF1</th> <th>HF0</th> <th>Hf Information</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>15 kHz < Hf < 20 kHz</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>20 kHz ≤ Hf < 35 kHz</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>35 kHz ≤ Hf < 50 kHz</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>50 kHz ≤ Hf < 65 kHz</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>65 kHz ≤ Hf < 80 kHz</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>80 kHz ≤ Hf < 95 kHz</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>95 kHz ≤ Hf < 110 kHz</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>110 kHz ≤ Hf < 120 kHz</td> </tr> </tbody> </table>	HF2	HF1	HF0	Hf Information	0	0	0	15 kHz < Hf < 20 kHz	0	0	1	20 kHz ≤ Hf < 35 kHz	0	1	0	35 kHz ≤ Hf < 50 kHz	0	1	1	50 kHz ≤ Hf < 65 kHz	1	0	0	65 kHz ≤ Hf < 80 kHz	1	0	1	80 kHz ≤ Hf < 95 kHz	1	1	0	95 kHz ≤ Hf < 110 kHz	1	1	1	110 kHz ≤ Hf < 120 kHz
HF2	HF1	HF0	Hf Information																																		
0	0	0	15 kHz < Hf < 20 kHz																																		
0	0	1	20 kHz ≤ Hf < 35 kHz																																		
0	1	0	35 kHz ≤ Hf < 50 kHz																																		
0	1	1	50 kHz ≤ Hf < 65 kHz																																		
1	0	0	65 kHz ≤ Hf < 80 kHz																																		
1	0	1	80 kHz ≤ Hf < 95 kHz																																		
1	1	0	95 kHz ≤ Hf < 110 kHz																																		
1	1	1	110 kHz ≤ Hf < 120 kHz																																		
FPLL (Bit D)	If this bit is high, the VCO block of OSD_PLL operates on full range (4 MHz - 96 MHz).																																				

Table 4. Register Description(Continued)

Registers	Bits	Description															
Frame Control Register-1 (Row 15, Column 01)	CP 1,CP 0 (Bit F,E)	This bit controls charge pump output current.															
		<table border="1"> <thead> <tr> <th>CP 1</th> <th>CP 0</th> <th>Charge Pump Current</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0.5mA</td> </tr> <tr> <td>0</td> <td>1</td> <td>0.75mA</td> </tr> <tr> <td>1</td> <td>0</td> <td>1.0mA</td> </tr> <tr> <td>1</td> <td>1</td> <td>1.25mA</td> </tr> </tbody> </table>	CP 1	CP 0	Charge Pump Current	0	0	0.5mA	0	1	0.75mA	1	0	1.0mA	1	1	1.25mA
		CP 1	CP 0	Charge Pump Current													
		0	0	0.5mA													
		0	1	0.75mA													
1	0	1.0mA															
1	1	1.25mA															
Frame Control Register-2 (Row 15, Column 02)	VP 7~VP 0 (Bit 7~0)	Vertical Start Position Control. It means the top margin height from the V-sync reference edge. (= VP[7:0] × 2)															
	HP 7~HP 0 (Bit F~8)	Horizontal Start Position Control. It means the horizontal display delay from the H-sync reference edge to the 1'st pixel position of characters. (= HP[7:0] × 6)															
Frame Control Register-3 (Row 15, Column 02)	STC 4 ~STC 0	Window Start Column Position. It means the column address that window starts from.															
	STR 3 ~STR 0	Window Start Row Position. It means the row address that window starts from.															
	RSI	Row Space Color Intensity.															
	RSR,RSG, RSB	Row Space Color Attribute.															
	RS 2~RS 0 (Bit F~D)	Row Space. It means the line number between a character row and the next row. The default value is 0. (line number for spacing = RS[2:0] × 1)															
Frame Control Registers-4 (Row 15, Column 04)	SPC 4~ STP 0	Window Stop Column Position. It means the column address that window stops on.															
	STR 3~ STR 0	Window Stop Row Position. It means the row address that window stops on.															
	VW 1, 0	Vertical width of window shadowing.															
	HW 1, 0	Horizontal width of window shadowing.															
	BW 1, 0	Width of window bordering.															
PWM Registers (Row 15, Column 05 - 08)	Bit 7~ 0	This 8-bit value decides the output duty cycle and waveforms of PWM for channel.															
	Bit F~8	for channel 2/4/6/8.															

STANDARD ROM FONTS

000	001	002	003	004	005	006	007	008	009	00A	00B	00C	00D	00E	00F
010	011	012	013	014	015	016	017	018	019	01A	01B	01C	01D	01E	01F
020	021	022	023	024	025	026	027	028	029	02A	02B	02C	02D	02E	02F
	1	2	3	4	5	6	7	8	9	:					
030	031	032	033	034	035	036	037	038	039	03A	03B	03C	03D	03E	03F
	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O
040	041	042	043	044	045	046	047	048	049	04A	04B	04C	04D	04E	04F
P	Q	R	S	T	U	V	W	X	Y	Z					
050	051	052	053	054	055	056	057	058	059	05A	05B	05C	05D	05E	05F
	a	b	c	d	e	f	g	h	i	j	k	l	m	n	o
060	061	062	063	064	065	066	067	068	069	06A	06B	06C	06D	06E	06F
p	q	r	s	t	u	v	w	x	y	z					
070	071	072	073	074	075	076	077	078	079	07A	07B	07C	07D	07E	07F

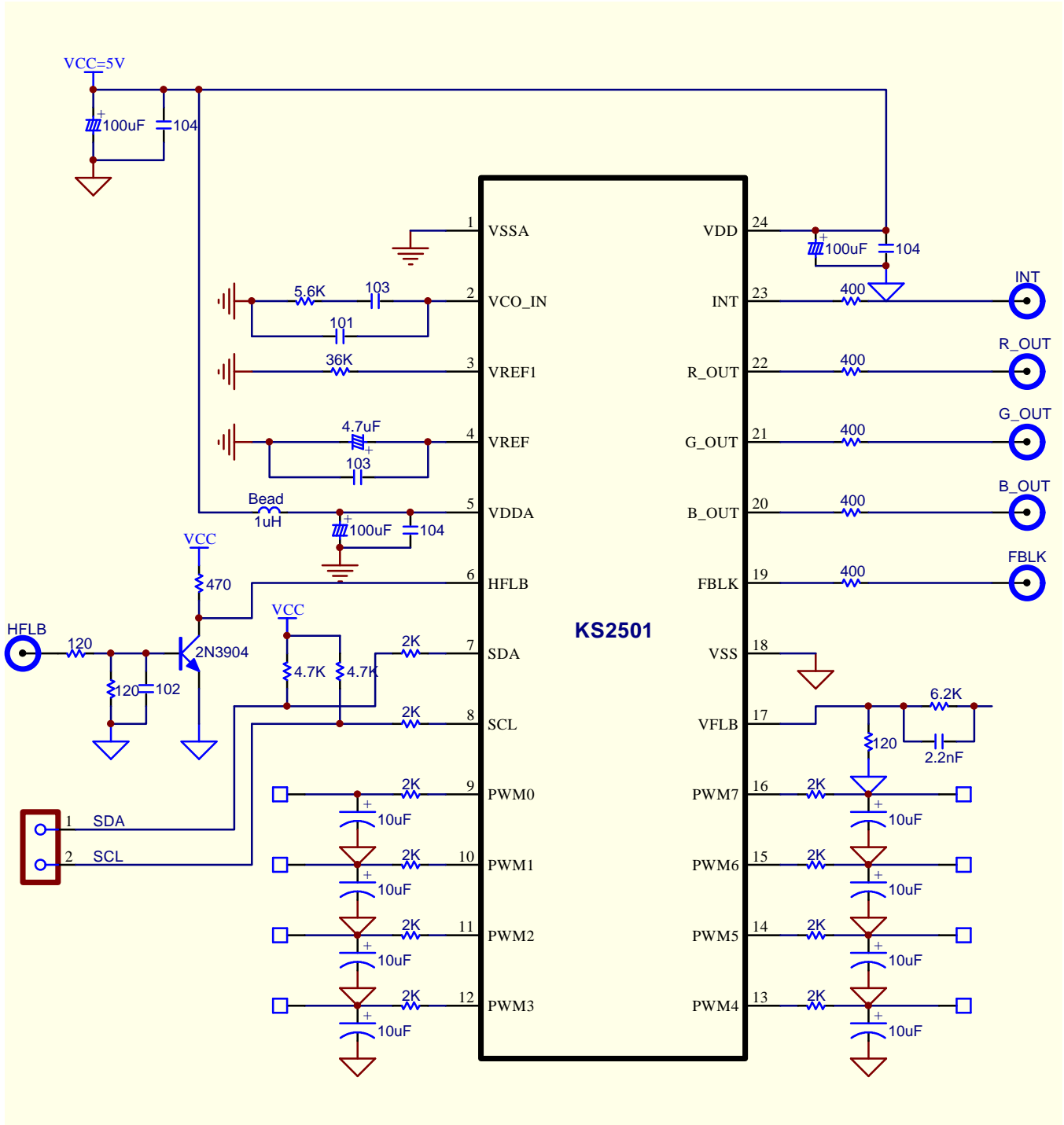
Ä	Ë	Ï	Ö	Ü	Â	Ê	Î	Ô	Û	Á	É	Í	Ó	Ú	Ç
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ä	ë	ï	ö	ü	â	ê	î	ô	û	á	é	í	ó	ú	ç
090	091	092	093	094	095	096	097	098	099	09A	09B	09C	09D	09E	09F
À	È	Ì	Ò	Ù	Ã	Õ	Ñ	Ã	Š	Ž	Ÿ	ß			
0A0	0A1	0A2	0A3	0A4	0A5	0A6	0A7	0A8	0A9	0AA	0AB	0AC	0AD	0AE	0AF
à	è	ì	ò	ù	ã	õ	ñ	ã	š	ž	ÿ	œ			
0B0	0B1	0B2	0B3	0B4	0B5	0B6	0B7	0B8	0B9	0BA	0BB	0BC	0BD	0BE	0BF
Ⓜ	Ⓝ	Ⓜ	Ⓜ	Ⓜ	Ⓜ	Ⓜ	Ⓜ	Ⓜ	Ⓜ	Ⓜ	Ⓜ	Ⓜ	Ⓜ	Ⓜ	Ⓜ
0C0	0C1	0C2	0C3	0C4	0C5	0C6	0C7	0C8	0C9	0CA	0CB	0CC	0CD	0CE	0CF
Ⓜ	Ⓜ	Ⓜ	Ⓜ	Ⓜ	Ⓜ	Ⓜ	Ⓜ	Ⓜ	Ⓜ	Ⓜ	Ⓜ	Ⓜ	Ⓜ	Ⓜ	Ⓜ
0D0	0D1	0D2	0D3	0D4	0D5	0D6	0D7	0D8	0D9	0DA	0DB	0DC	0DD	0DE	0DF
Ⓜ	Ⓜ	+	Ⓜ	Ⓜ	Ⓜ	Ⓜ	Ⓜ	Ⓜ	Ⓜ	Ⓜ	Ⓜ	Ⓜ	Ⓜ	Ⓜ	Ⓜ
0E0	0E1	0E2	0E3	0E4	0E5	0E6	0E7	0E8	0E9	0EA	0EB	0EC	0ED	0EE	0EF
Ⓜ	Ⓜ	Ⓜ	Ⓜ	?	,	!	~	&	Ⓜ	Ⓜ	Ⓜ	Ⓜ	Ⓜ	Ⓜ	Ⓜ
0F0	0F1	0F2	0F3	0F4	0F5	0F6	0F7	0F8	0F9	0FA	0FB	0FC	0FD	0FE	0FF

100	101	102	103	104	105	106	107	108	109	10A	10B	10C	10D	10E 10F
110	111	112	113	114	115	116	117	118	119	11A	11B	11C	11D	11E 11F
120	121	122	123	124	125	126	127	128	129	12A	12B	12C	12D	12E 12F
130	131	132	133	134	135	136	137	138	139	13A	13B	13C	13D	13E 13F
140	141	142	143	144	145	146	147	148	149	14A	14B	14C	14D	14E 14F
150	151	152	153	154	155	156	157	158	159	15A	15B	15C	15D	15E 15F
160	161	162	163	164	165	166	167	168	169	16A	16B	16C	16D	16E 16F
170	171	172	173	174	175	176	177	178	179	17A	17B	17C	17D	17E 17F

CURRENT FONT NO. : 198

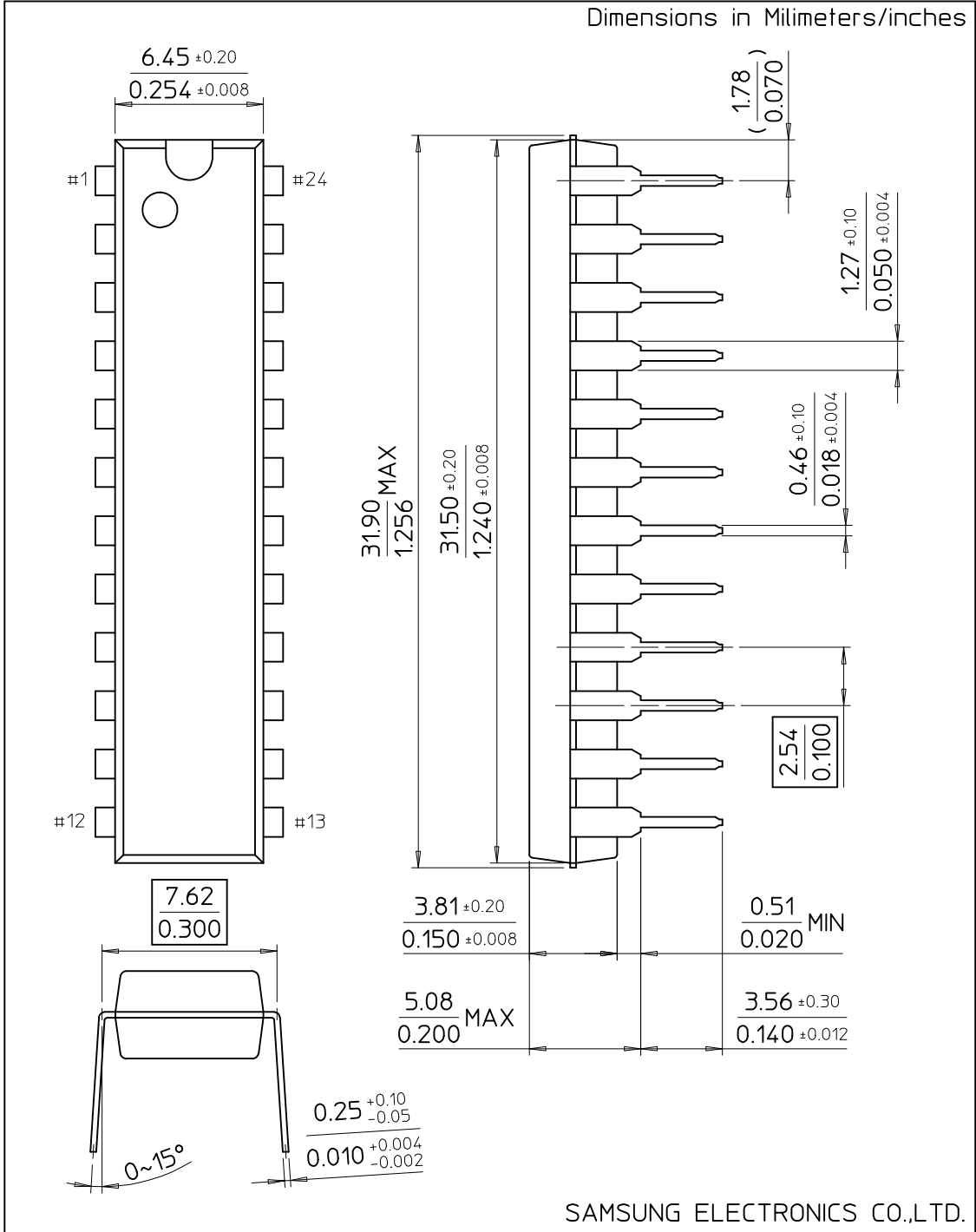
Ä	Ë	Ï	Ö	Ü	Â	Ê	Î	Ô	Û	Á	É	Í	Ó	Ú	Ç
180	181	182	183	184	185	186	187	188	189	18A	18B	18C	18D	18E	18F
ä	ë	ï	ö	ü	â	ê	î	ô	û	á	é	í	ó	ú	ç
190	191	192	193	194	195	196	197	198	199	19A	19B	19C	19D	19E	19F
À	È	Ì	Ò	Ù	Ã	Õ	Ñ	Ã	Š	Ž	Ÿ	ß			
1A0	1A1	1A2	1A3	1A4	1A5	1A6	1A7	1A8	1A9	1AA	1AB	1AC	1AD	1AE	1AF
à	è	ì	ò	ù	ã	õ	ñ	ã	š	ž	ÿ	œ			
1B0	1B1	1B2	1B3	1B4	1B5	1B6	1B7	1B8	1B9	1BA	1BB	1BC	1BD	1BE	1BF
R															
1C0	1C1	1C2	1C3	1C4	1C5	1C6	1C7	1C8	1C9	1CA	1CB	1CC	1CD	1CE	1CF
G															
1C0	1C1	1C2	1C3	1C4	1C5	1C6	1C7	1C8	1C9	1CA	1CB	1CC	1CD	1CE	1CF
B															
1C0	1C1	1C2	1C3	1C4	1C5	1C6	1C7	1C8	1C9	1CA	1CB	1CC	1CD	1CE	1CF
INT															
1C0	1C1	1C2	1C3	1C4	1C5	1C6	1C7	1C8	1C9	1CA	1CB	1CC	1CD	1CE	1CF

APPLICATION CIRCUIT



24-DIP-300

Dimensions in Millimeters/inches



SAMSUNG ELECTRONICS CO.,LTD.