INSTRODUCTION

6 BIT 384 CHANNEL OUTPUT SOURCE DRIVER

The KS0654 is a 6 Bits Source Driver capable of supporting XGA (1024 × 768) to SXGA (1280 × 1024) full color resolutions for TFT LCD displays. Input data consists of three colors and 2 port data, D0, D1, D2, D3, D4 and D5 (red, green, blue, red, green, blue, respectively).

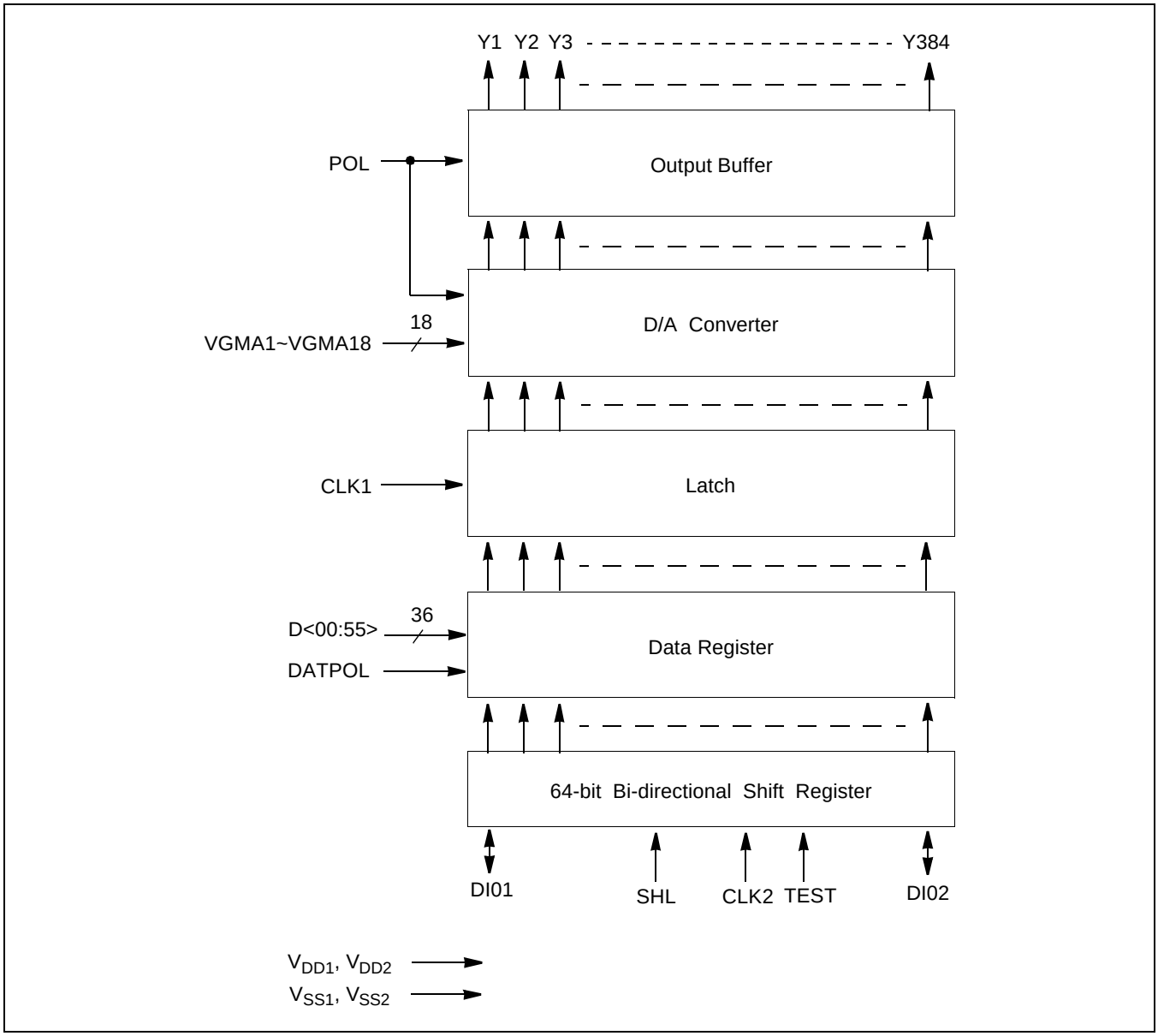
The KS0654 converts each 6 bits digital color data into the analog voltage for 384 columns of TFT LCD panel, switching the correct gray level corresponding to the digital value. This switched reference type DAC gives high accuracy within ± 10mV (typ.)

Since the output circuit on the KS0654 incorporates an operational amplifier and has a wide dynamic range, 6.0 to 12.6V, a dot inversion drive, which can apply the gray scale voltage with the opposite polarity to each adjacent dot, can be performed. This can decrease crosstalk degrading display quality and achieve high quality display. The KS0654 reduces power consumption by using LDI613 CMOS technology.

FEATURES

- ❑ High-speed operation
  Maximum operating clock frequency: f_{MAX} = 65MHz (2.7V operation)
- ❑ Logic operating voltage
  V_{DD1} = 2.7 to 3.6V
- ❑ LCD drive voltage
  V_{DD2} = 6.4 to 13.0V
- ❑ 6 bits 3 color 2 port digital input data; 36 bits data bus
- ❑ 384 LCD drive output
- ❑ Output dynamic range = 6.0 to 12.6Vp-p
- ❑ Low output voltage deviation = ± 10mV (typ.)
- ❑ Bidirectional shift register control: SHL
- ❑ Output polarity inversion control: POL
- ❑ Input data inversion control: DATPOL
- ❑ Package
  Slim-type TCP
- ❑ 18 or 10 external gamma reference voltage option

BLOCK DIAGRAM



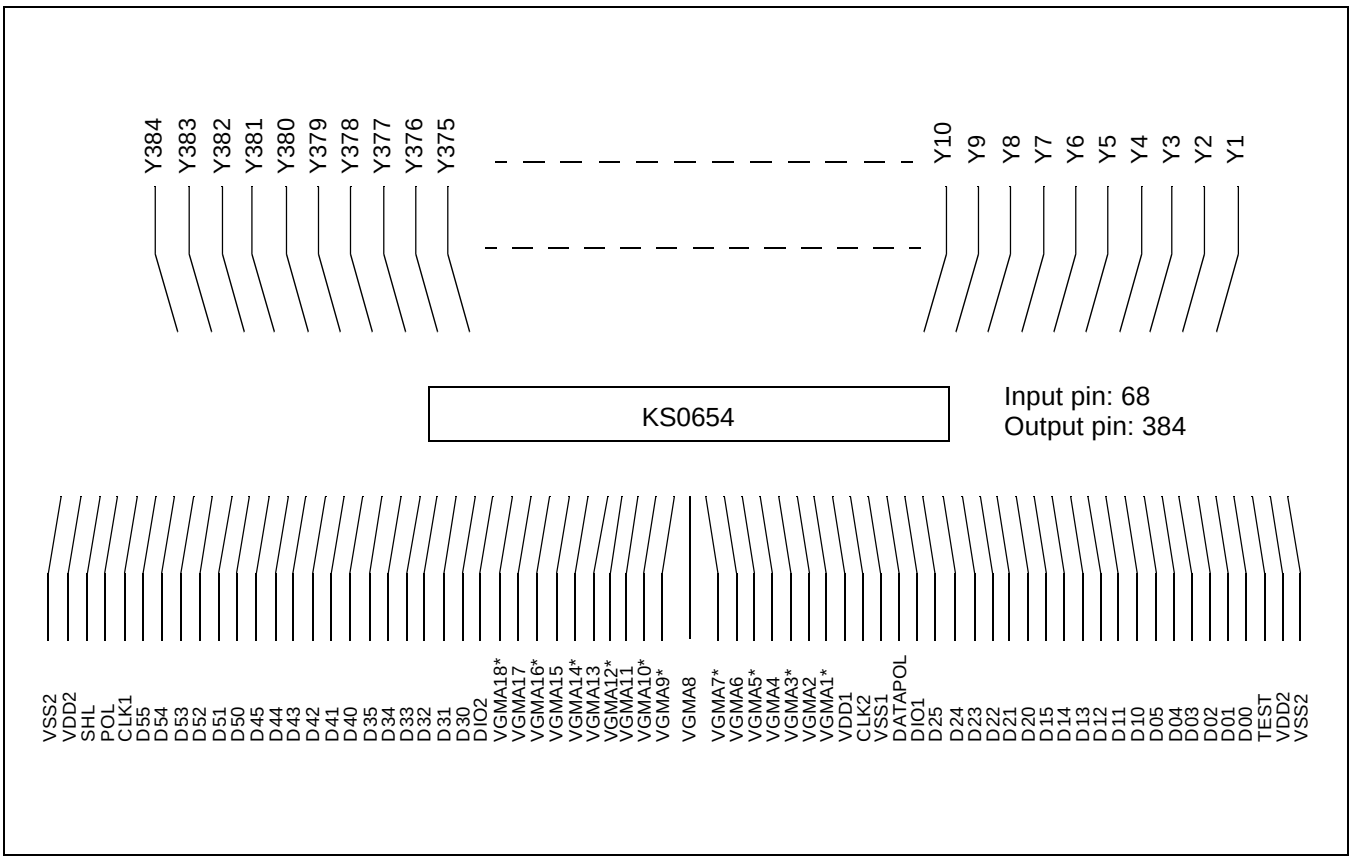
PIN DESCRIPTION

Pin Symbol	Pin Name	Description
V_{DD1}	Logic power supply	2.7 to 3.6V
V_{DD2}	Analog power supply	6.4V to 13.0V
V_{SS1}	Logic ground	Ground (0V)
V_{SS2}	Analog ground	Ground (0V)
Y1~Y384	Analog output	64 gray scale level analog voltage output
D0<0:5> D1<0:5> D2<0:5> D3<0:5> D4<0:5> D5<0:5>	Digital input data	Total data lines consist of 36 data bus (6 bits digital input data, 3 colors (R, G, B) and 2 port). Each 6 bits digital input data is connected to the digital MUX. DX0: LSB, DX5: MSB
SHL	Shift direction control input	Signal SHL determines the direction of bidirectional shift register. When SHL = H, DIO1 = input, DIO2 = output, the right shift operation (Y1 → Y2 →...→ Y384). When SHL = L, DIO1 = output, DIO2 = input, the left shift operation (Y384 → Y383 →... → Y1).
DI01	Right shift/start pulse input/output	SHL = H: DIO1 used as the start pulse input pin. (DIO2 is output) SHL = L: DIO1 used as the start pulse output pin. (DIO2 is input) The shift start pulse input triggers the latch of the bidirectional shift register, and the shift start pulse output transfers to the next chip as the next shift start pulse input. These start pulse in/out signal is controlled by the signal SHL.
DI02	Left shift/start pulse input/output	
CLK2	Shift clock input	The data register latches two triplet of 6 bits RGB data at each rising edge of CLK2. The data is sequentially loaded into the 384 data latch.
CLK1	Horizontal line latch input	Latches the data register contents as rising edge and transfers it to the D/A converter. Also, after CLK1 input, clears the internal shift register contents. After 1 pulse input on start, operates normally. CLK1 input timing refers to the Relationship between CLK1 start pulse (DIO1, DIO2) and blanking period of the switching characteristic waveform. (page 10)
VGMA1 to VGMA18	Gamma reference voltage	The gamma reference voltages, VGMA1 to 18, must be externally supported in order to operate the dot inversion. When a dot has a positive polarity, D/A converter refers to VGMA1 to 9 (high region) and when a dot has negative polarity, D/A converter refers to VGMA10 to 18 (low region). To ensure that the correct analog voltages appear at the DAC outputs, the external reference voltages, VGMA1 to 18, must stabilize before D/A conversion.

PIN DESCRIPTION (CONTINUED)

Pin Symbol	Pin Name	Description
POL	Polarity inversion input	Signal POL determines the output terminals of the high or low region D/A converted signals. When POL = H, D/A converted analog voltage signals with VGMA1 to 9 (high region) transfer to the odd number output terminals, and these with VGMA10 to 18 (low region) transfer to the even number output terminals. When POL = L, high region signals transfer to the even number output terminals, and low region signals transfers to the odd number output terminals.
DATPOL	Data inversion input	Signal DATPOL controls the digital MUX, which is connected to data latch. When DATPOL = H, the digital MUX provides the inverting digital data to data latch. When DATPOL = L, the digital MUX provides the non-inverting digital data to the data latch.
TEST	Test pin	TEST = L: Normal operation TEST = H: TEST MODE $\rightarrow$ OP-AMP cut-off This pin is internally pulled-down. < R_{PD} = 15kΩ >

TCP PIN CONFIGURATION



NOTES:

1. This figure does not specify the dimensions of the TCP package.
2. Customer has options which the total number of the reference voltage is 10 (5 ×2) or 18 (9 ×2) before ordering the product.
   When customer choose the total number of the reference voltages ten, device uses only the pins which are marked with "*" TCP pin configuration above.
3. In actual panel application the power should be supplied throgh all the V_{DD2} pins simultaneously.

ABSOLUTE MAXIMUM RATINGS

(V_{SS1} = V_{SS2} = 0V)

Characteristic	Symbol	Rating	Unit
Digital supply voltage	V_{DD1}	–0.3 to +6.5	V
Analog supply voltage	V_{DD2}	–0.3 to +15.0	V
Input voltage	VGMA1 to 18	–0.3 to V_{DD2}+0.3	V
	Other	–0.3 to V_{DD1}+0.3	
Output voltage	DIO1, DIO2	–0.3 to V_{DD1}+0.3	V
	Y1 to Y384	–0.3 to V_{DD2}+0.3	
Operating power dissipation	Pd	200	mW
Operating Temperature	Topr	–20 to +75	°C
Storage Temperature	Tstg	–55 to +125	°C

* If LSIs are stressed beyond the above absolute maximum ratings, they may be permanently destroyed. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under the below recommended operating range is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

NOTE: Power on sequence: V_{DD1} → input voltage → V_{DD2} → VGMA1 to VGMA18

RECOMMENDED OPERATION RANGE

(Ta = –20°C to +75°C, V_{SS1} = V_{SS2} = 0V)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Digital supply voltage	V_{DD1}	2.7	3.0	3.6	V
Analog supply voltage	V_{DD2}	6.4	9.0	13.0	V
Gamma reference voltage	VGMA1 to VGMA18	+0.2	–	V_{DD2}-0.2	V
Driver part output voltage	Vyo	+0.2	–	V_{DD2}-0.2	V
Max. clock frequency	*Note fmax	–	–	65	MHz
Output Load capacitance	CL	–	–	150	pF

NOTE:V_{DD1} = 2.7V

DC CHARACTERISTICS

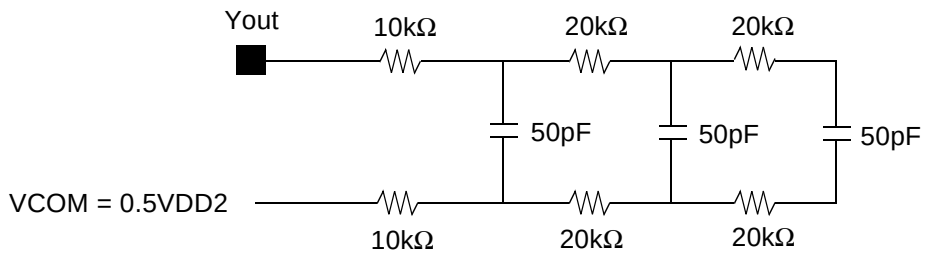
(Ta = –20 to +75°C, V_{DD1} = 2.7 to 3.6V, V_{DD2} = 6.4 to 13.0V, V_{SS1} = V_{SS2} = 0V)

Characteristics	Symbol	Condition	Min.	Typ.	Max.	Unit
High level input voltage	VIH	SHL, CLK2, D00 to D55, DATPOL, CLK1, POL, DIO1(DIO2)	$0.8V_{DD1}$	–	V_{DD1}	V
Low level input voltage	VIL		0	–	$0.2V_{DD1}$	
Input leak current	IL	D00 to D55, SHL, CLK2, CLK1 DATPOL, POL, Dio1 (Dio2)	–1	–	1	µA
High level output voltage	VOH	DIO1(DIO2), IO = –1.0mA	V_{DD1}-0.5	–	–	V
Low level output voltge	VOL	DIO1(DIO2), IO = +1.0mA	–	–	0.5	
Resistance between gamma referen voltage	RO to R63	* refer to page 17 resistance ladder circuit	Rn x 0.77	* refer to page 17	Rn x 1.3	Ω
Driver output current	IVOH	V_{DD2} = 13.0V, Vx = 3.5V, Vyo = 9.5V	–	–0.4	–0.3	mA
	IVOL	V_{DD2} = 13.0V, Vx = 7.5V, Vyo = 1.5V	0.3	0.4	–	mA
Output voltage deviation	ΔVO	Input data: 00H to 3FH	–	±10	±20	mV
Output voltage range	VYO	Input data: 00H to 3FH	V_{SS2}+0.2	-	V_{DD2}-0.2	V
Logic part dynamic current consumption	IDD1	*Note1: V_{DD1} = 3.0V	–	4.0	5.5	mA
Driver part dynamic current consumption	IDD2	V_{DD1} = 3.0V, V_{DD2} = 9.0V, VGMA1 = 8.5V, VGMA9 = 5.0V VGMA10 = 4.0V, VGMA18 = 0.5V *Note1, *Note2, *Note3	–	8.0	10.0	

(Vyo is the output voltage of analog output pins Y1 to Y384.)
(Vx is the applied voltage of analog output pins Y1 to Y384.)

NOTES:

1. CLK1 cycle =20µs, fCLK2 = 33MHz,data pattern = 1010 ... (Checkerboard pattern) applied, Ta = 25°C
2. The current consumption per driver in case of XGA single-bank connection.
3. Yout Load Condition



AC CHARACTERISTICS

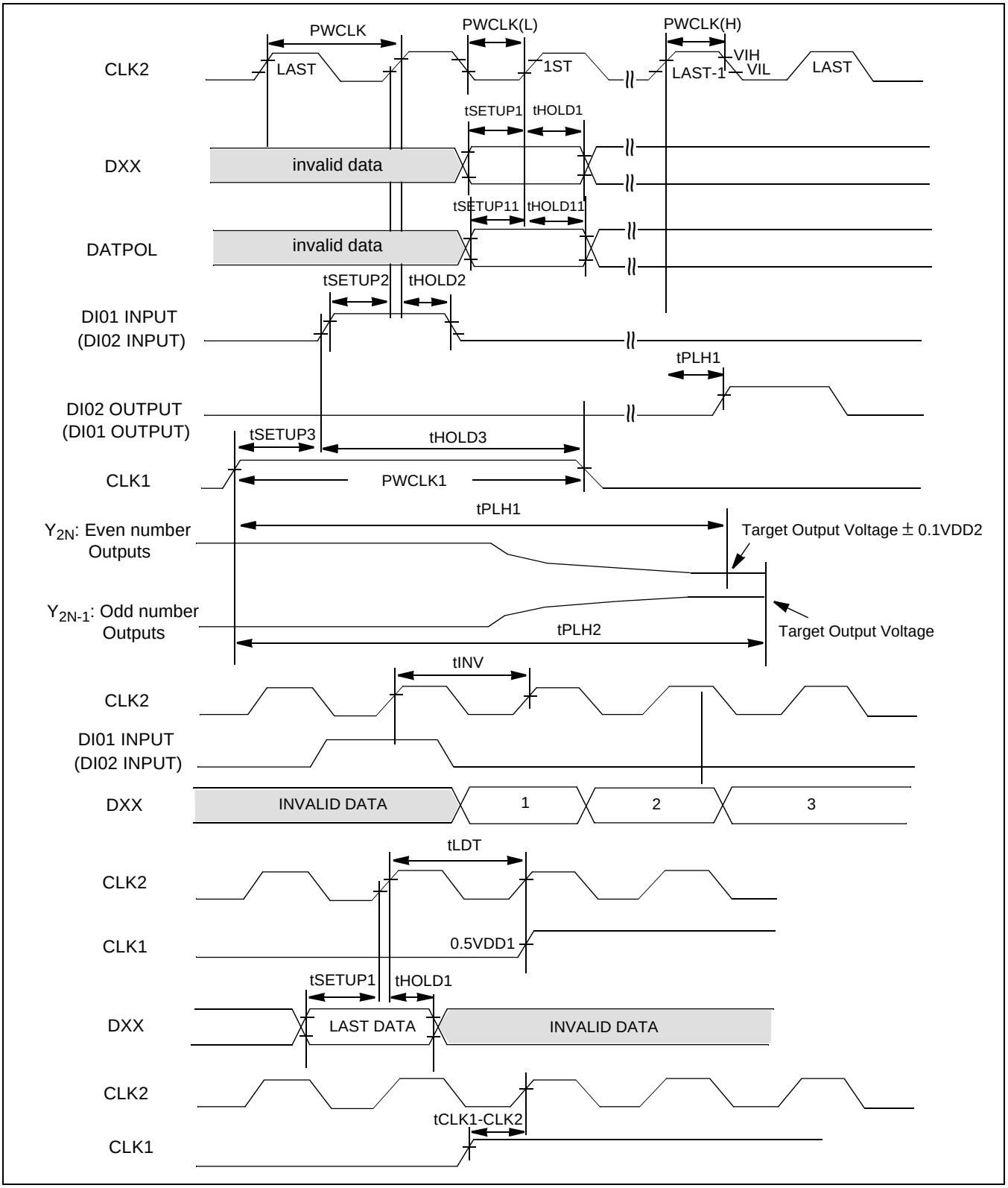
(Ta = –20 to +75°C, V_{DD1} = 2.7 to 3.6V, V_{DD2} = 6.4 to 13.0V, V_{SS1} = V_{SS2} = 0V)

Characteristics	Symbol	Condition	Min.	Typ.	Max.	Unit
Clock pulse width	PWCLK	–	15	–	–	ns
Clock pulse low period	PWCLK(L)	–	5	–	–	
Clock pulse high period	PWCLK(H)	–	5	–	–	
Data setup time	tSETUP1	–	5	–	–	
Data hold time	tHOLD1	–	0	–	–	
Start pulse setup time	tSETUP2	–	5	–	–	
Start pulse hold time	tHOLD2	–	0	–	–	
DATPOL-CLK2 setup time	tSETUP 11	–	5	–	–	
DATPOL-CLK2 hold time	tHOLD 11	–	0	–	–	
Start pulse delay time	tPLH1	CL=20pF	-	–	16	
CLK1 setup time	tSETUP3	–	1	–	–	CLK2cycle
CLK1 high pulse width	PWCLK1	–	3	–	–	
Driver output delay time 1	tPHL1	refer to Note 3 (page 6), Note 4	–	–	5	ms
Driver output delay time 2	tPHL2	refer to Note 3 (page 6), Note 5	–	–	10	
Data invalid time	tINV	Note 6	1	–	–	CLK2cycle
Last data time	tLDT	–	1	–	–	
CLK1-CLK2 time	tCLK1-CLK2	CLK 1 ↑ → CLK2 ↑	6	–	–	ns
POL-CLK1 time	tPOL-CLK1	POL ↑ or ↓ → CLK2 ↑	–9	–	–	ns

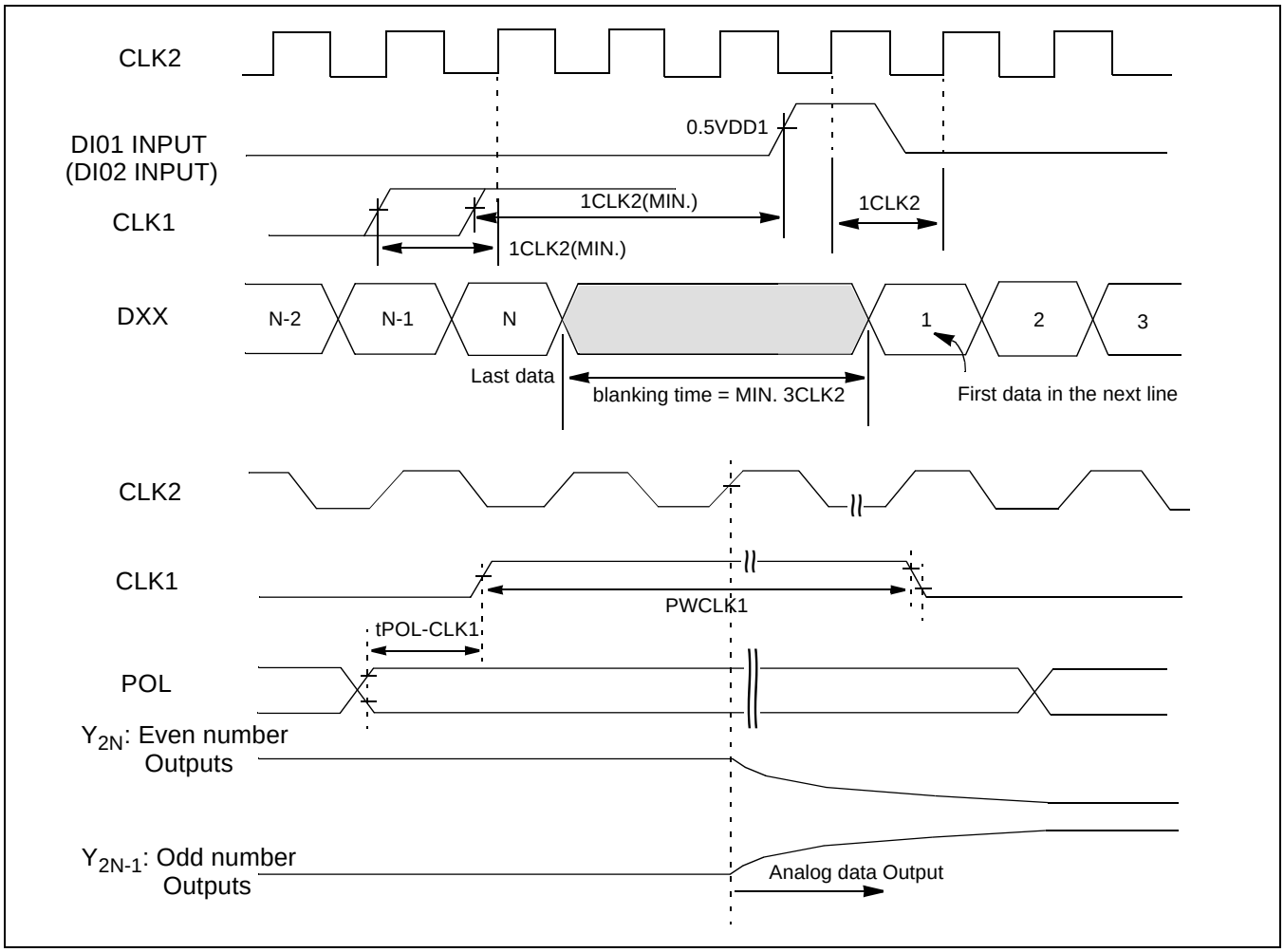
NOTES:

4. The value is specified when the drive voltage value reaches the target output voltage level of 90%.
5. The value is specified when the drive voltage value reaches the target output voltage level of 6-bit accuracy.
6. Set the first rising edge of the CLK2 after the rising edge of DI01 (or DI02).

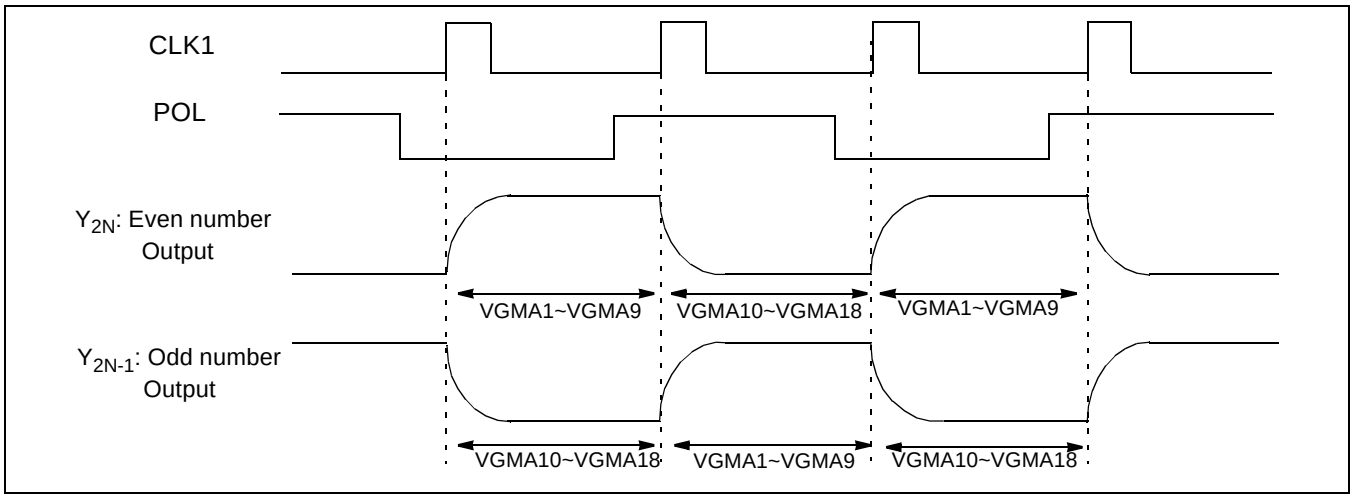
AC Waveform (VIH=0.8V_{DD1}, VIL=0.2V_{DD1})



Relationship between CLK1/start pulse(DIO1,DIO2) and blanking period



Relationship between CLK1, POL and output



RELATIONSHIP BETWEEN THE INPUT DATA AND OUTPUT VOLTAGE

RELATIONSHIP # 1 BETWEEN INPUT DATA AND OUTPUT VOLTAGE

The output voltage is determined by the digital input data, the gamma reference voltages, and the signal POL. The input data determines the analog voltage signal level, which refers to the gamma reference voltages. The gamma reference voltages, VGMA1-18, must be externally supported in order to operate the dot inversion, which can apply the gray scale voltage with the opposite polarity to each adjacent dot. When a dot has a positive polarity, the analog voltage signal with VGMA1-9(high region) transfers to the output terminal and when a dot has a negative polarity, the analog voltage signal with VGMA10-18 (low region) transfer to the output terminal.data format: 6-bits data × 3 colors × 2 port
Input width: 36 bits

- Details on 6-bits digital input data

DX5	DX4	DX3	DX2	DX1	DX0
Upper bits					Lower bits

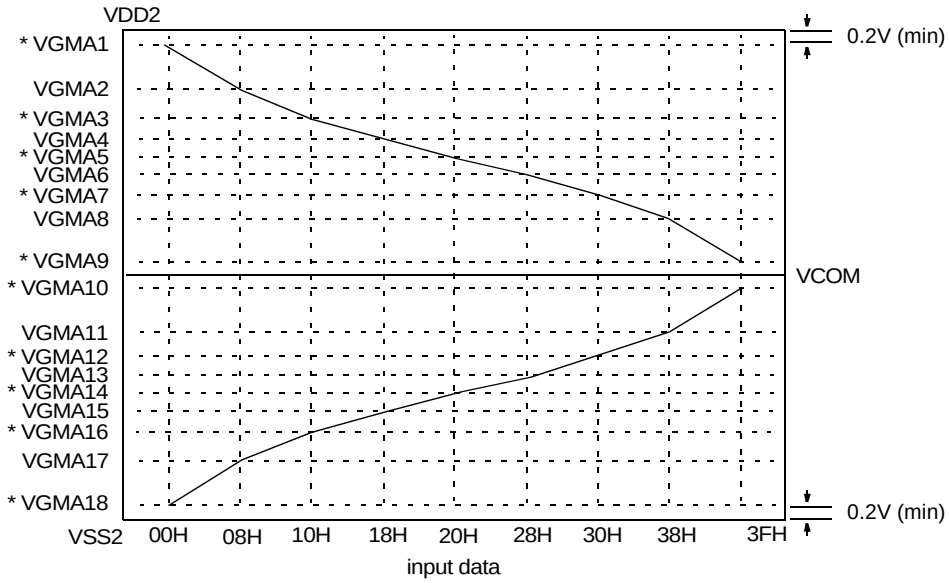
- Relationship between shift direction and output data
  SHL=H (Right shift)

Output	Y1	Y2	Y3	.....	Y382	Y383	Y384
–	First			→	Last		
DATA	D00 to D05	D10 to D15	D20 to D25	.....	D30 to D35	D40 to D45	D50 to 55

SHL=L (Left shift)

Output	Y1	Y2	Y3	.....	Y382	Y383	Y384
–	Last			←	First		
DATA	D00 to D05	D10 to D15	D20 to D25	.....	D30 to D35	D40 to D45	D50 to 55

Gamma reference voltage vs Input data value



When the total number of the reference voltages in ten, the device only used the pins which are marked with "*" picture above.

RELATIONSHIP #2 BETWEEN INPUT DATA AND OUTPUT VOLTAGE (1)

VGMA1>VGMA2>VGMA3>VGMA4>VGMA5>VGMA6>VGMA7>VGMA8>VGM9

Input data	DX5	DX4	DX3	DX2	DX1	DX0	Output Voltage	
00H	0	0	0	0	0	0	V0	VGMA1
01H	0	0	0	0	0	1	V1	VGMA1+(VGMA2-VGMA1) × 1/8
02H	0	0	0	0	1	0	V2	VGMA1+(VGMA2-VGMA1) × 2/8
03H	0	0	0	0	1	1	V3	VGMA1+(VGMA2-VGMA1) × 3/8
04H	0	0	0	1	0	0	V4	VGMA1+(VGMA2-VGMA1) × 4/8
05H	0	0	0	1	0	1	V5	VGMA1+(VGMA2-VGMA1) × 5/8
06H	0	0	0	1	1	0	V6	VGMA1+(VGMA2-VGMA1) × 6/8
07H	0	0	0	1	1	1	V7	VGMA1+(VGMA2-VGMA1) × 7/8
08H	0	0	1	0	0	0	V8	VGMA2
09H	0	0	1	0	0	1	V9	VGMA2+(VGMA3-VGMA2) × 500/3670
0AH	0	0	1	0	1	0	V10	VGMA2+(VGMA3-VGMA2) × 1000/3670
0BH	0	0	1	0	1	1	V11	VGMA2+(VGMA3-VGMA2) × 1500/3670
0CH	0	0	1	1	0	0	V12	VGMA2+(VGMA3-VGMA2) × 2000/3670
0DH	0	0	1	1	0	1	V13	VGMA2+(VGMA3-VGMA2) × 2450/3670
0EH	0	0	1	1	1	0	V4	VGMA2+(VGMA3-VGMA2) × 2900/3670
0FH	0	0	1	1	1	1	V15	VGMA2+(VGMA3-VGMA2) × 3300/3670
10H	0	1	0	0	0	0	V16	VGMA3
11H	0	1	0	0	0	1	V17	VGMA3+(VGMA4-VGMA3) × 330/2420
12H	0	1	0	0	1	0	V18	VGMA3+(VGMA4-VGMA3) × 660/2420
13H	0	1	0	0	1	1	V19	VGMA3+(VGMA4-VGMA3) × 990/2420
14H	0	1	0	1	0	0	V20	VGMA3+(VGMA4-VGMA3) × 1310/2420
15H	0	1	0	1	0	1	V21	VGMA3+(VGMA4-VGMA3) × 1610/2420
16H	0	1	0	1	1	0	V22	VGMA3+(VGMA4-VGMA3) × 1890/2420
17H	0	1	0	1	1	1	V23	VGMA3+(VGMA4-VGMA3) × 2160/2420
18H	0	1	1	0	0	0	V24	VGMA4
19H	0	1	1	0	0	1	V25	VGMA4+(VGMA5-VGMA4) × 250/1720
1AH	0	1	1	0	1	0	V26	VGMA4+(VGMA5-VGMA4) × 490/1720
1BH	0	1	1	0	1	1	V27	VGMA4+(VGMA5-VGMA4) × 720/1720
1CH	0	1	1	1	0	0	V28	VGMA4+(VGMA5-VGMA4) × 940/1720
1DH	0	1	1	1	0	1	V29	VGMA4+(VGMA5-VGMA4) × 1150/1720
1EH	0	1	1	1	1	0	V30	VGMA4+(VGMA5-VGMA4) × 1350/1720
1FH	0	1	1	1	1	1	V31	VGMA4+(VGMA5-VGMA4) × 1540/1720

RELATIONSHIP #2 BETWEEN INPUT DATA AND OUTPUT VOLTAGE (1) (Continued)

VGMA1>VGMA2>VGMA3>VGMA4>VGMA5>VGMA6>VGMA7>VGMA8>VGM9

Input data	DX5	DX4	DX3	DX2	DX1	DX0	Output Voltage	
20H	1	0	0	0	0	0	V32	VGMA5
21H	1	0	0	0	0	1	V33	VGMA5+(VGMA6-VGMA5) × 175/1350
22H	1	0	0	0	1	0	V34	VGMA5+(VGMA6-VGMA5) × 350/1350
23H	1	0	0	0	1	1	V35	VGMA5+(VGMA6-VGMA5) × 520/1350
24H	1	0	0	1	0	0	V36	VGMA5+(VGMA6-VGMA5) × 690/1350
25H	1	0	0	1	0	1	V37	VGMA5+(VGMA6-VGMA5) × 855/1350
26H	1	0	0	1	1	0	V38	VGMA5+(VGMA6-VGMA5) × 1020/1350
27H	1	0	0	1	1	1	V39	VGMA5+(VGMA6-VGMA5) × 1185/1350
28H	1	0	1	0	0	0	V40	VGMA6
29H	1	0	1	0	0	1	V41	VGMA6+(VGMA7-VGMA6) × 170/1415
2AH	1	0	1	0	1	0	V42	VGMA6+(VGMA7-VGMA6) × 340/1415
2BH	1	0	1	0	1	1	V43	VGMA6+(VGMA7-VGMA6) × 510/1415
2CH	1	0	1	1	0	0	V44	VGMA6+(VGMA7-VGMA6) × 685/1415
2DH	1	0	1	1	0	1	V45	VGMA6+(VGMA7-VGMA6) × 860/1415
2EH	1	0	1	1	1	0	V46	VGMA6+(VGMA7-VGMA6) × 1035/1415
2FH	1	0	1	1	1	1	V47	VGMA6+(VGMA7-VGMA6) × 1215/1415
30H	1	1	0	0	0	0	V48	VGMA7
31H	1	1	0	0	0	1	V49	VGMA7+(VGMA8-VGMA7) × 210/1970
32H	1	1	1	0	1	0	V50	VGMA7+(VGMA8-VGMA7) × 430/1970
33H	1	1	0	0	1	1	V51	VGMA7+(VGMA8-VGMA7) × 660/1970
34H	1	1	0	1	0	0	V52	VGMA7+(VGMA8-VGMA7) × 900/1970
35H	1	1	0	1	0	1	V53	VGMA7+(VGMA8-VGMA7) × 1150/1970
36H	1	1	0	1	1	0	V54	VGMA7+(VGMA8-VGMA7) × 1410/1970
37H	1	1	0	1	1	1	V55	VGMA7+(VGMA8-VGMA7) × 1680/1970
38H	1	1	1	0	0	0	V56	VGMA8
39H	1	1	1	0	0	1	V57	VGMA8+(VGMA9-VGMA8) × 300/2290
3AH	1	1	1	0	1	0	V58	VGMA8+(VGMA9-VGMA8) × 610/2290
3BH	1	1	1	0	1	1	V59	VGMA8+(VGMA9-VGMA8) × 930/2290
3CH	1	1	1	1	0	0	V60	VGMA8+(VGMA9-VGMA8) × 1270/2290
3DH	1	1	1	1	0	1	V61	VGMA8+(VGMA9-VGMA8) × 1610/2290
3EH	1	1	1	1	1	0	V62	VGMA8+(VGMA9-VGMA8) × 1950/2290
3FH	1	1	1	1	1	1	V63	VGMA9

RELATIONSHIP #2 BETWEEN INPUT DATA AND OUTPUT VOLTAGE (2)

VGMA18>VGMA17>VGMA16>VGMA15>VGMA14>VGMA13>VGMA12>VGMA11>VGMA11

Input data	DX5	DX4	DX3	DX2	DX1	DX0	Output Voltage	
00H	0	0	0	0	0	0	V0’	VGMA18
01H	0	0	0	0	0	1	V1’	VGMA18+(VGMA17-VGMA18) × 1/8
02H	0	0	0	0	1	0	V2’	VGMA18+(VGMA17-VGMA18) × 2/8
03H	0	0	0	0	1	1	V3’	VGMA18+(VGMA17-VGMA18) × 3/8
04H	0	0	0	1	0	0	V4’	VGMA18+(VGMA17-VGMA18) × 4/8
05H	0	0	0	1	0	1	V5’	VGMA18+(VGMA17-VGMA18) × 5/8
06H	0	0	0	1	1	0	V6’	VGMA18+(VGMA17-VGMA18) × 6/8
07H	0	0	0	1	1	1	V7’	VGMA18+(VGMA17-VGMA18) × 7/8
08H	0	0	1	0	0	0	V8’	VGMA17
09H	0	0	1	0	0	1	V9’	VGMA17+(VGMA16-VGMA17) × 500/3670
0AH	0	0	1	0	1	0	V10’	VGMA17+(VGMA16-VGMA17) × 1000/3670
0BH	0	0	1	0	1	1	V11’	VGMA17+(VGMA16-VGMA17) × 1500/3670
0CH	0	0	1	1	0	0	V12’	VGMA17+(VGMA16-VGMA17) × 2000/3670
0DH	0	0	1	1	0	1	V13’	VGMA17+(VGMA16-VGMA17) × 2450/3670
0EH	0	0	1	1	1	0	V4’	VGMA17+(VGMA16-VGMA17) × 2900/3670
0FH	0	0	1	1	1	1	V15’	VGMA17+(VGMA16-VGMA17) × 3300/3670
10H	0	1	0	0	0	0	V16’	VGMA16
11H	0	1	0	0	0	1	V17’	VGMA16+(VGMA15-VGMA16) × 330/2420
12H	0	1	0	0	1	0	V18’	VGMA16+(VGMA15-VGMA16) × 660/2420
13H	0	1	0	0	1	1	V19’	VGMA16+(VGMA15-VGMA16) × 990/2420
14H	0	1	0	1	0	0	V20’	VGMA16+(VGMA15-VGMA16) × 1310/2420
15H	0	1	0	1	0	1	V21’	VGMA16+(VGMA15-VGMA16) × 1610/2420
16H	0	1	0	1	1	0	V22’	VGMA16+(VGMA15-VGMA16) × 1890/2420
17H	0	1	0	1	1	1	V23’	VGMA16+(VGMA15-VGMA16) × 2160/2420
18H	0	1	1	0	0	0	V24’	VGMA15
19H	0	1	1	0	0	1	V25’	VGMA15+(VGMA14-VGMA15) × 250/1720
1AH	0	1	1	0	1	0	V26’	VGMA15+(VGMA14-VGMA15) × 490/1720
1BH	0	1	1	0	1	1	V27’	VGMA15+(VGMA14-VGMA15) × 720/1720
1CH	0	1	1	1	0	0	V28’	VGMA15+(VGMA14-VGMA15) × 940/1720
1DH	0	1	1	1	0	1	V29’	VGMA15+(VGMA14-VGMA15) × 1150/1720
1EH	0	1	1	1	1	0	V30’	VGMA15+(VGMA14-VGMA15) × 1350/1720
1FH	0	1	1	1	1	1	V31’	VGMA15+(VGMA14-VGMA15) × 1540/1720

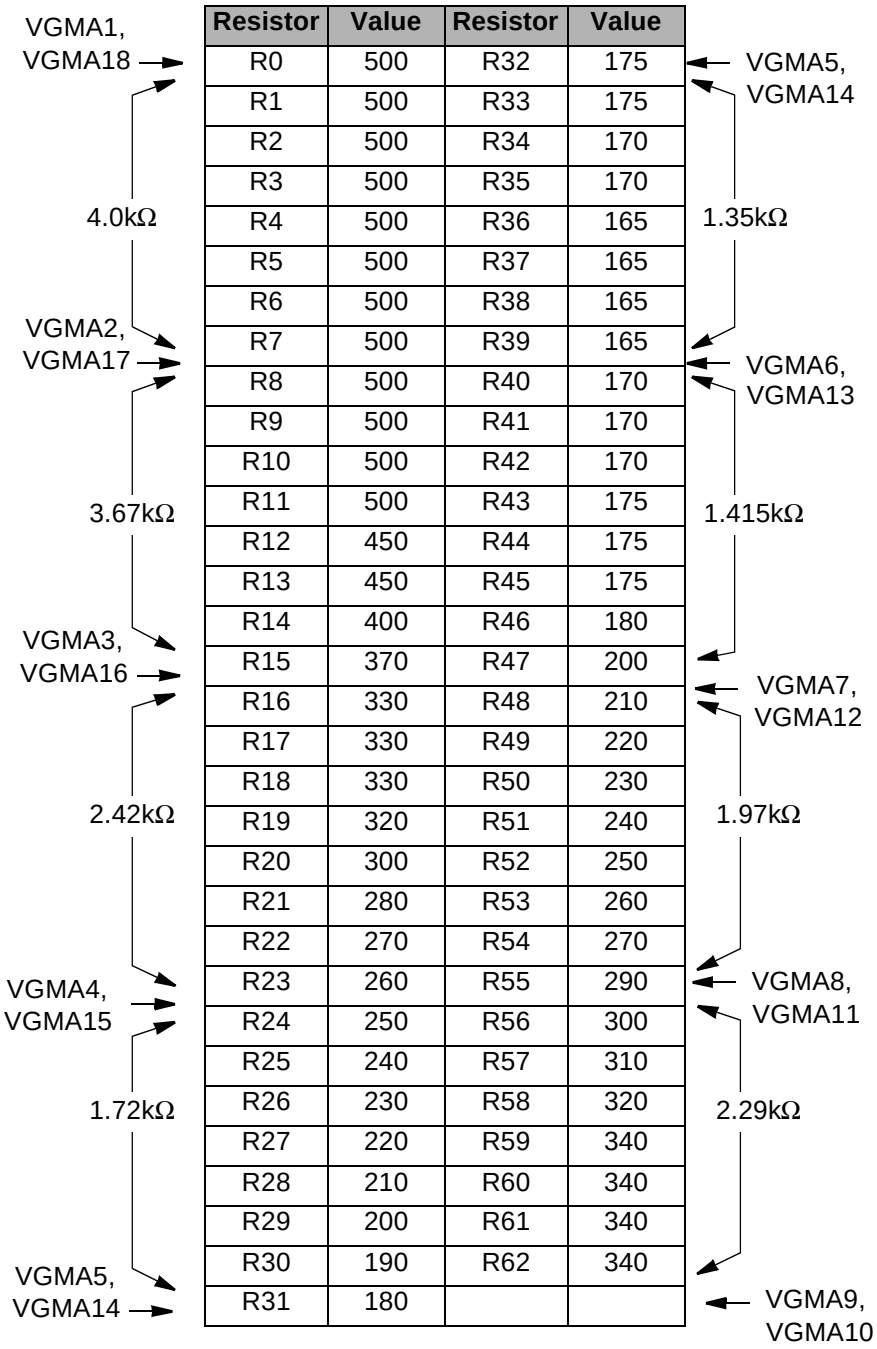
RELATIONSHIP #2 BETWEEN INPUT DATA AND OUTPUT VOLTAGE (2) (Continued)

VGMA18>VGMA17>VGMA16>VGMA15>VGMA14>VGMA13>VGMA12>VGMA11>VGMA11

Input data	DX5	DX4	DX3	DX2	DX1	DX0	Output Voltage	
20H	1	0	0	0	0	0	V32’	VGMA14
21H	1	0	0	0	0	1	V33’	VGMA14+(VGMA13-VGMA14) × 175/1350
22H	1	0	0	0	1	0	V34’	VGMA14+(VGMA13-VGMA14) × 350/1350
23H	1	0	0	0	1	1	V35’	VGMA14+(VGMA13-VGMA14) × 520/1350
24H	1	0	0	1	0	0	V36’	VGMA14+(VGMA13-VGMA14) × 690/1350
25H	1	0	0	1	0	1	V37’	VGMA14+(VGMA13-VGMA14) × 855/1350
26H	1	0	0	1	1	0	V38’	VGMA14+(VGMA13-VGMA14) × 1020/1350
27H	1	0	0	1	1	1	V39’	VGMA14+(VGMA13-VGMA14) × 1185/1350
28H	1	0	1	0	0	0	V40’	VGMA13
29H	1	0	1	0	0	1	V41’	VGMA13+(VGMA12-VGMA13) × 170/1415
2AH	1	0	1	0	1	0	V42’	VGMA13+(VGMA12-VGMA13) × 340/1415
2BH	1	0	1	0	1	1	V43’	VGMA13+(VGMA12-VGMA13) × 510/1415
2CH	1	0	1	1	0	0	V44’	VGMA13+(VGMA12-VGMA13) × 685/1415
2DH	1	0	1	1	0	1	V45’	VGMA13+(VGMA12-VGMA13) × 860/1415
2EH	1	0	1	1	1	0	V46’	VGMA13+(VGMA12-VGMA13) × 1035/1415
2FH	1	0	1	1	1	1	V47’	VGMA13+(VGMA12-VGMA13) × 1215/1415
30H	1	1	0	0	0	0	V48’	VGMA12
31H	1	1	0	0	0	1	V49’	VGMA12+(VGMA11-VGMA12) × 210/1970
32H	1	1	1	0	1	0	V50’	VGMA12+(VGMA11-VGMA12) × 430/1970
33H	1	1	0	0	1	1	V51’	VGMA12+(VGMA11-VGMA12) × 660/1970
34H	1	1	0	1	0	0	V52’	VGMA12+(VGMA11-VGMA12) × 900/1970
35H	1	1	0	1	0	1	V53’	VGMA12+(VGMA11-VGMA12) × 1150/1970
36H	1	1	0	1	1	0	V54’	VGMA12+(VGMA11-VGMA12) × 1410/1970
37H	1	1	0	1	1	1	V55’	VGMA12+(VGMA11-VGMA12) × 1680/1970
38H	1	1	1	0	0	0	V56’	VGMA11
39H	1	1	1	0	0	1	V57’	VGMA11+(VGMA10-VGMA11) × 300/2290
3AH	1	1	1	0	1	0	V58’	VGMA11+(VGMA10-VGMA11) × 610/2290
3BH	1	1	1	0	1	1	V59’	VGMA11+(VGMA10-VGMA11) × 930/2290
3CH	1	1	1	1	0	0	V60’	VGMA11+(VGMA10-VGMA11) × 1270/2290
3DH	1	1	1	1	0	1	V61’	VGMA11+(VGMA10-VGMA11) × 1610/2290
3EH	1	1	1	1	1	0	V62’	VGMA11+(VGMA10-VGMA11) × 1950/2290
3FH	1	1	1	1	1	1	V63’	VGMA10

Gamma reference voltage generator and relationship input data and output voltage.

* Ladder Resistance Value (R0~R63, Unit: Ω)



Resistor	Value	Resistor	Value
R0	500	R32	175
R1	500	R33	175
R2	500	R34	170
R3	500	R35	170
R4	500	R36	165
R5	500	R37	165
R6	500	R38	165
R7	500	R39	165
R8	500	R40	170
R9	500	R41	170
R10	500	R42	170
R11	500	R43	175
R12	450	R44	175
R13	450	R45	175
R14	400	R46	180
R15	370	R47	200
R16	330	R48	210
R17	330	R49	220
R18	330	R50	230
R19	320	R51	240
R20	300	R52	250
R21	280	R53	260
R22	270	R54	270
R23	260	R55	290
R24	250	R56	300
R25	240	R57	310
R26	230	R58	320
R27	220	R59	340
R28	210	R60	340
R29	200	R61	340
R30	190	R62	340
R31	180