INTRODUCTION

The KS0093 is an LCD driver and controller LSI for liquid crystal dot matrix character display systems. It can display 2 to 3 lines of 16 characters with a 5×8 dots format. It is capable of interfacing various micro processors, supporting the 4-bit, 8-bit parallel modes and the clock synchronized serial mode. Voltage converter, oscillator, voltage regulator, voltage follower and bias circuit are built in the IC. The double height character mode and line vertical scroll function are supported.

FEATURES

- **Driver outputs**
  - — Common outputs: 26 common
  - — Segment outputs: 80 segment
- **Applicable panel size**

Font	Display Size	Duty	Contents of Outputs
5×8	2 line × 16 char.	1/17	2×16 characters + 80 icons
	3 line × 16 char.	1/25	3×16 characters + 80 icons

- **Internal memory**
  - — Character generator ROM (CGROM): 10,240 bits (256 characters × 5 × 8 dot)
  - — Character generator RAM (CGRAM): 320 bits (8 characters × 5 × 8 dot)
  - — Display data RAM (DDRAM): 512 bits (16 characters × 4 lines)
  - — Segment icon RAM (ICONRAM): 80 bits (80 icon)
- **MPU interface**
  - — No busy MPU interface (No busy check or no execution waiting time)
  - — 8-/4-bit parallel interface mode: 68-series, 80-series are available
  - — Serial interface mode: 4 pin clock synchronous serial interface
- **Function set**
  - — Various instruction set: Display control, Power save, Power control ... etc.
  - — COM/SEG bi-directional (4 type LCD application available)
  - — H/W Reset (RESETB)
- **Built-in analog circuit**
  - — Internal RC oscillator circuit or external clock
  - — Electronic volume for contrast control (32 steps)
  - — Voltage converter / Voltage regulator / Voltage follower & Bias circuit

- **Low power operation**
  - — Sleep mode operation (5μA Max.)
  - — Normal mode operation (80μA Max.)
- **Operating voltage range**
  - — Power supply voltage (VDD): 2.4V to 5.5V
  - — LCD driving voltage (VLCD = V0 – VSS): 6.0V Max.
- **Package type**
  - — Bumped chip / TCP

BLOCK DIAGRAM

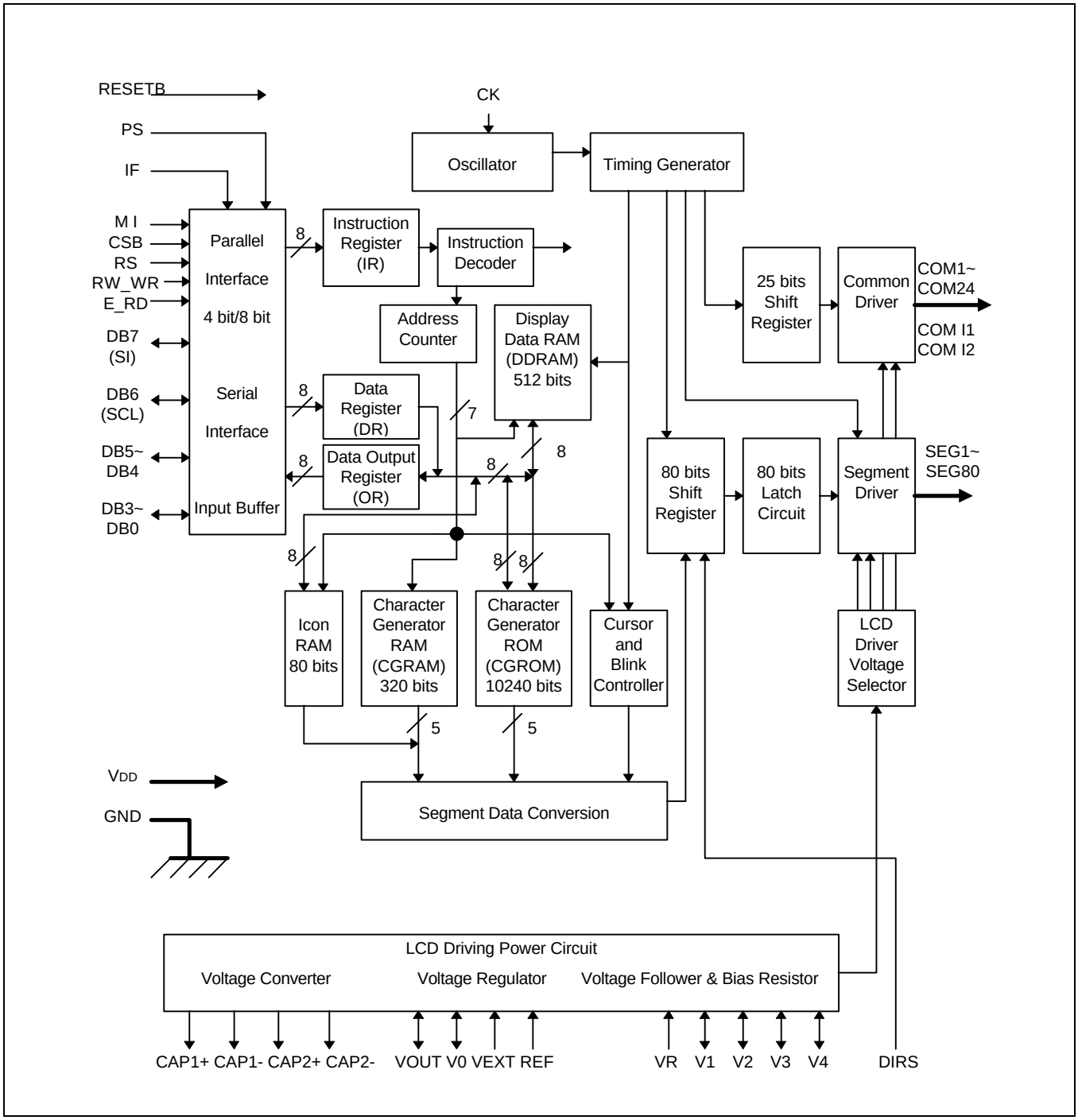


Figure 1. Block Diagram

PAD CONFIGURATION (NOT FIXED)

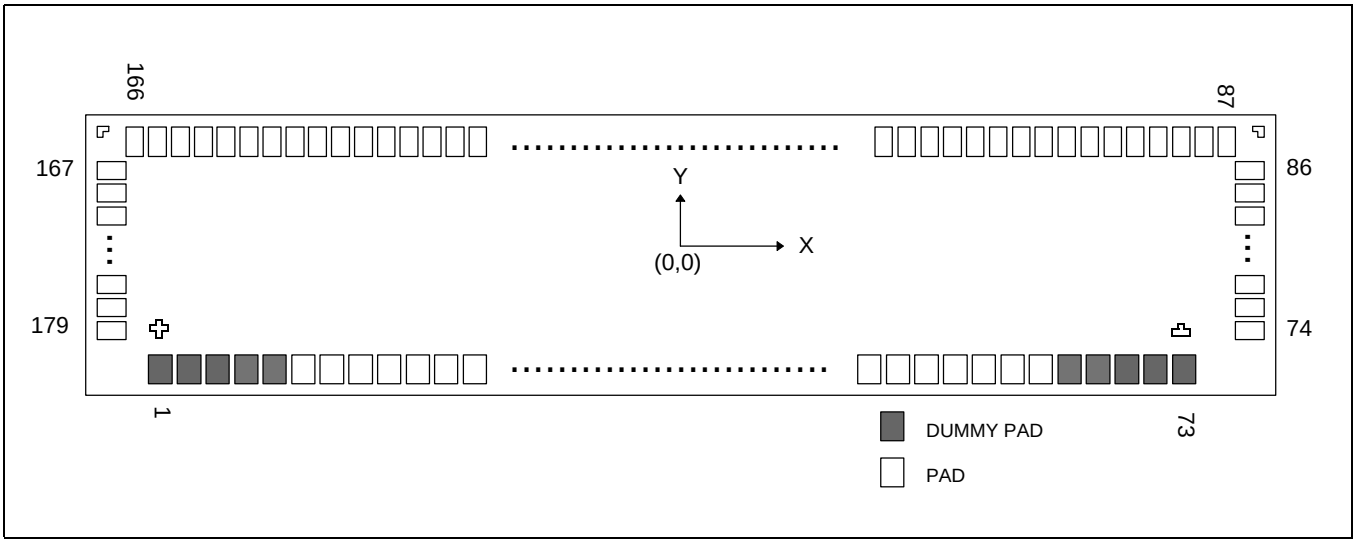


Figure 2. Pad Configuration

Item	Pad No.	Size		Unit
		X	Y	
Chip size	–	7020	1620	μm
Pad pitch	1 to 73	90		
	74 to 179	80		
Bumped pad size	1 to 73	60	100	
	74 to 86	100	50	
	87 to 166	50	100	
	167 to 179	100	50	
Bumped pad height	All pad	17		

PAD LOCATION

[Unit: μm]

Pad No.	Pad Name	Coordinate		Pad No.	Pad Name	Coordinate		Pad No.	Pad Name	Coordinate	
		X	Y			X	Y			X	Y
1	DUMMY	-3240	-700	61	PS	2160	-700	121	SEG35	440	700
2	DUMMY	-3150	-700	62	VDD	2250	-700	122	SEG36	360	700
3	DUMMY	-3060	-700	63	IF	2340	-700	123	SEG37	280	700
4	DUMMY	-2970	-700	64	VSS	2430	-700	124	SEG38	200	700
5	DUMMY	-2880	-700	65	MI	2520	-700	125	SEG39	120	700
6	RS	-2790	-700	66	VDD	2610	-700	126	SEG40	40	700
7	VSS	-2700	-700	67	RESETB	2700	-700	127	SEG41	-40	700
8	RW_WR	-2610	-700	68	TEST	2790	-700	128	SEG42	-120	700
9	VDD	-2520	-700	69	DUMMY	2880	-700	129	SEG43	-200	700
10	E_RD	-2430	-700	70	DUMMY	2970	-700	130	SEG44	-280	700
11	CSB	-2340	-700	71	DUMMY	3060	-700	131	SEG45	-360	700
12	DB7	-2250	-700	72	DUMMY	3150	-700	132	SEG46	-440	700
13	DB6	-2160	-700	73	DUMMY	3240	-700	133	SEG47	-520	700
14	DB5	-2070	-700	74	COMI1	3400	-520	134	SEG48	-600	700
15	DB4	-1980	-700	75	COM1	3400	-440	135	SEG49	-680	700
16	DB3	-1890	-700	76	COM2	3400	-360	136	SEG50	-760	700
17	DB2	-1800	-700	77	COM3	3400	-280	137	SEG51	-840	700
18	DB1	-1710	-700	78	COM4	3400	-200	138	SEG52	-920	700
19	DB0	-1620	-700	79	COM5	3400	-120	139	SEG53	-1000	700
20	VDD	-1530	-700	80	COM6	3400	-40	140	SEG54	-1080	700
21	VDD	-1440	-700	81	COM7	3400	40	141	SEG55	-1160	700
22	VDD	-1350	-700	82	COM8	3400	120	142	SEG56	-1240	700
23	VSS	-1260	-700	83	COM17	3400	200	143	SEG57	-1320	700
24	VSS	-1170	-700	84	COM18	3400	280	144	SEG58	-1400	700
25	VSS	-1080	-700	85	COM19	3400	360	145	SEG59	-1480	700
26	V4	-990	-700	86	COM20	3400	440	146	SEG60	-1560	700
27	V4	-900	-700	87	SEG1	3160	700	147	SEG61	-1640	700
28	V3	-810	-700	88	SEG2	3080	700	148	SEG62	-1720	700
29	V3	-720	-700	89	SEG3	3000	700	149	SEG63	-1800	700
30	V2	-630	-700	90	SEG4	2920	700	150	SEG64	-1880	700
31	V2	-540	-700	91	SEG5	2840	700	151	SEG65	-1960	700
32	V1	-450	-700	92	SEG6	2760	700	152	SEG66	-2040	700
33	V1	-360	-700	93	SEG7	2680	700	153	SEG67	-2120	700
34	V0	-270	-700	94	SEG8	2600	700	154	SEG68	-2200	700
35	V0	-180	-700	95	SEG9	2520	700	155	SEG69	-2280	700
36	V0	-90	-700	96	SEG10	2440	700	156	SEG70	-2360	700
37	V0	0	-700	97	SEG11	2360	700	157	SEG71	-2440	700
38	VR	90	-700	98	SEG12	2280	700	158	SEG72	-2520	700
39	VR	180	-700	99	SEG13	2200	700	159	SEG73	-2600	700
40	VOUT	270	-700	100	SEG14	2120	700	160	SEG74	-2680	700
41	VOUT	360	-700	101	SEG15	2040	700	161	SEG75	-2760	700
42	CAP2-	450	-700	102	SEG16	1960	700	162	SEG76	-2840	700
43	CAP2-	540	-700	103	SEG17	1880	700	163	SEG77	-2920	700
44	CAP2+	630	-700	104	SEG18	1800	700	164	SEG78	-3000	700
45	CAP2+	720	-700	105	SEG19	1720	700	165	SEG79	-3080	700
46	CAP1-	810	-700	106	SEG20	1640	700	166	SEG80	-3160	700
47	CAP1-	900	-700	107	SEG21	1560	700	167	COMI2	-3400	440
48	CAP1+	990	-700	108	SEG22	1480	700	168	COM24	-3400	360
49	CAP1+	1080	-700	109	SEG23	1400	700	169	COM23	-3400	280
50	VEXT	1170	-700	110	SEG24	1320	700	170	COM22	-3400	200
51	VSS	1260	-700	111	SEG25	1240	700	171	COM21	-3400	120
52	VSS	1350	-700	112	SEG26	1160	700	172	COM16	-3400	40
53	VSS	1440	-700	113	SEG27	1080	700	173	COM15	-3400	-40
54	REF	1530	-700	114	SEG28	1000	700	174	COM14	-3400	-120
55	DIRS	1620	-700	115	SEG29	920	700	175	COM13	-3400	-200
56	VDD	1710	-700	116	SEG30	840	700	176	COM12	-3400	-280
57	VDD	1800	-700	117	SEG31	760	700	177	COM11	-3400	-360
58	VDD	1890	-700	118	SEG32	680	700	178	COM10	-3400	-440
59	CK	1980	-700	119	SEG33	600	700	179	COM9	-3400	-520
60	VSS	2070	-700	120	SEG34	520	700				

PIN DESCRIPTIONS

Table 1. Pin Description

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td colspan="3">Power Supply</td></tr>
<tr><td>VDD</td><td>Power</td><td>Power supply
Connect to MPU power supply pin.</td></tr>
<tr><td>VSS</td><td></td><td>0V (GND)</td></tr>
<tr><td>V0
V1
V2
V3
V4</td><td>I/O</td><td>Bias voltage level for LCD driving.
Voltages should have the following relationship:

V0 ≥ V1 ≥ V2 ≥ V3 ≥ V4 ≥ VSS

When the built-in power circuit is active, internal 1/4 or 1/5 bias resisters are used.
<table>
<tr><th>LCD Bias</th><th>V1</th><th>V2</th><th>V3</th><th>V4</th></tr>
<tr><td>1/5 Bias</td><td>(4/5) V0</td><td>(3/5) V0</td><td>(2/5) V0</td><td>(1/5) V0</td></tr>
<tr><td>1/4 Bias</td><td>(3/4) V0</td><td colspan="2">(1/2) V0</td><td>(1/4) V0</td></tr>
</table></td></tr>
<tr><td colspan="3">LCD Driver Supply</td></tr>
<tr><td>CAP1+</td><td>O</td><td>Capacitor1+ connecting pin for the internal voltage converter</td></tr>
<tr><td>CAP1–</td><td></td><td>Capacitor1– connecting pin for the internal voltage converter</td></tr>
<tr><td>CAP2+</td><td></td><td>Capacitor2+ connecting pin for the internal voltage converter</td></tr>
<tr><td>CAP2–</td><td></td><td>Capacitor2– connecting pin for the internal voltage converter</td></tr>
<tr><td>VOUT</td><td>I/O</td><td>DC/DC Voltage converter output (7.2 V)</td></tr>
<tr><td>VR</td><td>I</td><td>Voltage adjust pin. This pin gives a voltage between V0 and V_{SS} by resistance-division of voltage.</td></tr>
<tr><td>VEXT</td><td>I</td><td>External reference voltage for internal regulator (instead of the internal V_{REF}, 2V).
REF = “Low(VSS)”: VEXT is not used (open).
REF = “High(VDD)”: VEXT is reference input voltage of the internal voltage regulator.</td></tr>
<tr><td>REF</td><td>I</td><td>Select the reference voltage of internal voltage regulator.
REF = “Low(V_{SS})”: The input voltage of the internal voltage regulator is the internal V_{REF} (2.0 V).
REF = “High(V_{DD})”: The input voltage of the internal voltage regulator is the voltage of VEXT.</td></tr>
</table>

Table 1. Pin Description (Continued)

Name	I/O	Description
System Control		
CK	I	External clock input. It must be fixed to "High" or "Low" when the internal oscillation circuit is used. In the external clock mode, CK is used as the clock input and OS bit should be off.
MI	I	Select the kinds of the MPU to interface. When MI = "High": 68-series MPU interface mode. When MI = "Low": 80-series MPU interface.
IF	I	Interface data length selection pin for parallel data input. When PS = "Low" IF = "Low" or "High": Serial interface mode. When PS = "High" IF = "Low": 4-bit bus mode. IF = "High": 8-bit bus mode .
PS	I	Parallel / Serial selection input. When PS = "High": 4-bit/8-bit bus, When PS = "Low": Serial mode.
DIRS	I	SEG direction selection input. When DIRS = "High", SEG80 → SEG79 → SEG2 → SEG1. When DIRS = "Low" SEG1 → SEG2 → SEG79 → SEG80.
MPU Interface		
RESETB	I	Hardware Reset input. KS0093 is initialized while RESETB is low.
CSB	I	Chip selection input. KS0093 is selected while CSB is low.
RS	I	Register selection input. When RS = "High", Data register. When RS = "Low", Instruction register.
RW_WR	I	In 80-series MPU Interface mode: this pin is connected to $\overline{WR}$ pin of MPU and is an active low write signal. In 68-series MPU Interface mode: this pin is connected to R/$\overline{W}$pin of MPU. When RW_WR = "High", Read mode. When RW_WR = "Low", Write mode.
E_RD	I	In 80-series MPU Interface mode: this pin is connected to $\overline{RD}$ pin of MPU and is an active low read signal. In 68-series MPU Interface mode: this pin is connected to E pin of MPU and enables read or write command according to RW_WR signal.

Table 1. Pin Description (Continued)

Name	I/O	Description
DB0 to DB3, DB4 to DB5, DB6(SCL), DB7(SI)	I/O	When 8-bit interface mode, used as bi-directional data bus pin DB0 to DB7. During 4-bit interface mode, only DB4 to DB7 are used. In this case, DB0 to DB3 pins are not used. When in serial mode, DB6(SCL) is used as serial clock input pin, DB7(SI) is used as serial data input pin.
LCD Driver Output		
COM1 to COM24	O	Common signal output for driving LCD
COMI1, COMI2	O	Common signal output for horizontal icon display. Each signal is the same, but the name is different.
SEG1 to SEG80	O	Segment signal output for driving LCD
TEST		
TEST	I	Test pin. This pin is not used for normal operation. TEST: Open

FUNCTION DESCRIPTION

SYSTEM INTERFACE

KS0093 has two kinds of MPU interface types: bus mode and serial mode.
Serial or bus mode is selected by PS pin. In bus mode, 4-bit bus or 8-bit bus is selected by IF pin, and 68-series MPU or 80-series MPU is selected by MI pin.

Table 2. Various Kinds of MPU Interface According to PS, MI and IF

PS	MI	IF	CSB	RS	RW_WR	E_RD	DB0 to 3	DB4 to 5	DB6	DB7
Bus mode (H)	68-series (H)	8-bit (H)	CSB	RS	R/$\overline{W}$	E	DB0 to 3	DB4 to 5	DB6	DB7
		4-bit (L)	CSB	RS	R/$\overline{W}$	E	* (1)	DB4 to 5	DB6	DB7
	80-series (L)	8-bit (H)	CSB	RS	$\overline{WR}$	$\overline{RD}$	DB0 to 3	DB4 to 5	DB6	DB7
		4-bit (L)	CSB	RS	$\overline{WR}$	$\overline{RD}$	*	DB4 to 5	DB6	DB7
Serial mode (L)	(H)/(L) (2)	(H)/(L)	CSB	RS	(H)/(L)	(H)/(L)	*	*	SCL	SI

NOTES:
1. "*": Dont care. (high, low or open)
2. Fixed high (V_{DD}) or low (V_{SS}).

PS

H	Bus mode
L	Serial bus mode

MI

H	6800-Series MPU interface
L	8080-Series MPU interface

IF

H	8-Bit interface mode
L	4-Bit interface mode

CSB

H	Chip is not selected
L	Chip is selected

RS

H	Data register select
L	Instruction register select

RW_WR

MI=H	6800-series read/write select
MI=L	8080-series "Low" write enable

E_RD

MI=H	6800-series active "High" enable
MI=L	8080-series "Low" read enable

SCL(DB6)

PS=L	Serial clock input

SI(DB7)

PS=L	Serial data input

Interface with MPU in Parallel Bus Mode (PS = "High")

During writing operation, two 8-bit registers, data register (DR) and instruction register (IR) are used. The data register (DR) is used as a temporary data storage place to be written into DDRAM / CGRAM / ICONRAM and one of these RAMs is selected by the RAM address setting instruction. The Instruction register (IR) is used only to store instruction code transferred from MPU. To select DR or IR register, RS input pin is used.

During reading operation, 8-bit register, output data register (OR) is used. The output data register (OR) is used as a temporary data storage place to be read from DDRAM / CGRAM / ICONRAM and one of these RAMS is selected by the RAM address setting instruction. After RAM address setting, the first reading is a dummy cycle in 8-bit bus mode (Figure 3, 4). The valid data comes from the second reading. In 4-bit bus mode, after RAM address setting, the first and the second reading are dummy cycles (Figure 5, 6). The valid data comes from the third reading. The dummy read increases the address counter (AC) increased by 1. So it is recommended to set address again before writing. The instruction read cycle is not supported and it is regarded as a "no operation" cycle.

In 4-bit bus mode, you need to transfer 4-bit data (through DB4 to DB7) two times. The high order bits (for 8-bit mode DB4 to DB7) are transferred before the low order bits (for 8-bit mode DB0 to DB3) are in read and write transaction. The DB0 to DB3 pins are floated in this 4-bit bus mode.
After RESETB resets, KS0093 considers first 4-bit data from MPU as the high order bits.

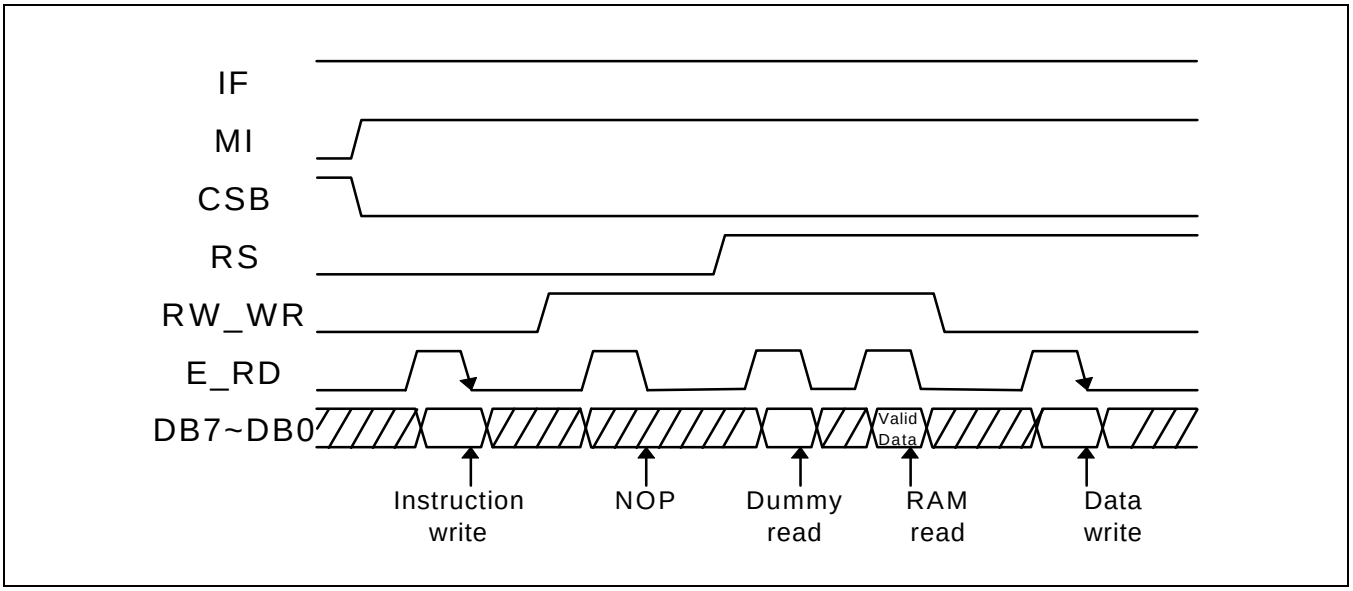


Figure 3. Timing Diagram of 8-bit Parallel Bus Mode Data Transfer (68-series MPU Mode)

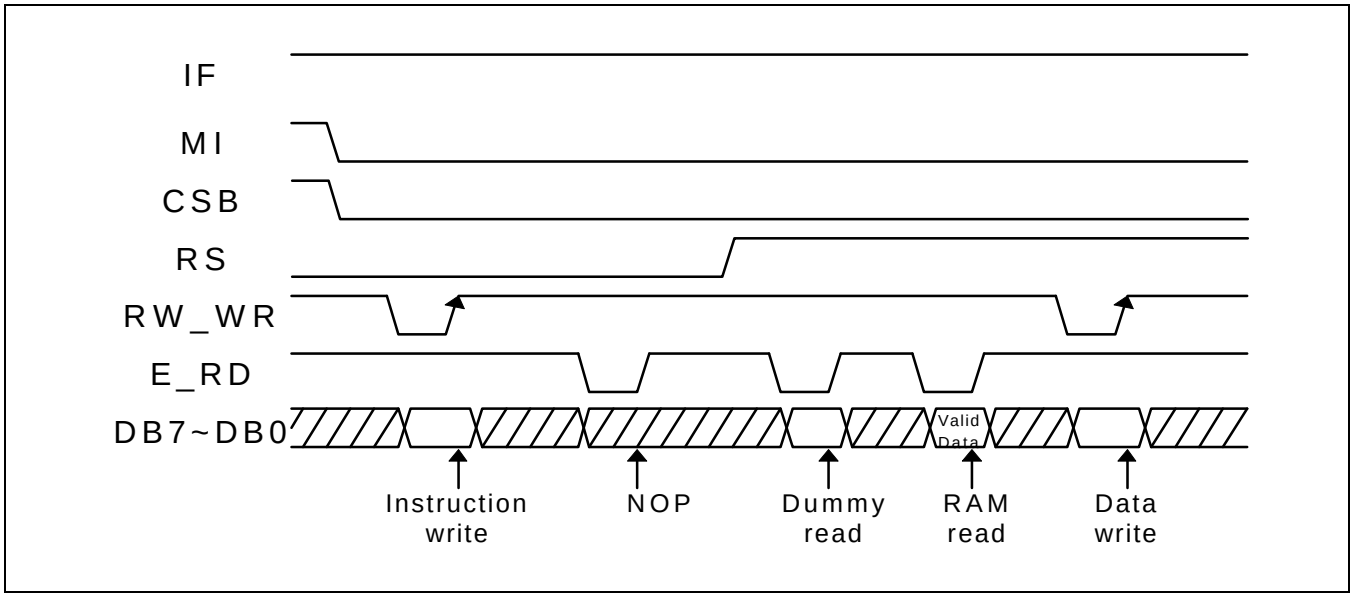


Figure 4. Timing Diagram of 8-bit Parallel Bus Mode Data Transfer (80-series MPU Mode)

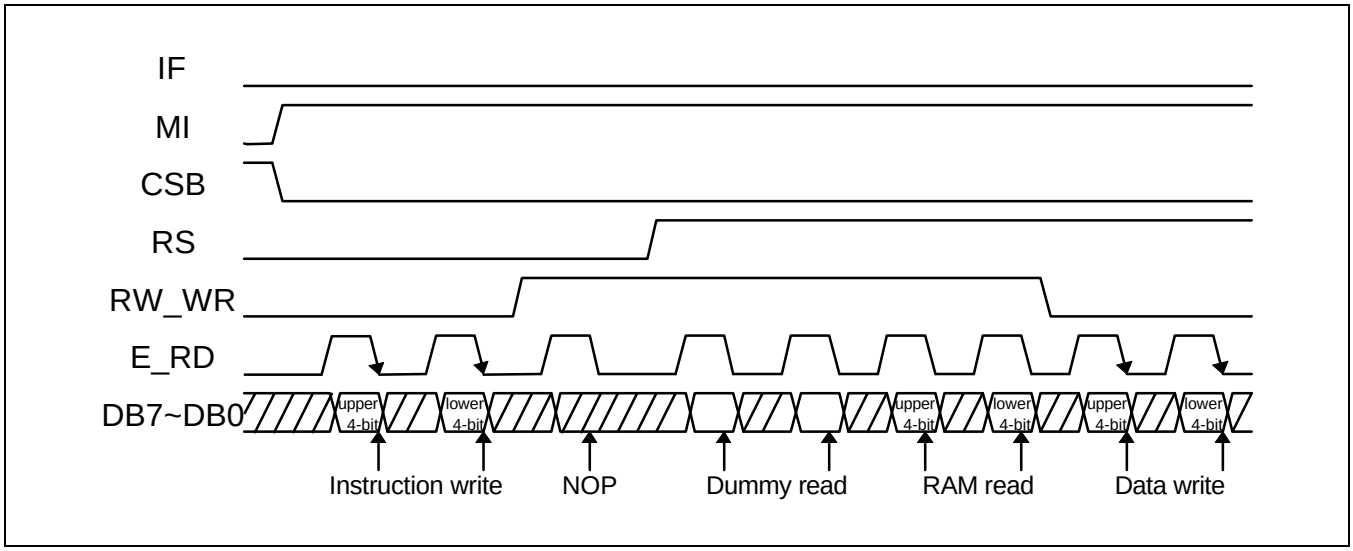


Figure 5. Timing Diagram of 4-bit Parallel Bus Mode Data Transfer (68-series MPU Mode)

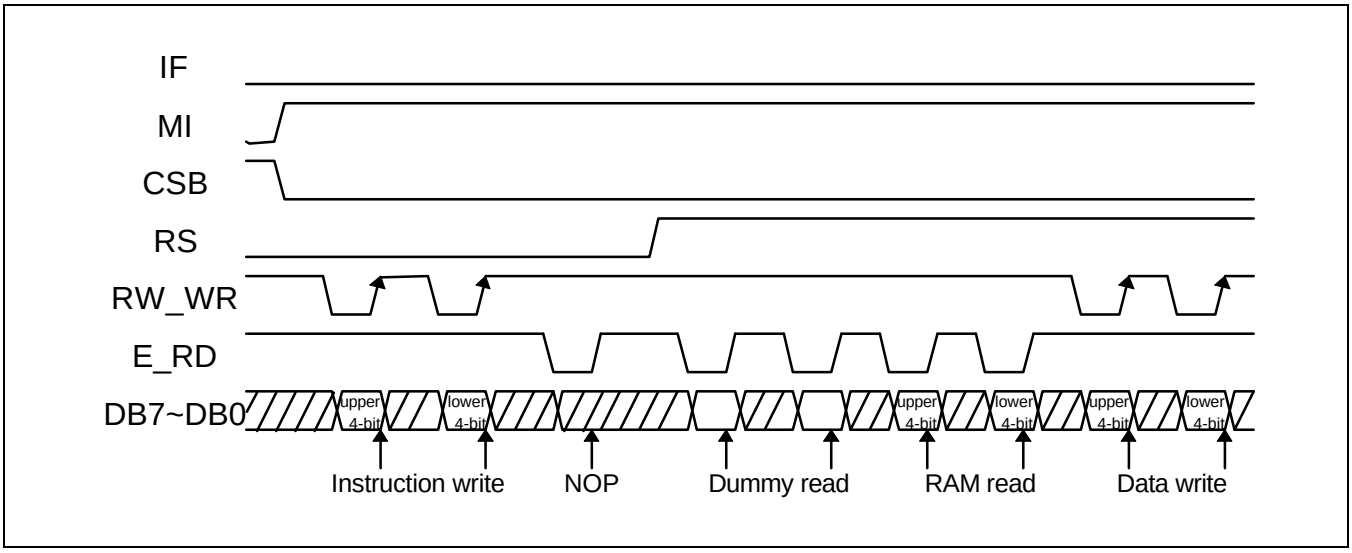


Figure 6. Timing Diagram of 4-bit Parallel Bus Mode Data Transfer (80-series MPU Mode)

Interface With MPU in Serial Bus Mode (PS = "Low")

When PS input pin is "Low", "clock synchronized serial interface mode" is selected.
At this time, four ports, SCL (DB6, synchronizing transfer clock input), SI (DB7, serial data input), and RS (register selection input), CSB (chip selection input) are used.
By setting CSB to "Low", KS0093 can receive SCL input. If CSB is set to "High", KS0093 initialize the interface circuit (8-bit shift register and 3-bit counter).
Serial data is input in the order of "D7, D6, D5, D4, D3, D2, D1, D0" from the serial data input pin (SI = DB7) at the rising edge of serial clock (SCL = DB6).
At the rising edge of the 8th serial clock, the serial data (D7–D0) is converted into 8-bit bus data. The RS input of the DR/IR selection is latched at the rising edge of the 8th serial clock (SCL).

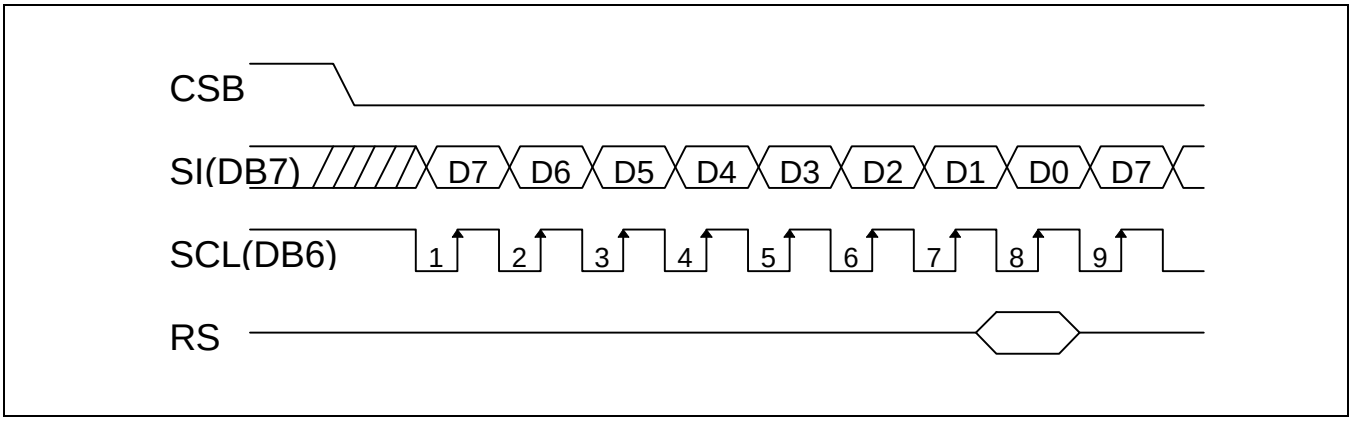


Figure 7. Timing Diagram of Serial Data Transfer

ADDRESS COUNTER (AC)

Address counter (AC) in KS0093 stores the DDRAM / CGRAM / ICONRAM address. After writing into or reading from DDRAM / CGRAM / ICONRAM, AC is automatically increased by 1.

DISPLAY DATA RAM (DDRAM)

DDRAM stores display data of maximum 64×8 bits (Max. 64 characters).
DDRAM address is set in the address counter (AC) as a hexadecimal number.

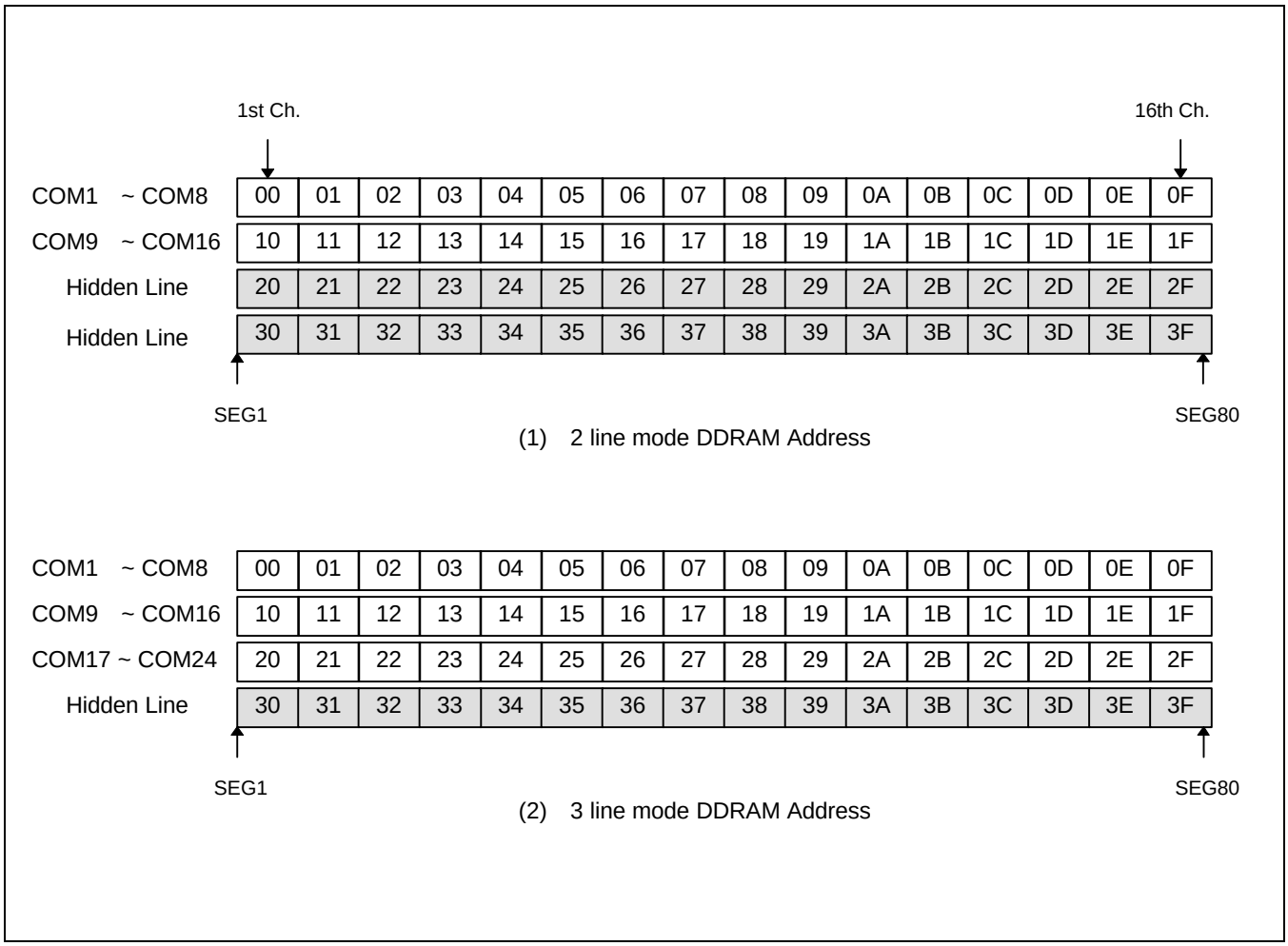


Figure 8. DDRAM Address

CHARACTER GENERATOR ROM (CGROM)

CGROM has 256 5 × 8-dot characters. The CG bit of the instruction table selects 8 characters (00h to 07h) of CGROM or CGRAM.

CGROM Character Code Table is to be determined.

CHARACTER GENERATOR RAM (CGRAM)

CGRAM has up to 5 × 8-dot 8 characters. By writing font data to CGRAM, user defined character can be used.

Table 3. Relationship between Character Code (DDRAM) and Character Pattern (CGRAM)

Character Code (DDRAM Data)								CGRAM Address								CGRAM Data (Character Pattern)								Pattern Number
D7	D6	D5	D4	D3	D2	D1	D0	A7	A6	A5	A4	A3	A2	A1	A0	P7	P6	P5	P4	P3	P2	P1	P0	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	–	–	–	0	1	0	1	0	Pattern 1
			(00h)					0	0	0	0	0	0	0	1	–	–	–	1	0	1	0	1	
								0	0	0	0	0	0	1	0	–	–	–	0	1	0	1	0	
								0	0	0	0	0	0	1	1	–	–	–	1	0	1	0	1	
								0	0	0	0	0	1	0	0	–	–	–	0	1	0	1	0	
								0	0	0	0	0	1	0	1	–	–	–	1	0	1	0	1	
								0	0	0	0	0	1	1	0	–	–	–	0	1	0	1	0	
								0	0	0	0	0	1	1	1	–	–	–	1	0	1	0	1	
0	0	0	0	0	0	0	1	0	0	0	0	1	0	0	0	–	–	–	0	0	0	0	0	Pattern 2
			(01h)					0	0	0	0	1	0	0	1	–	–	–	1	1	1	1	1	
								0	0	0	0	1	0	1	0	–	–	–	0	0	0	0	0	
								0	0	0	0	1	0	1	1	–	–	–	1	1	1	1	1	
								0	0	0	0	1	1	0	0	–	–	–	0	0	0	0	0	
								0	0	0	0	1	1	0	1	–	–	–	1	1	1	1	1	
								0	0	0	0	1	1	1	0	–	–	–	0	0	0	0	0	
								0	0	0	0	1	1	1	1	–	–	–	1	1	1	1	1	
0	0	0	0	0	0	1	0	0	0	0	1	0	0	0	0	–	–	–	0	1	0	1	0	Pattern 3
			(02h)					0	0	0	1	0	0	0	1	–	–	–	0	1	0	1	0	
								0	0	0	1	0	0	1	0	–	–	–	0	1	0	1	0	
								0	0	0	1	0	0	1	1	–	–	–	0	1	0	1	0	
								0	0	0	1	0	1	0	0	–	–	–	0	1	0	1	0	
								0	0	0	1	0	1	0	1	–	–	–	0	1	0	1	0	
								0	0	0	1	0	1	1	0	–	–	–	0	1	0	1	0	
								0	0	0	1	0	1	1	1	–	–	–	0	1	0	1	0	
0	0	0	0	0	0	1	1	0	0	0	1	1	0	0	0	–	–	–	0	1	1	1	0	Pattern 4
			(03h)					0	0	0	1	1	0	0	1	–	–	–	1	0	1	0	1	
								0	0	0	1	1	0	1	0	–	–	–	1	1	0	1	1	
								0	0	0	1	1	0	1	1	–	–	–	1	0	1	0	1	
								0	0	0	1	1	1	0	0	–	–	–	0	1	1	1	0	
								0	0	0	1	1	1	0	1	–	–	–	1	1	1	1	1	
								0	0	0	1	1	1	1	0	–	–	–	1	1	1	1	1	
								0	0	0	1	1	1	1	1	–	–	–	1	1	1	1	1	

Table 3. Relationship between Character Code (DDRAM) and Character Pattern (CGRAM) (Continued)

Character Code (DDRAM Data)								CGRAM Address								CGRAM Data (Character Pattern)								Pattern Number
D7	D6	D5	D4	D3	D2	D1	D0	A7	A6	A5	A4	A3	A2	A1	A0	P7	P6	P5	P4	P3	P2	P1	P0	
0	0	0	0	0	1	0	0	0	0	1	0	0	0	0	0	–	–	–	1	1	0	1	1	Pattern 5
			(04h)					0	0	1	0	0	0	0	1	–	–	–	1	0	0	0	1	
								0	0	1	0	0	0	1	0	–	–	–	0	0	0	0	0	
								0	0	1	0	0	0	1	1	–	–	–	1	0	0	0	1	
								0	0	1	0	0	1	0	0	–	–	–	1	1	0	1	1	
								0	0	1	0	0	1	0	1	–	–	–	1	1	1	1	1	
								0	0	1	0	0	1	1	0	–	–	–	1	1	1	1	1	
								0	0	1	0	0	1	1	1	–	–	–	1	1	1	1	1	
0	0	0	0	0	1	0	1	0	0	1	0	1	0	0	0	–	–	–	1	1	1	1	1	Pattern 6
			(05h)					0	0	1	0	1	0	0	1	–	–	–	1	1	1	1	1	
								0	0	1	0	1	0	1	0	–	–	–	0	0	0	0	0	
								0	0	1	0	1	0	1	1	–	–	–	0	0	0	0	0	
								0	0	1	0	1	1	0	0	–	–	–	1	1	1	1	1	
								0	0	1	0	1	1	0	1	–	–	–	1	1	1	1	1	
								0	0	1	0	1	1	1	0	–	–	–	0	0	0	0	0	
								0	0	1	0	1	1	1	1	–	–	–	0	0	0	0	0	
0	0	0	0	0	1	1	0	0	0	1	1	0	0	0	0	–	–	–	0	0	1	1	0	Pattern 7
			(06h)					0	0	1	1	0	0	0	1	–	–	–	0	0	1	1	0	
								0	0	1	1	0	0	1	0	–	–	–	0	0	1	1	0	
								0	0	1	1	0	0	1	1	–	–	–	0	0	1	1	0	
								0	0	1	1	0	1	0	0	–	–	–	0	0	1	1	0	
								0	0	1	1	0	1	0	1	–	–	–	0	0	1	1	0	
								0	0	1	1	0	1	1	0	–	–	–	0	0	1	1	0	
								0	0	1	1	0	1	1	1	–	–	–	0	0	1	1	0	
0	0	0	0	0	1	1	1	0	0	1	1	1	0	0	0	–	–	–	0	0	0	0	0	Pattern 8
			(07h)					0	0	1	1	1	0	0	1	–	–	–	1	0	0	0	1	
								0	0	1	1	1	0	1	0	–	–	–	1	1	0	1	1	
								0	0	1	1	1	0	1	1	–	–	–	1	0	0	0	1	
								0	0	1	1	1	1	0	0	–	–	–	0	0	0	0	0	
								0	0	1	1	1	1	0	1	–	–	–	1	0	0	0	1	
								0	0	1	1	1	1	1	0	–	–	–	1	1	0	1	1	
								0	0	1	1	1	1	1	1	–	–	–	1	1	1	1	1	

NOTE: "–": Dont care

SEGMENT & COMMON ICON RAM (ICONRAM)

ICONRAM has segment control data and segment pattern data. COMI1 and COMI2 are the same signal but the name is different. So the icons on the same SEG are displayed at the same time. The number of icons is 80.

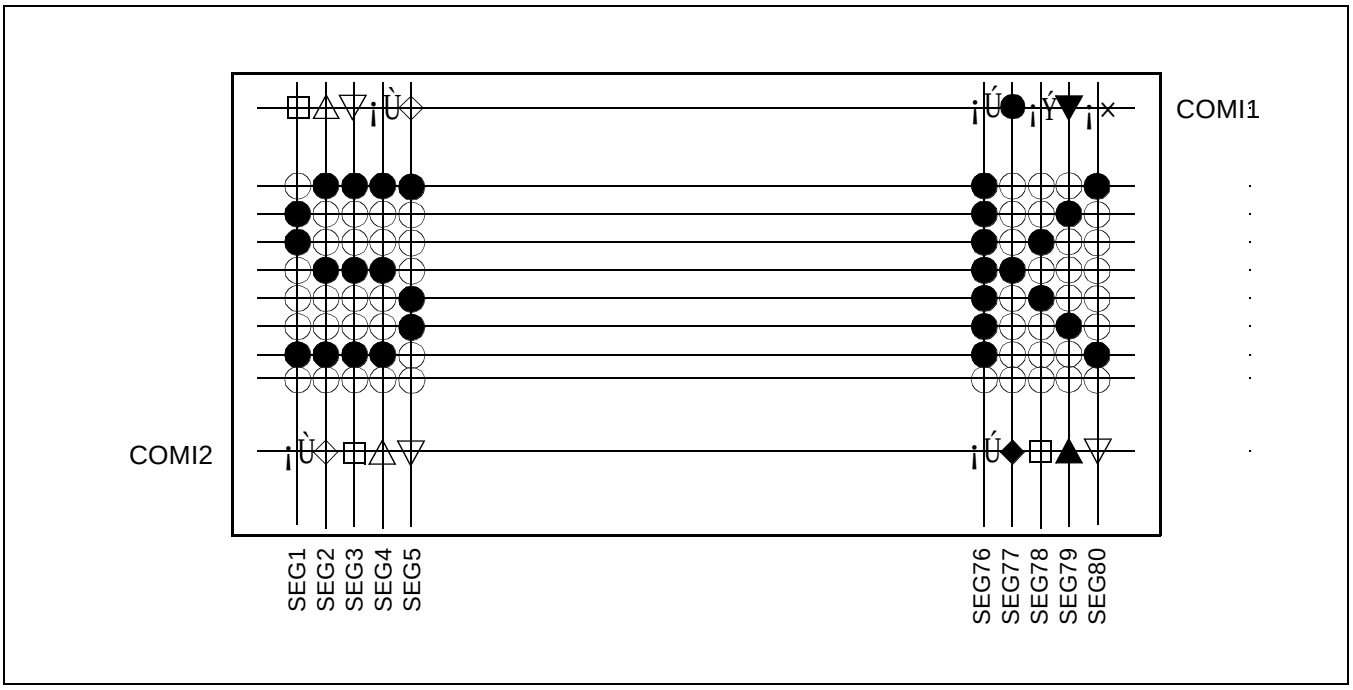


Figure 9. Relationship Between ICONRAM and Icon Display

.

Table 4. Relationship Between ICONRAM Address and Display Pattern

ICONRAM Address	ICONRAM Bits							
	D7	D6	D5	D4	D3	D2	D1	D0
00h	–	–	–	S1	S2	S3	S4	S5
01h	–	–	–	S6	S7	S8	S9	S10
02h	–	–	–	S11	S12	S13	S14	S15
. .	. .	. .	. .	. .	. .	. .	. .	. .
0Dh	–	–	–	S66	S67	S68	S69	S70
0Eh	–	–	–	S71	S72	S73	S74	S75
0Fh	–	–	–	S76	S77	S78	S79	S80

NOTE: "–": dont care

LOW POWER CONSUMPTION MODE

KS0093 has a sleep mode for reducing power consumption during standby period.

Sleep mode (Power save bit on, oscillation bit off)
To enter the sleep mode, the power circuit and oscillation circuit should be turned off by using the power save command and the power control command. This mode helps save power by reducing current to reset level.

- Liquid crystal display output
  - — COM1 to COM24, COMI1, COMI2: V_{SS} level
  - — SEG1 to SEG80: V_{SS} level
- Data written in DDRAM, CGRAM, ICONRAM and registers remain at previous value.
- Operation mode is retained as it was prior to the execution of the sleep mode. All internal circuits are stopped.
- Power circuit and oscillation circuit
  - — The built-in supply circuit and oscillation circuit are turned off by power save command and power control command.

LCD DRIVING CIRCUIT

LCD driver circuit has 26 common and 80 segment signals for driving LCD. Data from ICONRAM/CGRAM / CGROM are transferred to 80-bit segment register serially, and then stored to 80-bit shift latch. In case of 2-line display mode, COM1 to COM16, COMI1 and COMI2 have 1/17 duty, and in 3-line mode, COM1 to COM24, COMI1 and COMI2 have 1/25 duty ratio. SEG bi-directional function is selected by DIRS input pin, and COM shift direction is selected by function set instruction "S" bit.

Table 5. SEG Data Shift Direction

DIRS	SEG Data Shift Direction
Low	SEG1, SEG2 ,SEG3 → SEG78, SEG79, SEG80
High	SEG80, SEG79, SEG78 → SEG3, SEG2, SEG1

Table 6. COM Data Shift Direction

Duty	S	COM Data Shift Direction
2-Line mode	Low (Left)	COM1 → COM2 . . . . . COM15, → COM16 → COMI1 (COMI2)
	High (Right)	COMI1 (COMI2) → COM16 → COMI15 . . . . . COM2 → COM1
3-Line mode	Low (Left)	COM1 → COM2 . . . . . COM23, COM24 → COMI1 (COMI2)
	High (Right)	COMI1 (COMI2) → COM24 → COM23 . . . . . COM2 → COM1

INSTRUCTION DESCRIPTION

Table 7. Instructction Table

Instruction	Instructction Code									Description
	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
Return home	0	0	0	0	0	0	0	1	–	DDRAM address to "00h" from AC and the cursor retruns to 00h position. The contents of DDRAM are not changed.
Double height mode	0	0	0	0	0	1	0	DH2	DH1	Doubled height mode DH2, DH1: 00: normal display (default) 01: COM1 to COM16 is a double height, COM17 to COM24 is normal 10: 1) 2-line mode: normal display 2) 3-line mode: COM1 to COM8 is normal, COM9 to COM24 is a double height 11: normal display
Power save	0	0	0	0	0	1	1	OS	PS	Power save/oscillation circuit on/off OS=0: oscillator off (default) 1: oscillator on PS=0: power save off (default) 1: power save on
Function set	0	0	0	0	1	0	N	S	CG	Display line mode. N=0:2-line display mode (default) 1:3-line display mode Shifting direction of COM. S=0: 2-line mode: COM1 → COM16 (default) 3-line mode: COM1 → COM24 (default) 1: 2-line mode: COM16 → COM1 3-line mode: COM24 → COM1 Select CGRAM or CGROM CG=0: CGROM (default) 1: CGRAM
Line shift mode	0	0	0	0	1	1	0	LS2	LS1	Determination of the DDRAM line which is displayed at the first line at LCD LS2, LS1= 00: DDRAM line 1 shows at the first line of LCD (default). 01: DDRAM line 2 shows at the first line of LCD. 10: DDRAM line 3 shows at the first line of LCD. 11: DDRAM line 4 shows at the first line of LCD
Bias control	0	0	0	0	1	1	1	–	BS	Determination of bias BS=0: 1/5 bias (default) 1: 1/4 bias
Power control	0	0	0	1	0	0	VC	VR	VF	LCD power control. VC=0: Voltage converter off (default) 1: Voltage converter on VR=0: Voltage regulator off (default) 1: Voltage regulator on VF=0: Voltage follower off (default) 1: Voltage follower on

Table 7. Instructction Table (Continued)

Instruction	Instructction Code									Description
	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
Display control	0	0	0	1	0	1	C	B	D	Cursor/blink/display on/off C=0: cursor off (default), 1: cursor on B=0: blink off (default), 1: blink on D=0: display off (default), 1: display on
DD/CGRAM address set	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	DDRAM/CGRAM address. Range: DDRAM 00h to 3Fh CGRAM 40h to 7Fh
ICONRAM address set	0	0	1	0	IA4	IA3	IA2	IA1	IA0	ICONRAM address, electronic volume and test byte address Range: ICONRAM 00h to 0Fh EV 10h(Electronic volume byte), TE 11h (Test byte)
Write data	1	D7	D6	D5	D4	D3	D2	D1	D0	Write DDRAM /CGRAM/ICONRAM
Read data	1	D7	D6	D5	D4	D3	D2	D1	D0	Read DDRAM/CGRAM/ICONRAM or registers data [(3)].
NOP	0	0	0	0	0	0	0	0	0	Non-operation Instruction
Test	0	0	0	1	1	*	*	*	*	Dont use this Instruction

NOTE:

1. "–": Dont care
2. "*": Dont use
3. Instruction execution time depends on the internal process time of KS0093, therefore it is necessary to provide a time larger than one MPU interface cycle time (tc) between execution of two successive instructions.

RETURN HOME

RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**–**

Retrun home instruction field makes the cursor return home.
DDRAM address is set to '00h" from AC and the cursor returns to '00h" position. The contents of DDRAM are not changed.

DOUBLE HEIGHT MODE

RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**0**	**0**	**0**	**0**	**1**	**0**	**DH2**	**DH1**

Double height mode instruction field selects the double height line type.

DH2	**DH1**		
0	0	Normal display line mode. (default)	
0	1	COM1 to COM16 is a double height, COM17 to COM24 is normal	
1	0	2-Line mode	Normal display
		3-Line mode	COM1 to COM8 is normal, COM9 to COM24 is a double height
1	1	Normal display	

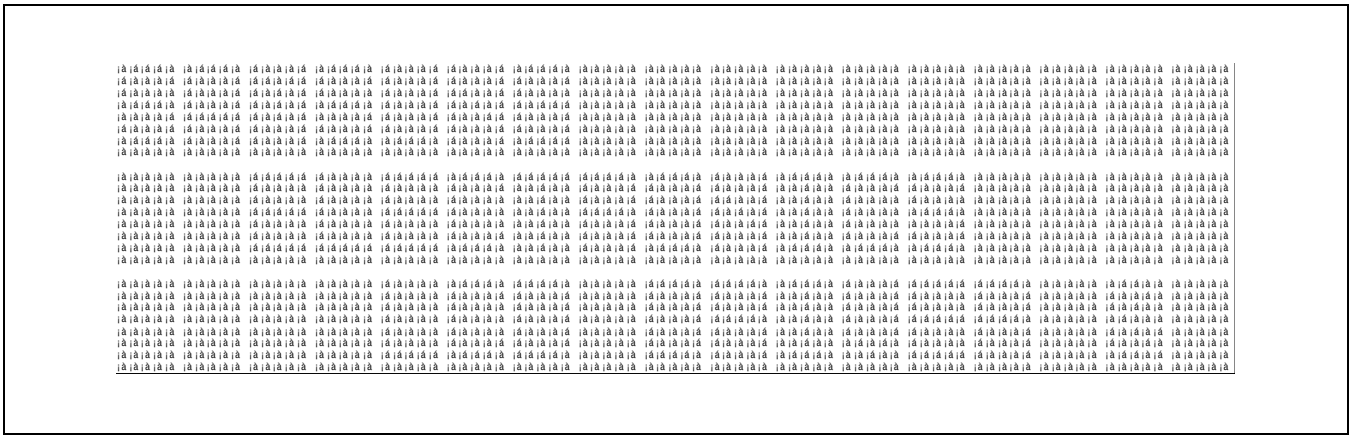


Figure 10. 3 Line Normal Mode Display (DH2, DH1 = 00)

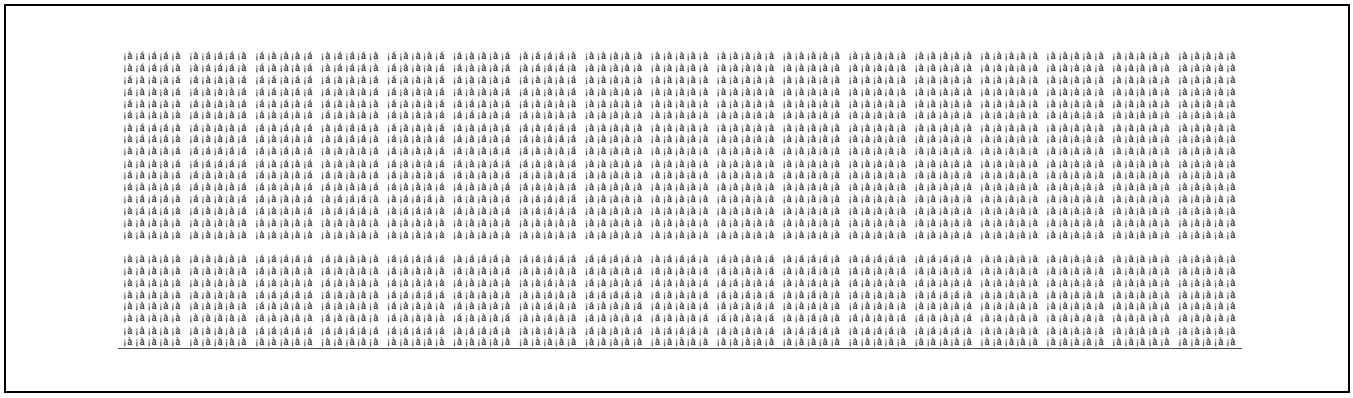


Figure 11. COM1 to COM16 is a Double Height Line, COM17 to COM24 is Normal (DH2, DH1 = 01)

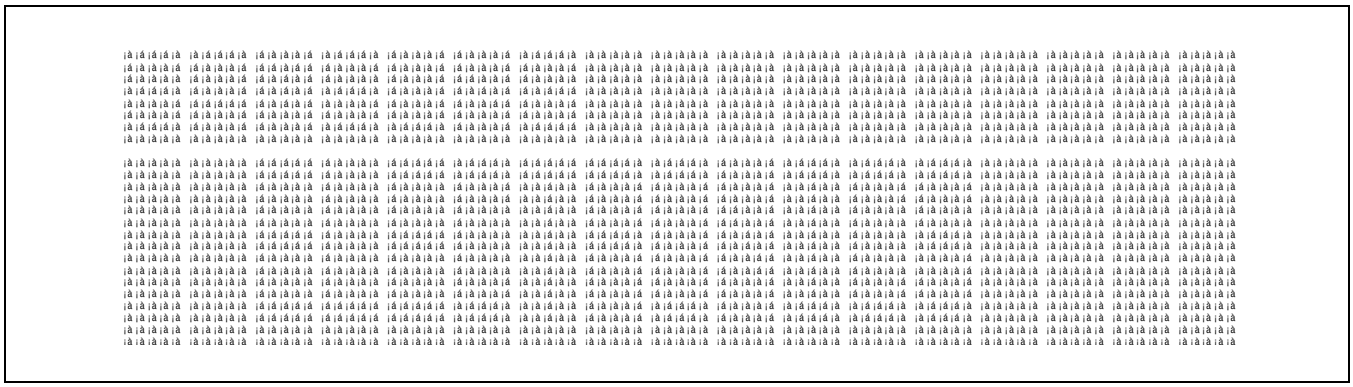


Figure 12. COM1 to 8 is Normal, COM9 to COM24 is a Double Height Line (DH2, DH1 = 10)

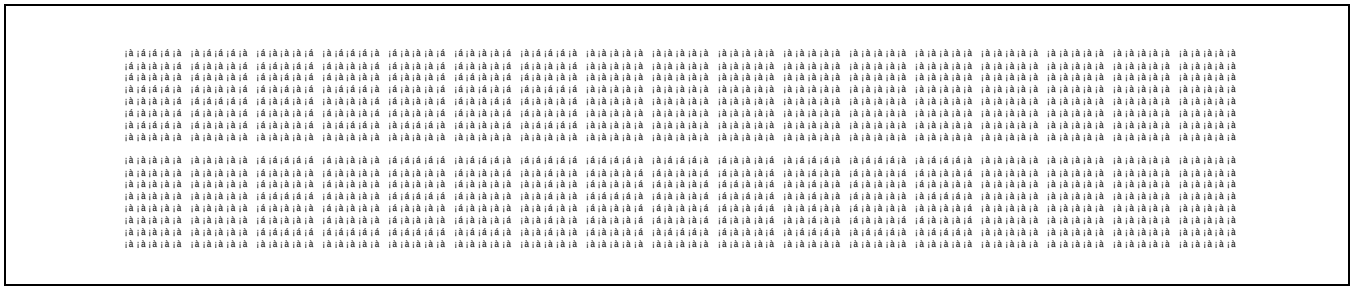


Figure 13. 2-Line Normal Mode Display (DH2, DH1 = 00)

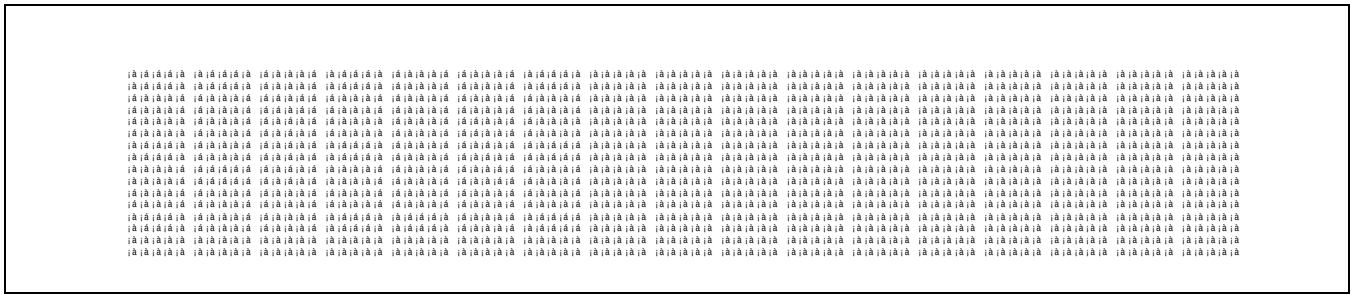


Figure 14. COM1 to COM16 is a Double Height Line (DH2, DH1 = 01)

POWER SAVE SET

RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**0**	**0**	**0**	**0**	**1**	**1**	**OS**	**PS**

Power save instruction field is used to control the oscillator and set or reset the power save mode.

OS	**Oscillator on / off control bit**
H	Oscillator is turned on
L	Oscillator is turned off. (default)

PS	**Power save on / off control bit**
H	Power save mode is turned on
L	Power save mode is turned off. (default)

FUNCTION SET

RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**0**	**0**	**0**	**1**	**0**	**N**	**S**	**CG**

N	**Display line mode instruction field selects 2-line or 3-line display mode**
H	3-Line display mode
L	2-Line display mode. (default)

S	**Data shift direction of common**
H	COM right shift
L	COM left shift (default)

NOTE: Refer to table 6.

CG	**CGRAM Enable bit**
H	CGRAM can be accessed and you can use this RAM for eight special character area. (00h – 07h = CGRAM font display)
L	CGRAM is disabled. CGROM (00h to 07h) can be accessed and the additional current consumption is saved by using this mode. (default) (00h – 07h = CGROM font display)

LINE SHIFT MODE

RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**0**	**0**	**0**	**1**	**1**	**0**	**LS2**	**LS1**

LS2, LS1 **Line shift mode instruction field selects the DD RAM to be displayed in first line.**

0	0	DDRAM line 1 shows at the first line of LCD. (default)
0	1	DDRAM line 2 shows at the first line of LCD
1	0	DDRAM line 3 shows at the first line of LCD
1	1	DDRAM line 4 shows at the first line of LCD

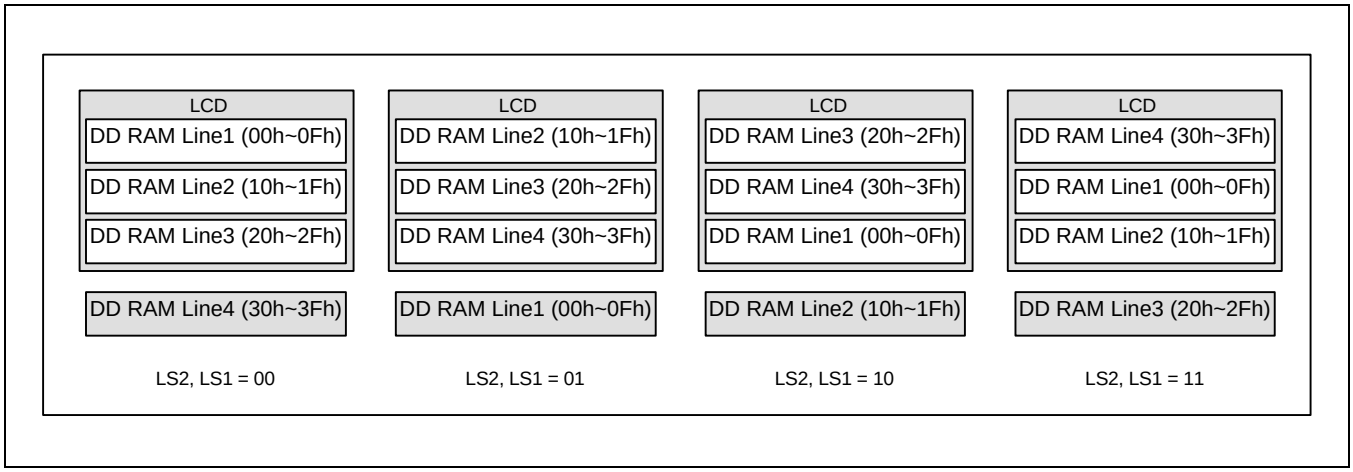


Figure 15. Line Shift Mode Display at 3-Line LCD

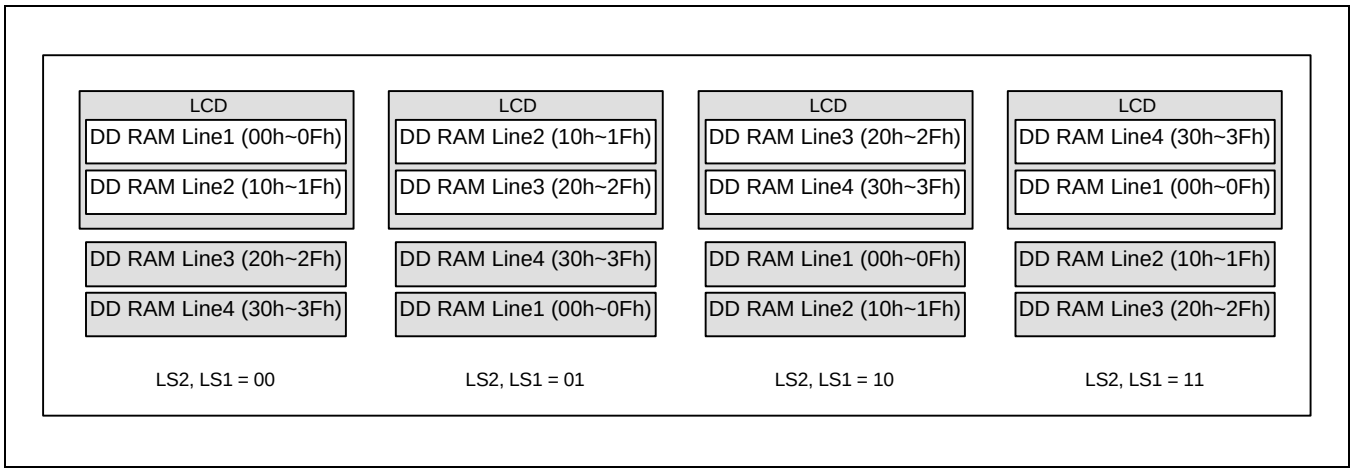


Figure 16. Line Shift Mode Display at 2-Line LCD

BIAS CONTROL

RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**0**	**0**	**0**	**1**	**1**	**1**	**–**	**BS**

Bias control instruction field sets LCD bias voltages generated internally. This bits is used when the internal voltage follower is on.

BS	
0	1/5 Bias (default).
0	1/4 Bias (V2 = V3)

POWER CONTROL SET

RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**0**	**0**	**1**	**0**	**0**	**VC**	**VR**	**VF**

Power control instruction filed sets voltage converter / regulator / follower on / off.

VC	**Voltage converter circuit control bit**
H	Voltage converter is turned on
L	Voltage regulator converter is turned off. (default)

VR	**Voltage regulator circuit control bit**
H	Voltage regulator is turned on
L	Voltage regulator is turned off. (default)

VF	**Voltage follower circuit control bit**
H	Voltage follower is turned on
L	Voltage follower is turned off. (default)

NOTE: The oscillation circuit must be turned on for the voltage converter circuit to be active.

DISPLAY CONTROL

RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**0**	**0**	**1**	**0**	**1**	**C**	**B**	**D**

Display control instruction field controls cursor / blink / display on / off.

C	**Cursor on / off control bit**
H	Cursor is turned on
L	Cursor is disappeared in current display. (default)

B	**Cursor blink on / off control bit**
H	When C="High", KS0093 makes LCD alternate between inverting display character and normal display character at the cursor position with about a half second. On the contrary, if C="Low", only a normal character is displayed regardless of "B" flag.
L	Blink is off. (default)

D	**Display on / off control bit**
H	Entire display is turned on
L	Display is turned off, but display data are remained in DDRAM. (default)

DD/CG RAM ADDRESS SET

RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**1**	**AC6**	**AC5**	**AC4**	**AC3**	**AC2**	**AC1**	**AC0**

DD / CG RAM address set instruction field sets DDRAM / CGRAM address.
Before writing / reading data into/from the RAM, set the address by RAM address set instruction. Next, when data are written / read in succession, the address is automatically increased by 1. After accessing 7Fh, the address of AC is 00h.
The address ranges are 00h to 7Fh.

Table 8. DD/CG RAM Address Mapping

Addres	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**A**	**B**	**C**	**D**	**E**	**F**
00h	DDRAM line 1 (00h to 0Fh)															
10h	DDRAM line 2 (10h to 1Fh)															
20h	DDRAM line 3 (20h to 2Fh)															
30h	DDRAM line 4 (30h to 3Fh)															
40h	CGRAM (pattern 0)								CGRAM (pattern 1)							
50h	CGRAM (pattern 2)								CGRAM (pattern 3)							
60h	CGRAM (pattern 4)								CGRAM (pattern 5)							
70h	CGRAM (pattern 6)								CGRAM (pattern 7)							

ICONRAM ADDRESS SET

RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**0**	**1**	**0**	**IA4**	**IA3**	**IA2**	**IA1**	**IA0**

ICONRAM address set instruction field sets ICONRAM / Registers address.
Before writing / reading data into/from the ICON RAM, set the address by ICONRAM address set instruction. Next, when data are written / read in succession, the address is automatically increased by 1. For accessing DD/CGRAM, the DD / CGRAM address set instruction should be set beforehand. After accessing 0Fh, the address of ICONRAM address is 00h. The ICONRAM address ranges are 00h to 1Fh.

Table 9. ICONRAM Address Mapping

Address	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**A**	**B**	**C**	**D**	**E**	**F**
00h	ICON RAM (00h to 0Fh)															
10h	EV	TE	Reserved													

When the EV and TE registers are written, the address counter (AC) is not increased.

EV	Electronic volume register (10h) – default (00000)
TE	Test register (Do not use). (11h)

WRITE DATA

RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**

This instruction field makes KS0093 write binary 8-bit data to DDRAM / CGRAM / ICONRAM or register. The RAM address to be written into is determined by previous DD / CGRAM Address Set or ICONRAM Address Set instruction. After writing operation, the address is automatically increased by 1.

READ DATA

RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**

DDRAM / CGRAM / ICONRAM data read instruction.
Each RAM is selected by address set instruction. And then you can read the RAM data. You can get correct RAM data from second read transaction. The first read data after setting RAM address is dummy data, so the correct RAM data come from the second read transaction. After reading operation, the address is increased by 1 automatically.

INITIALIZING & POWER SAVE MODE SETUP

HARDWARE RESET

After reset by RESETB pin="Low", KS0093 can be initialized the following state.

1. Control Display on/off instruction
C=0: Cursor off
B=0: Blink off
D=0: Display off

2. Power Save Set instruction
OS=0: Oscillator off
PS=0: Power save off

3. Power Control Set instruction
VR=0: Voltage regulator off
VF=0: Voltage follower off
VC=0: Voltage converter off

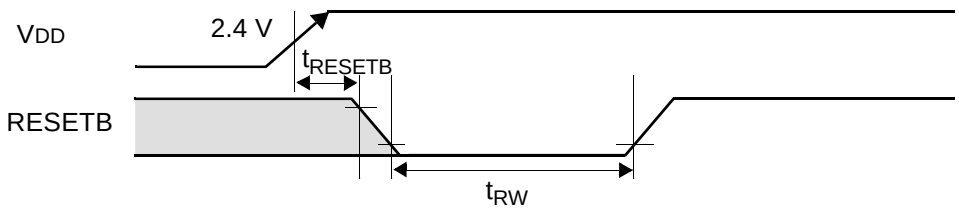
4. Function Set instruction
N=0: 2 line display mode
S=0: COM left shift
CG=0: CGRAM is not used

5. Return Home
Address counter = 00h

6. Electronic contrast control register
Electronic contrast control register: 10h = (0, 0, 0, 0, 0)

In case of 4-bit interface mode selection KS0093 considers the first 4-bit data from MPU as the high order bits.

NOTE: If initialization is not done by the RESETB pin at application, an unknown condition may result. Then you can initialize by instruction.

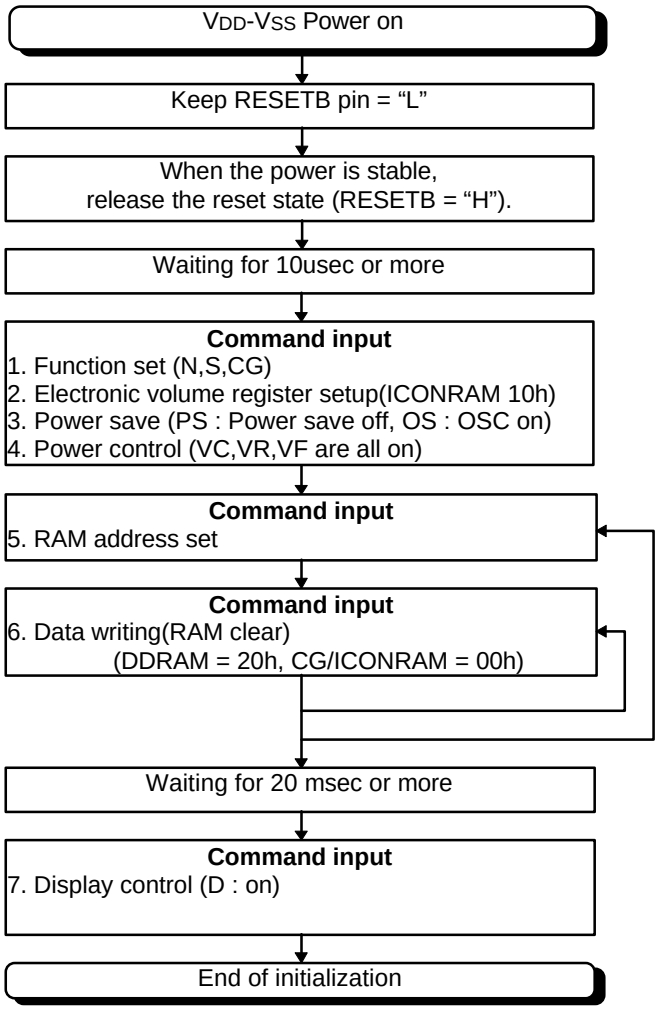


Reset pulse width	t_{RW}	10 µs
Reset start time	t_{RESETB}	50 ns

Figure 17. RESET Timing

INITIALIZING AND POWER SAVE SETUP

Initializing by Instruction



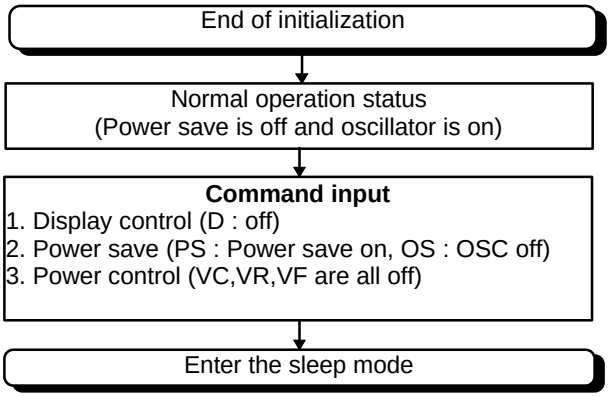
NOTE:
At command 5 and 6, the internal RAM should be cleared.
To clear DDRAM, set address at 00h (first DDRAM) and then write 20h (space character code) 64 times.

To clear CGRAM, Set address at 40h(first CGRAM) and then write 00h (null data) 64 times.

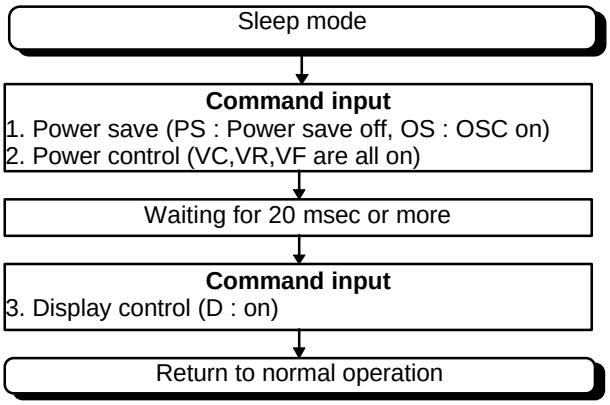
To clear ICONRAM, set ICONRAM address at 00h(first ICONRAM) and then write 00h (null data) 16 times

Sleep Mode Set or Release by Instruction

(a) Sleep mode setting



(b) Sleep mode release



LCD DRIVING POWER SUPPLY CIRCUIT

The power supply circuit produces LCD panel driving voltage at low power consumption. The LCD driving power supply circuit consists of voltage converter, voltage regulator, and voltage follower. It is controlled by power control instruction. Table 11. shows how the LCD driving power supply circuit works by power control instruction sets.

Table 10. Power Supply Control Mode Set

VC	VR	VF	Voltage Converter	Voltage Regulator	Voltage Follower	VOUT Pin	VR Pin	V0, V1, V2, V3, V4 Pin
1	1	1	Enable	Enable	Enable	Internal voltage output	Used for voltage adjustment	Internal voltage output
0	1	1	Disable	Enable	Enable	External voltage input	Used for voltage adjustment	Internal voltage output
0	0	1	Disable	Disable	Enable	Open	Open	V1 to V4: Internal voltage output V0: External voltage input
0	0	0	Disable	Disable	Disable	Open	Open	V0 to V4: External voltage input

NOTE: Any other case which is not written in this table is prohibited.

VOLTAGE CONVERTER

The voltage converter circuit generates positive 4 times voltage of 1.8V that is generated internally. VOUT is generated from the voltage converter. And this conversion voltage is used in the built-in voltage regulator circuit. This application circuit is same as 3-times DC / DC converter.

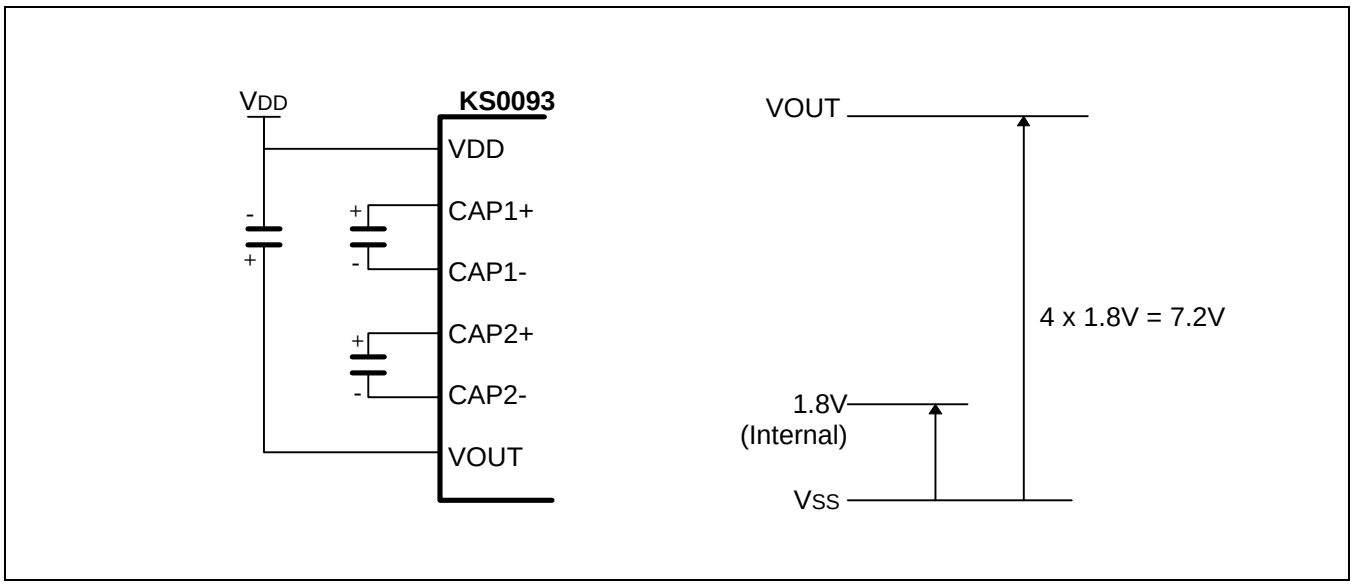


Figure 18. DC/DC Converter Circuit and Output

VOLTAGE REGULATOR

The voltage regulator circuit is used to obtain an appropriate LCD panel driving voltage. This voltage is obtained by adjusting resistors Ra and Rb as shown in equation (1) or (2), and by setting electronic contrast control data bits, see equation (3) or (4).
The potential of V0 pin can be adjusted within VOUT – V_{REF}. V_{REF} is the internal constant voltage source of the chip and this value is 2.0V in the condition $V_{DD} \geq 2.4V$.
The REF selects which voltage is used for voltage regulator between the external VEXT and the internal V_{REF} .

- Voltage regulation by adjusting resistors Ra, Rb

When REF is "Low"

$$V0 = \left(1 + \frac{Rb}{Ra}\right) \times V_{REF} \quad \ldots\ldots\ldots\ldots (1)$$

When REF is "High"

$$V0 = \left(1 + \frac{Rb}{Ra}\right) \times VEXT \quad \ldots\ldots\ldots\ldots (2)$$

The internal V_{REF} of voltage regulator has the temperature compensation function, and the temperature coefficient is TBD.

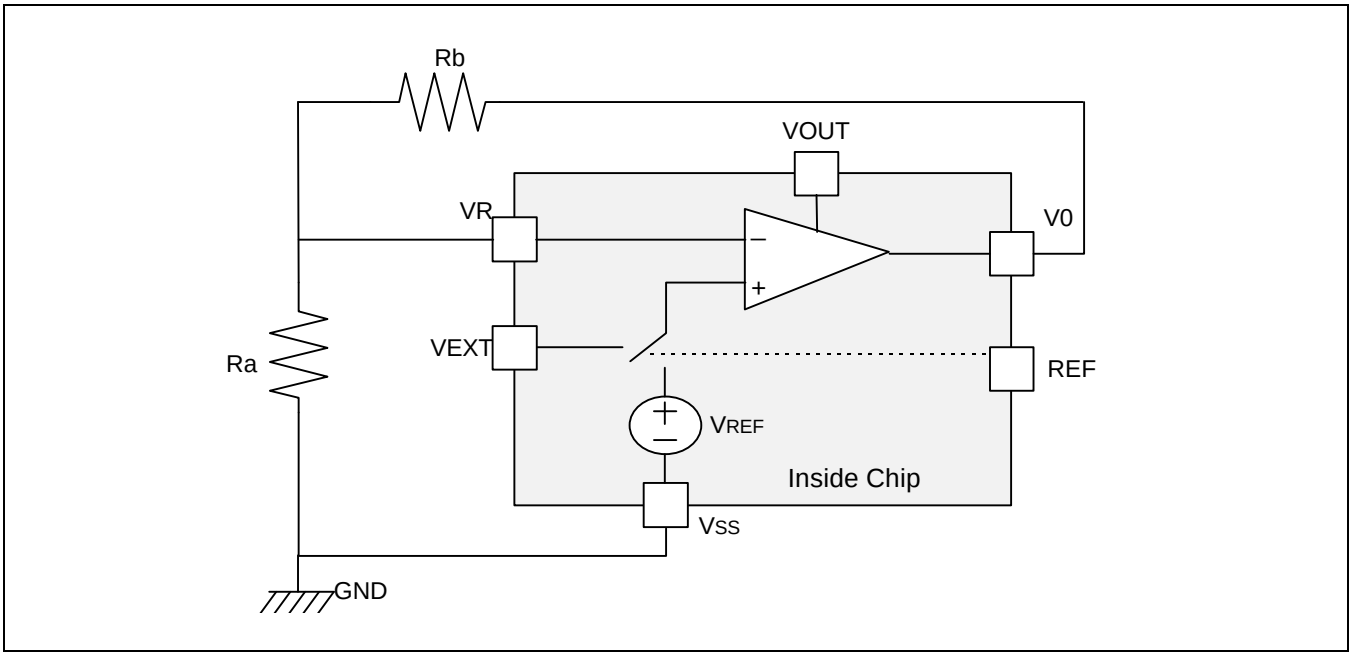


Figure 19. Voltage Regulator Circuit

ELECTRONIC CONTRAST CONTROL (32 STEPS)

Electronic contrast control data bits is 10h = (d4, d3, d2, d1, d0). Voltage regulation is adjusted as 32-contrast step according to the value of electronic contrast control data bits. LCD drive voltage V0 has one of 32 voltage values if 5-bit data is set to the electronic contrast control register (ICONRAM address 10h). When using the electronic contrast control function, you need to turn the voltage regulators on using the power control instruction.

When REF is "Low"

$$V0 = \left(1 + \frac{Rb}{Ra}\right) \times V_{EV} \quad \text{.....(3)}$$

$$V_{EV} = V_{REF} - n\alpha \qquad (n = 0, 1, 2, \text{..... } 30, 31)$$

$$\alpha = V_{REF} / 150$$

When REF is "High"

$$V0 = \left(1 + \frac{Rb}{Ra}\right) \times V_{EV} \quad \text{.....(4)}$$

$$V_{EV} = VEXT - n\alpha \qquad (n = 0, 1, 2, \text{..... } 30, 31)$$

$$\alpha = VEXT / 150$$

Table 11. Electronic Contrast Control Register

No.	d7	d6	d5	d4	d3	d2	d1	d0	nα	V0	Contrast
1	–	–	–	0	0	0	0	0	0α (default)	Maximum	High
2	–	–	–	0	0	0	0	1	1α	:	:
3	–	–	–	0	0	0	1	0	2α	:	:
4	–	–	–	0	0	0	1	1	3α	:	:
:	:	:	:	:	:	:	:	:	:	:	:
31	–	–	–	1	1	1	1	0	(n-1) α	:	:
32	–	–	–	1	1	1	1	1	nα	Maximum	Low

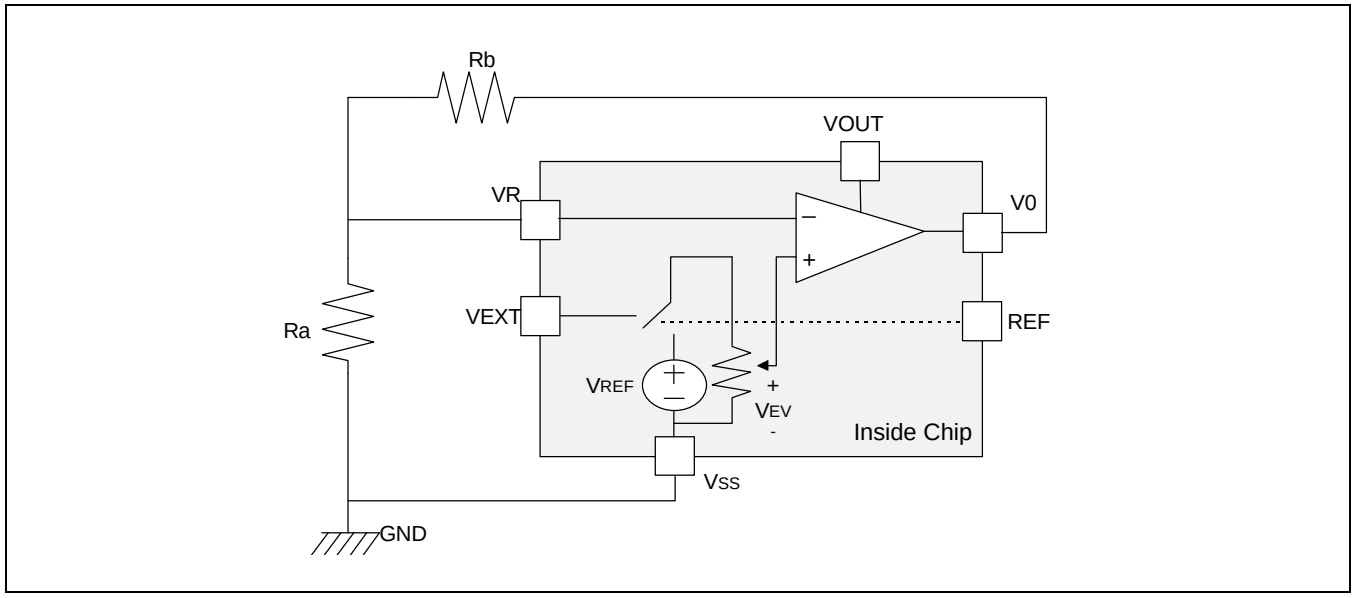


Figure 20. Electronic Contrast Control Circuit

VOLTAGE GENERATOR CIRCUIT

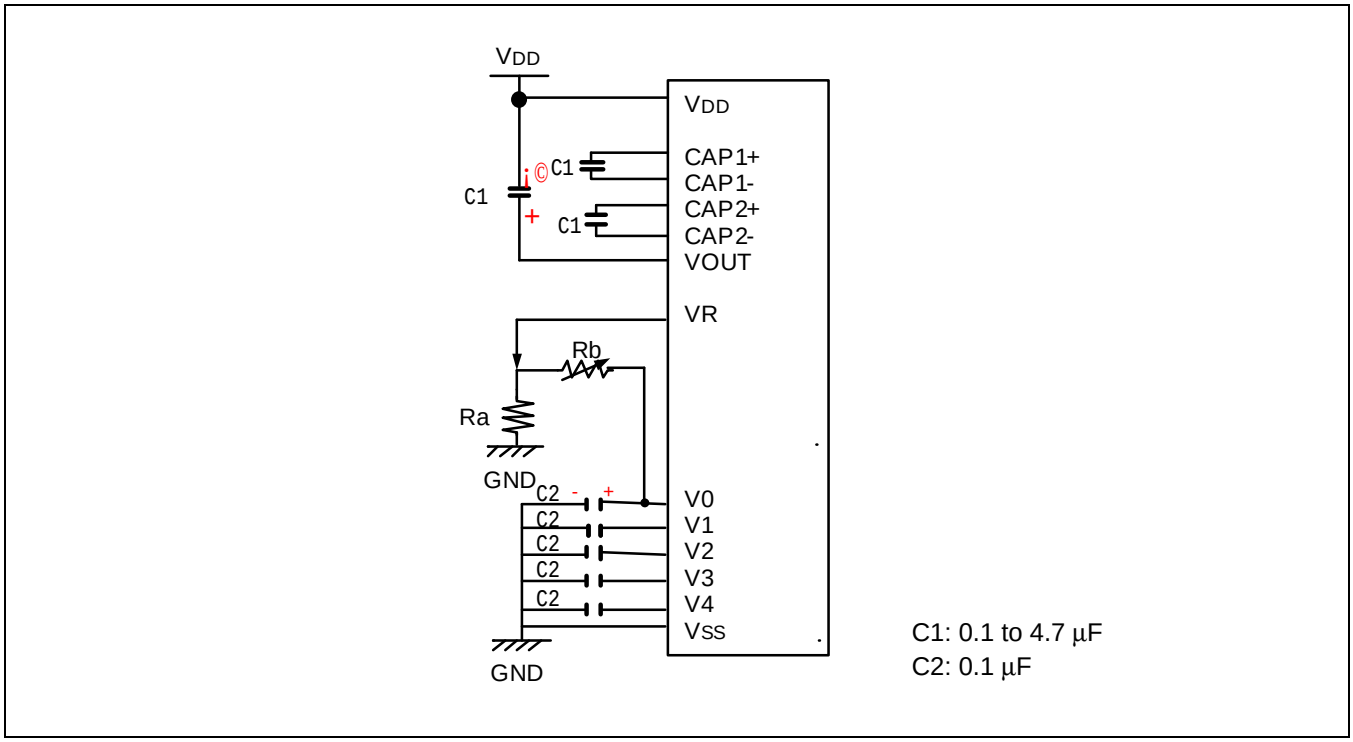


Figure 21. When Built-in Power Supply is Used (VC, VR, VF = 1, 1, 1)

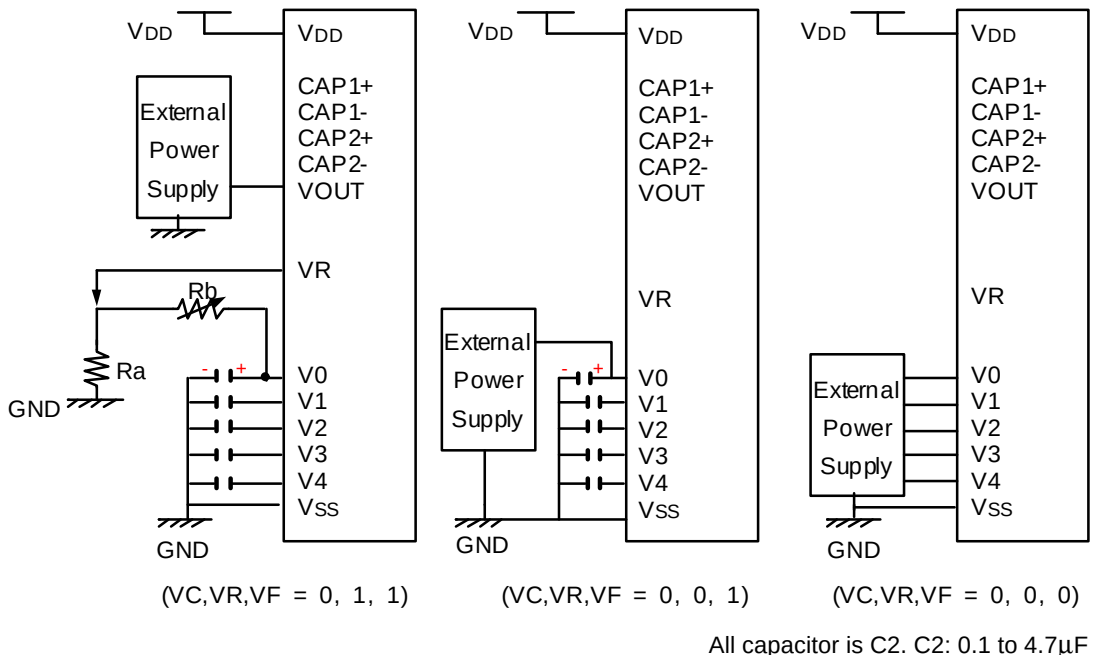


Figure 22. When External Power Supply is Used

MPU INTERFACE

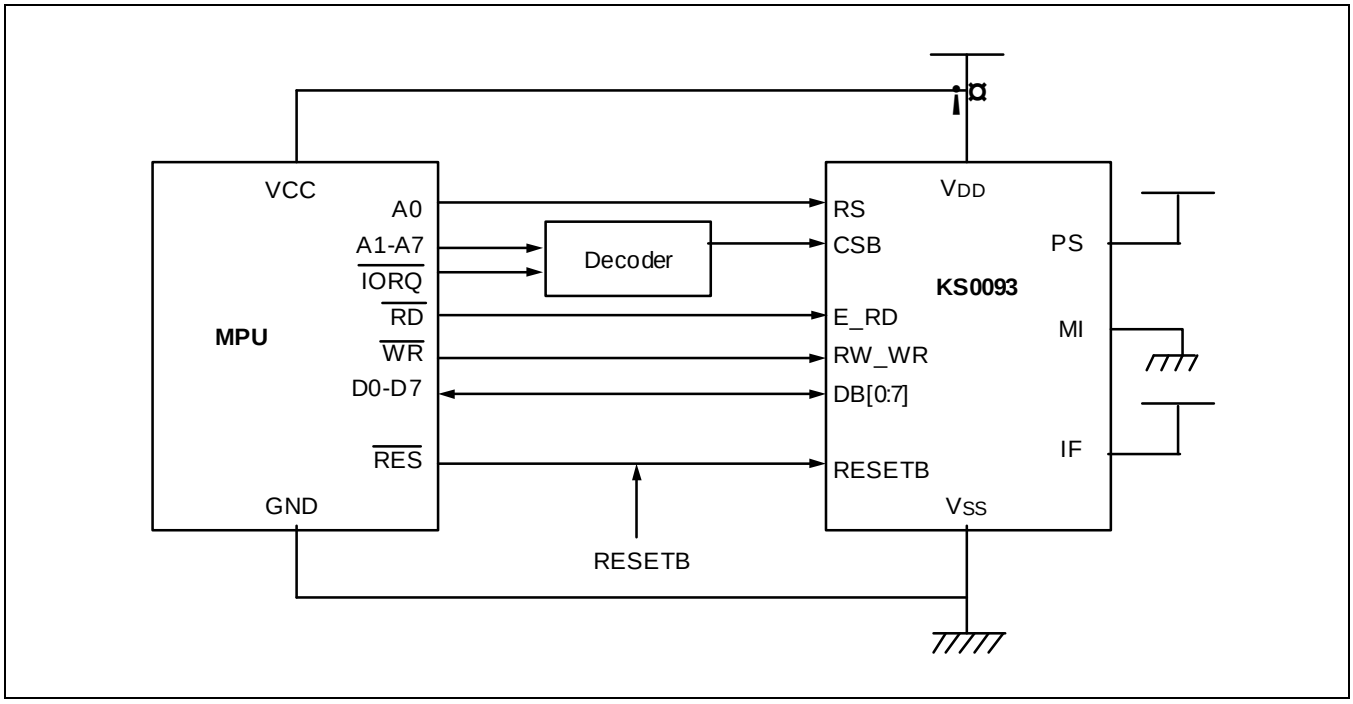


Figure 23. Parallel Interfacing With 8080-series Microprocessors

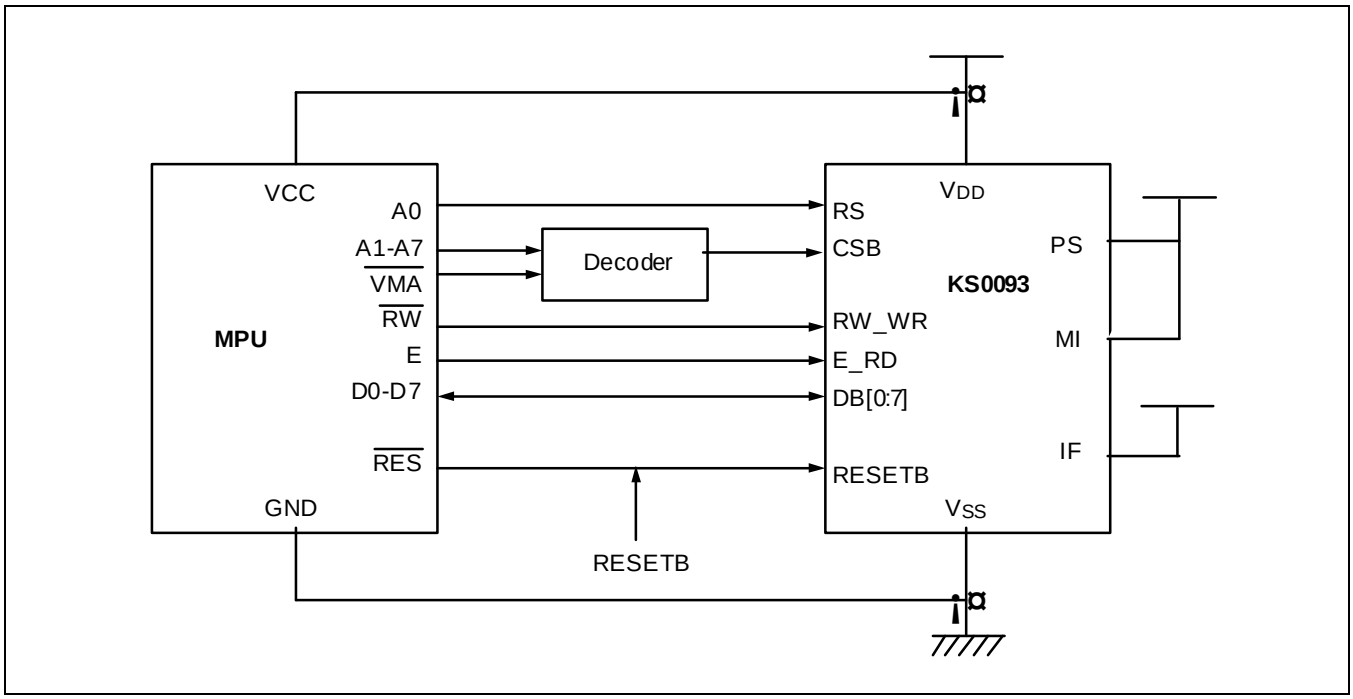


Figure 24. Parallel Interfacing With 6800-series Microprocessors

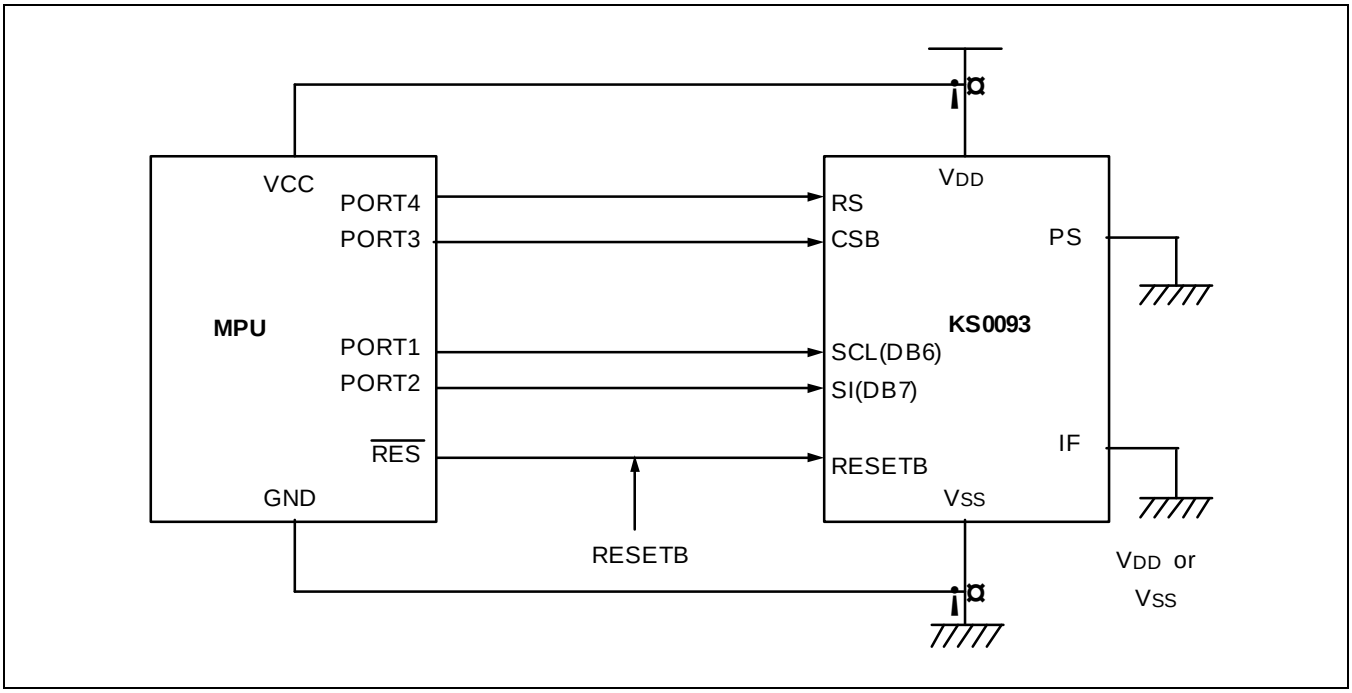


Figure 25. Clock Synchronized Serial Interfacing With Any Microprocessor

APPLICATION INFORMATION FOR LCD PANEL

CHIP BOTTOM & LOWER VIEW (S BIT = “0”, DIRS = “0”)

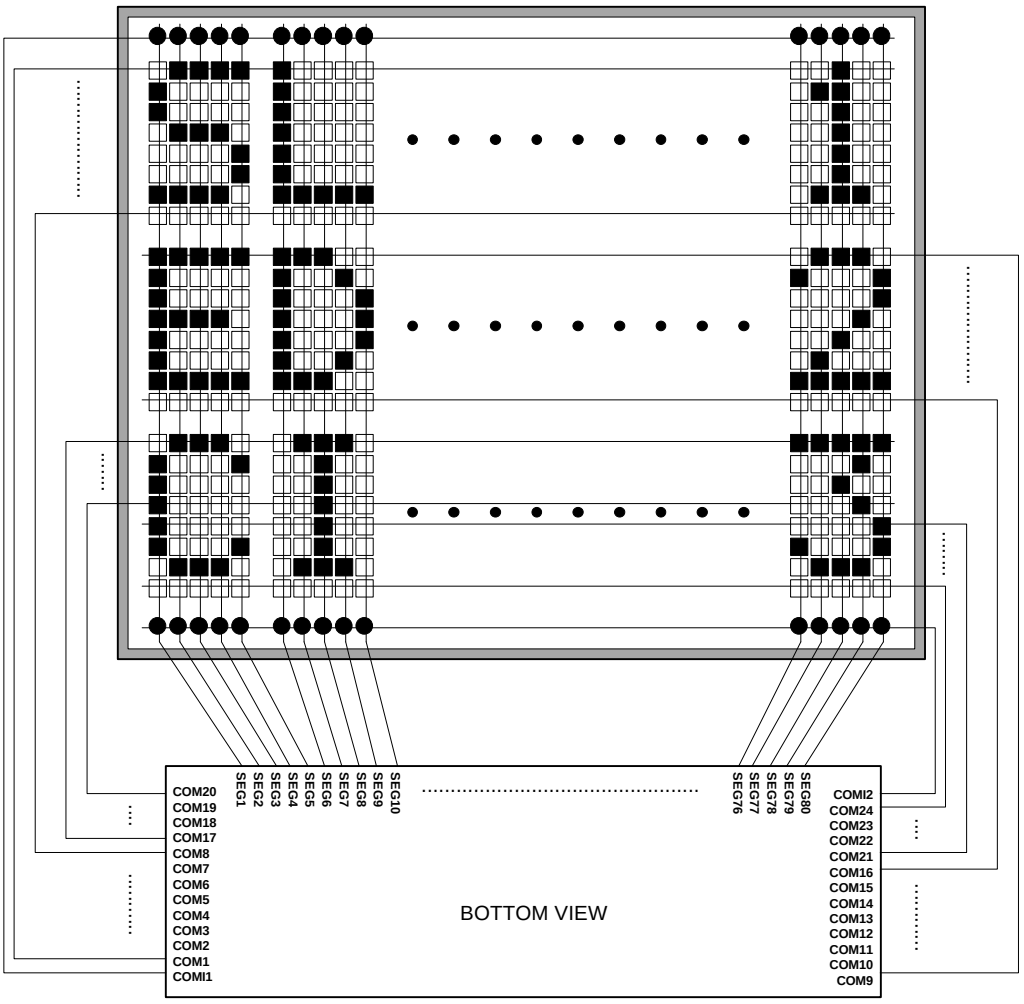


Figure 26. Chip Bott & Lower View (S Bit = “0”, DIRS = “0”)

CHIP BOTTOM & UPPER VIEW (S BIT = “1”, DIRC = “1”)

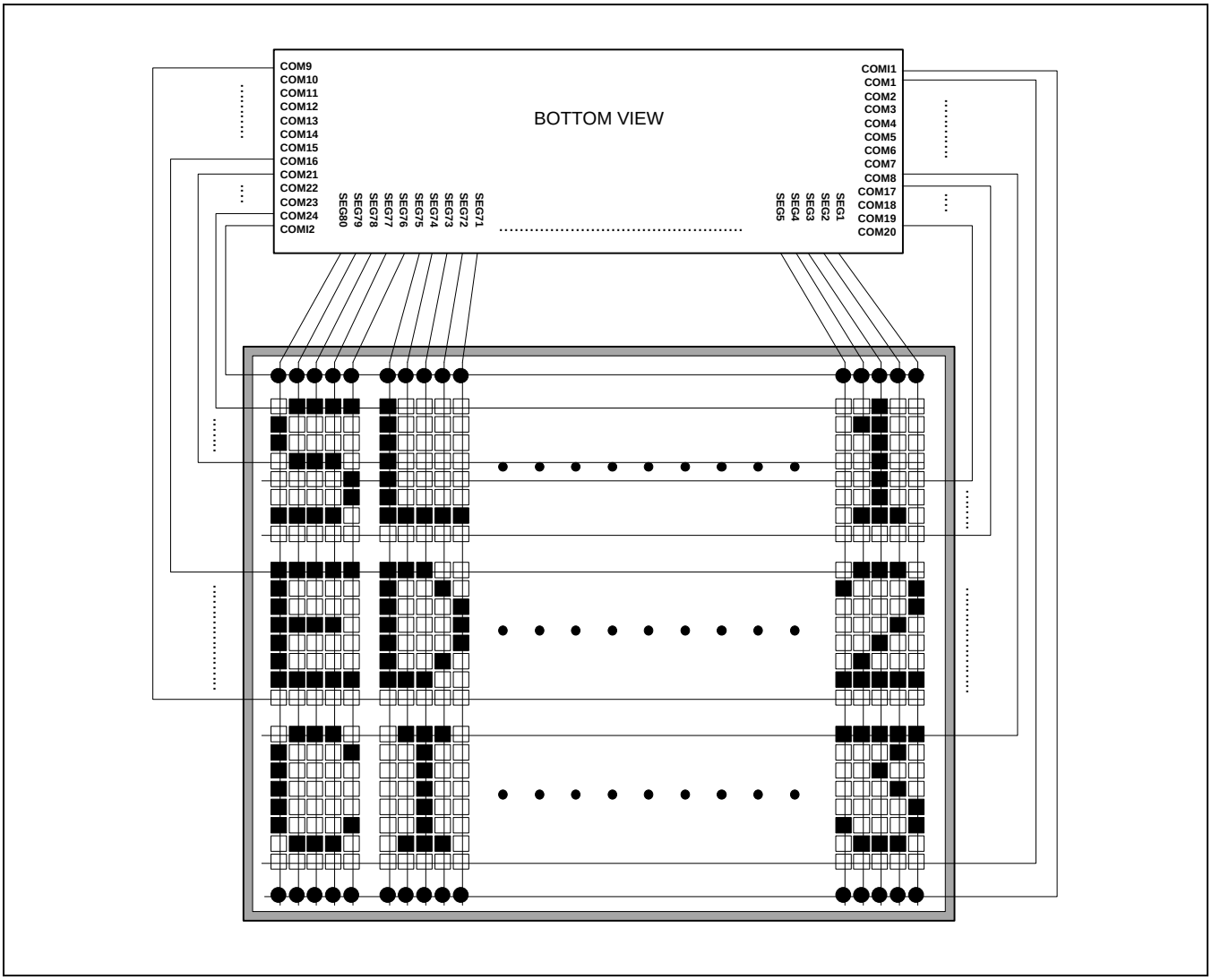


Figure 27. Chip Bottom & Upper View (S Bit = “1”, DIRS = “1”)

CHIP TOP & LOWER VIEW (S BIT = “0”, DIRS = “1”)

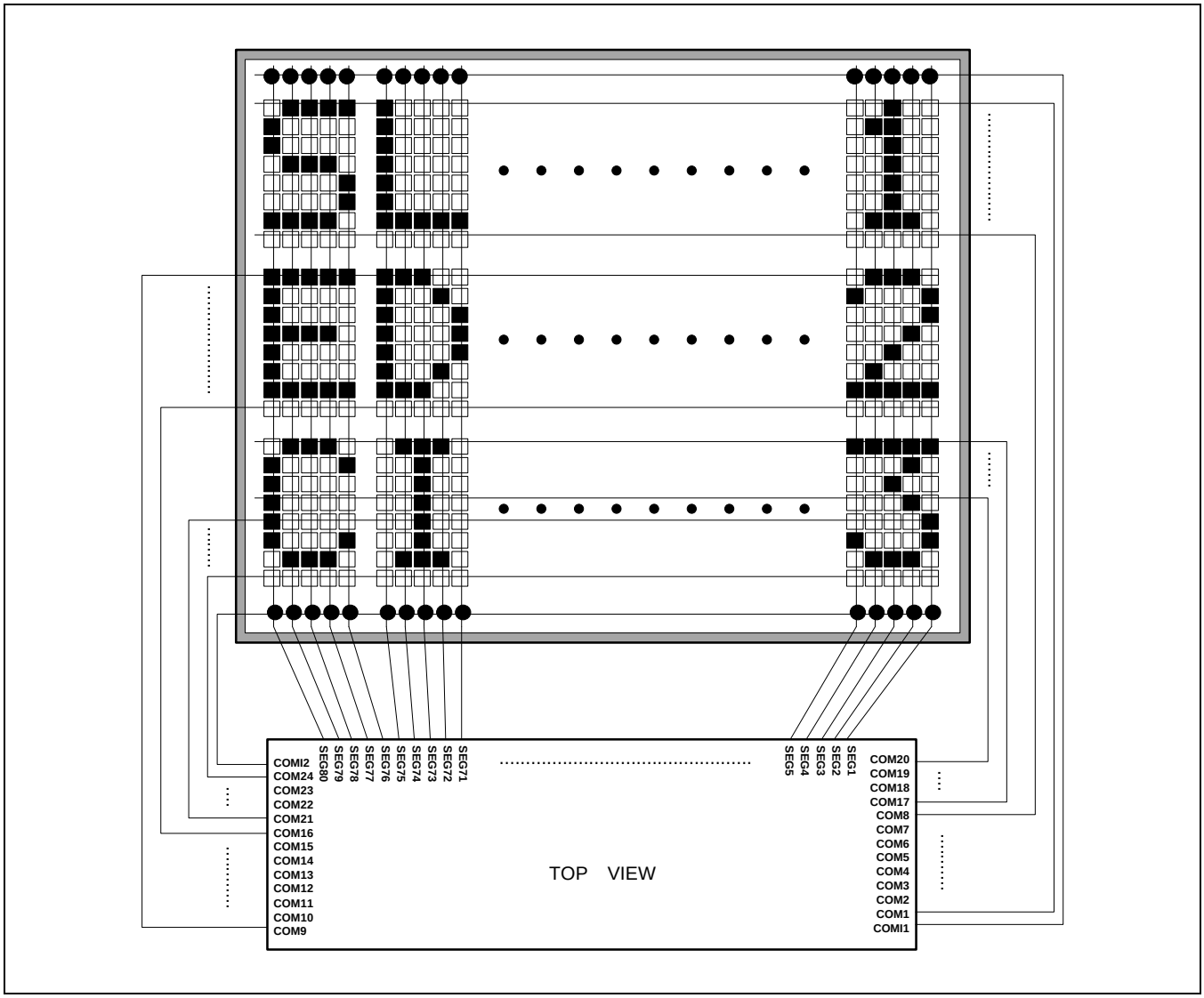


Figure 28. Chip Top & Lower View (S Bit = “0”, DIRS = “1”)

CHIP TOP & UPPER VIEW (S BIT = “1”, DIRS = “0”)

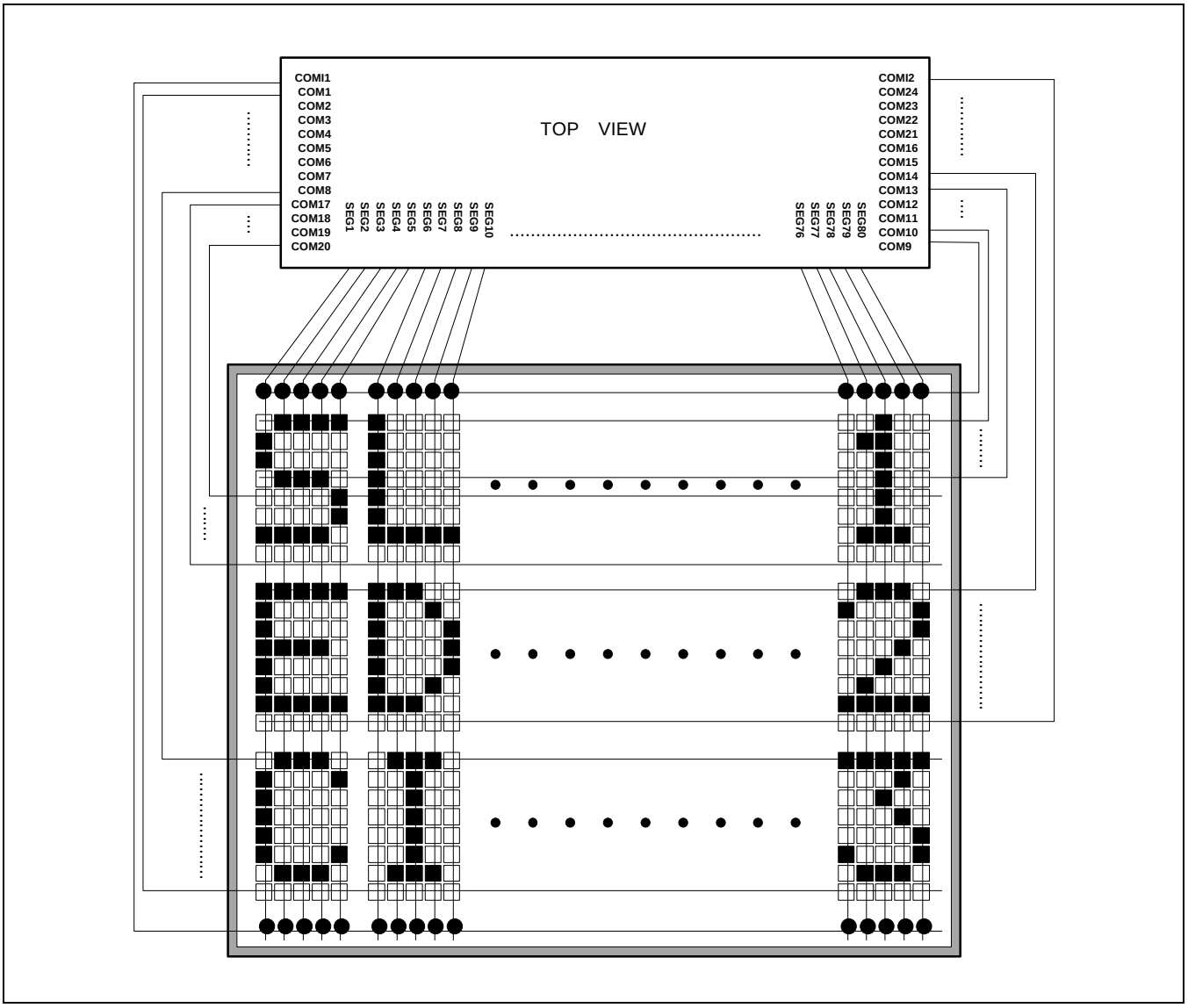
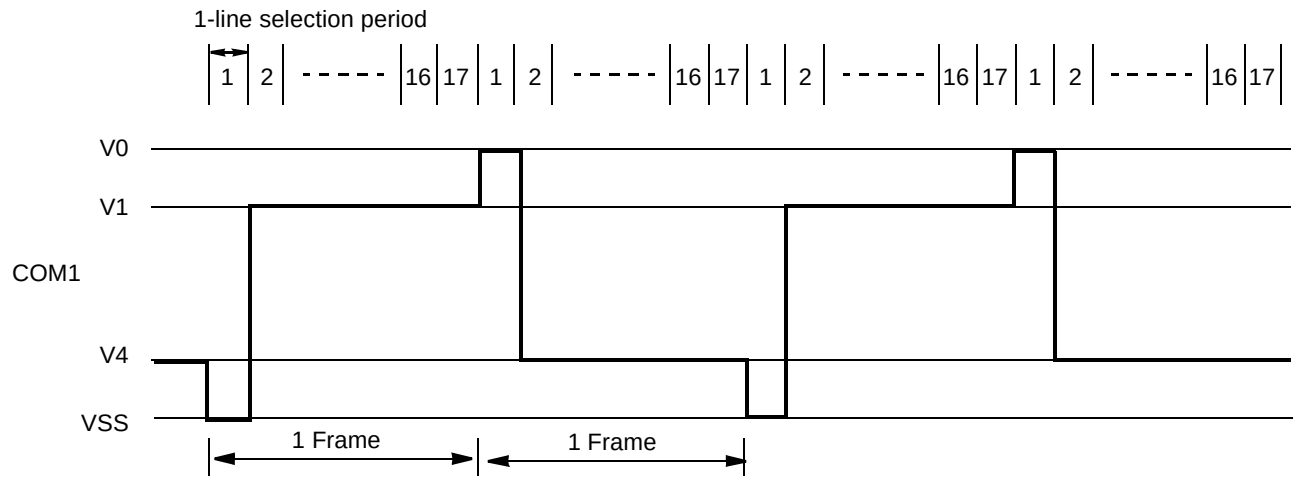


Figure 29. Chip Top & Upper View (S Bit = “1”, DIRS = “0”)

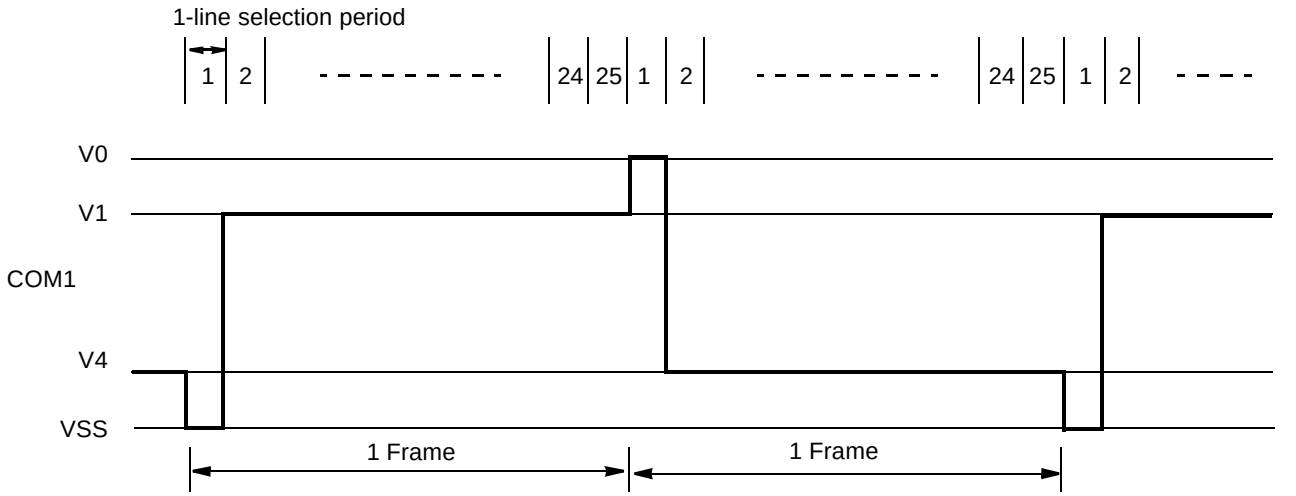
FRAME FREQUENCY

1/17 DUTY (2-LINE MODE)



1-line selection period = 16 clocks
One Frame = 16 × 17 × 36.8 µs = 10.0 ms (1 clock = 36.8 µs at fosc = 27.2 kHz)
Frame frequency = 1/10.0 ms = 100 Hz

1/25 DUTY (3-LINE MODE)



1-line selection period = 16 clocks
One Frame = 16 × 25 × 25 µs = 10.0 ms (1 clock = 25 µs at fosc = 40 kHz)
Frame frequency = 1/10.0 ms = 100 Hz

MAXIMUM ABSOLUTE RATINGS

Table 12. Maximub Absolute Ratings

Characteristics	Symbol	Value	Unit
Power supply voltage (1)	V_{DD}	– 0.3 to + 7.0	V
Power supply voltage (2)	V0, VOUT	– 0.3 to + 8.0	V
Power supply voltage (3)	V1, V2, V3, V4	– 0.3 to V0	V
Input voltage	V_{IN}	– 0.3 to V_{DD} + 0.3	V
Operating temperature	T_{OPR}	– 30 to + 85	°C
Storage temperature	T_{STG}	– 55 to + 125	°C

NOTES:

1. All the voltage levels are based on V_{SS} = 0V
2. Voltage greater than above may damage the circuit
   Voltage level: VOUT ≥ V0 ≥ V_{DD} ≥ V_{SS}
   Voltage level: V0 ≥ V1 ≥ V2 ≥ V3 ≥ V4 ≥ V_{SS}

ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS

Table 13. DC Characteristics

(V_{DD} = 2.4V to 3.6V, Ta = – 30 to + 85°C)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit
Operating voltage		V_{DD}	–	2.4	–	3.6	V
Supply current (V_{DD} = 5V, Ta = 25°C)		I_{DD1}	Display operation, VLCD = 6 V without load no access from MPU	–	–	80	µA
		I_{DD2}	Access operation from MPU Fcyc = 200kHz	–	–	500	
		I_{DDS1}	Sleep operation without load oscillator OFF, power save ON	–	–	5	
Input voltage		V_{IH}	–	$0.7V_{DD}$	–	VDD	V
		V_{IL}	–	V_{SS}	–	0.3VDD	
Output voltage		V_{OH}	I_{OH} = –1mA, V_{DD} = 2.4V	V_{DD}–0.4	–	–	V
		V_{OL}	I_{OL} = 1mA, V_{DD} = 2.4V	–	–	0.4	
Input leakage current		I_{IZ}	V_{IN} = 0V to V_{DD}	–1	–	1	µA
Output leakage current		I_{OZ}	V_{IN} = 0 V to V_{DD}	–3	–	3	µA
R_{ON} resistance		R_{COM}	I_O = ± 50µA	–	–	5	KΩ
		R_{SEG}	I_O = ± 50µA	–	–	10	
Frame frequency (Internal)		f_{FR}	V_{DD} = 3V, Ta = 25°C	70	100	130	Hz
Voltage converter	Conversion efficiency	V_{EF}	RL = ∞	95	99	–	%
	Outpu voltage	V_{OUT}	Ta = 25°C, C = 1µF	6.9	7.2	7.5	V
Voltage regulator reference voltage		V_{REF}	Ta = 25°C	1.94	2.0	2.06	V
LCD driving voltage		V_{LCD}	V_{LCD} = V0 – V_{SS}	4.0	–	6.0	

Table 14. DC Characteristics

(V_{DD} = 3.6V to 5.5V, Ta = – 30 to + 85°C)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit
Operating voltage		V_{DD}	–	3.6	–	5.5	V
Supply current (V_{DD} = 5V, Ta = 25°C)		I_{DD1}	Display operation V0 = 6V without load no access from MPU	–	–	100	µA
		I_{DD2}	Access operation from MPU fcyc = 200kHz	–	–	1000	
		I_{DDS1}	Sleep operation without load oscillator OFF, power save ON	–	–	10	
Input voltage		V_{IH}	–	0.7 V_{DD}	–	V_{DD}	V
		V_{IL}	–	V_{SS}	–	0.3 V_{DD}	
Output voltage		V_{OH}	I_{OH} = – 1mA, V_{DD} = 4.0V	V_{DD} – 0.4	–	–	V
		V_{OL}	I_{OL} = 1mA, V_{DD} = 4.0V	–	–	0.4	
Input leakage current		I_{IZ}	V_{IN} = 0V to V_{DD}	–1	–	1	µA
Output leakage current		I_{OZ}	V_{IN} = 0V to V_{DD}	–3	–	3	
R_{ON} resistance		R_{COM}	I_O = ± 50µA	–	–	5	KΩ
		R_{SEG}	I_O = ± 50µA	–	–	10	
Frame frequency (Internal)		f_{FR}	V_{DD} = 5V, Ta = 25°C	70	100	130	Hz
Voltage converter	Conversion efficiency	V_{EF}	RL = ∞	95	99	–	%
	Output voltage	V_{OUT}	Ta = 25°C, C = 1µF	6.9	7.2	7.5	V
Voltage regulator reference voltage		V_{REF}	Ta = 25°C	1.94	2.0	2.06	V
LCD driving voltage		V_{LCD}	V_{LCD} = V0 – V_{SS}	4.0	–	6.0	

AC CHARACTERISTICS

Parallel Write Interface Mode (68 Mode)

(V_{DD} = 2.4V to 3.6V, Ta = – 30 to + 85°C)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
E_RD cycle time	t_C	650	–	–	ns
Pulse rise / fall time	t_R, t_F	–	–	25	
E_RD pulse width high	t_{WH}	450	–	–	
E_RD pulse width low	t_{WL}	150	–	–	
RS and CSB setup time	t_{SU1}	60	–	–	
RS and CSB hold time	t_{H1}	30	–	–	
DB setup time	t_{SU2}	100	–	–	
DB hold time	t_{H2}	50	–	–	

(V_{DD} = 3.6V to 5.5V, Ta = – 30 to + 85°C)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
E_RD cycle time	t_C	350	–	–	ns
Pulse rise / fall time	t_R, t_F	–	–	25	
E_RD pulse width high	t_{WH}	250	–	–	
E_RD pulse width low	t_{WL}	100	–	–	
RS and CSB setup time	t_{SU1}	40	–	–	
RS and CSB hold time	t_{H1}	10	–	–	
DB setup time	t_{SU2}	40	–	–	
DB hold time	t_{H2}	10	–	–	

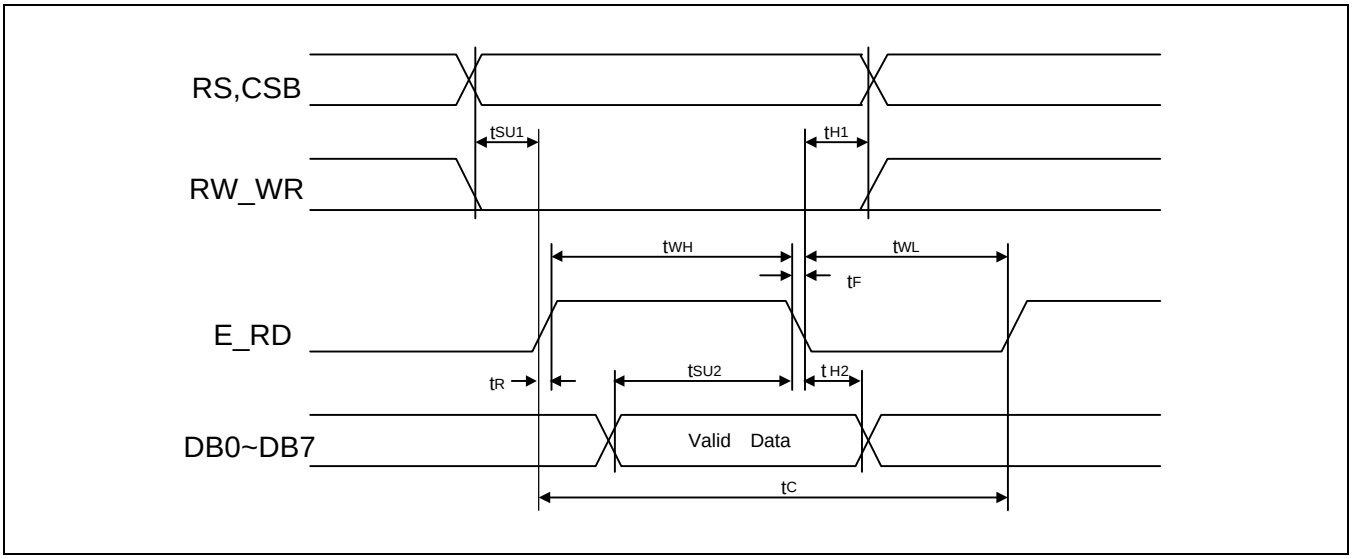


Figure 30. Write Timing Diagram (6800-series MPU Interface)

Parallel Read Interface Mode (68 Mode)

(V_{DD} = 2.4V to 3.6V, Ta = – 30 to + 85°C)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
E_RD cycle time	t_C	650	–	–	ns
Pulse rise / fall time	t_R, t_F	–	–	25	
E_RD pulse width high	t_{WH}	450	–	–	
E_RD pulse width low	t_{WL}	150	–	–	
RS and CSB setup time	t_{SU}	60	–	–	
RS and CSB hold time	t_H	30	–	–	
DB output delay time	t_D	100	–	–	
DB output hold time	t_{DH}	50	–	–	

(V_{DD} = 3.6V to 5.5V, Ta = – 30 to + 85°C)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
E_RD cycle time	t_C	650	–	–	ns
Pulse rise / fall time	t_R, t_F	–	–	25	
E_RD pulse width high	t_{WH}	450	–	–	
E_RD pulse width low	t_{WL}	150	–	–	
RS and CSB setup time	t_{SU}	60	–	–	
RS and CSB hold time	t_H	30	–	–	
DB output delay time	t_D	100	–	–	
DB output hold time	t_{DH}	50	–	–	

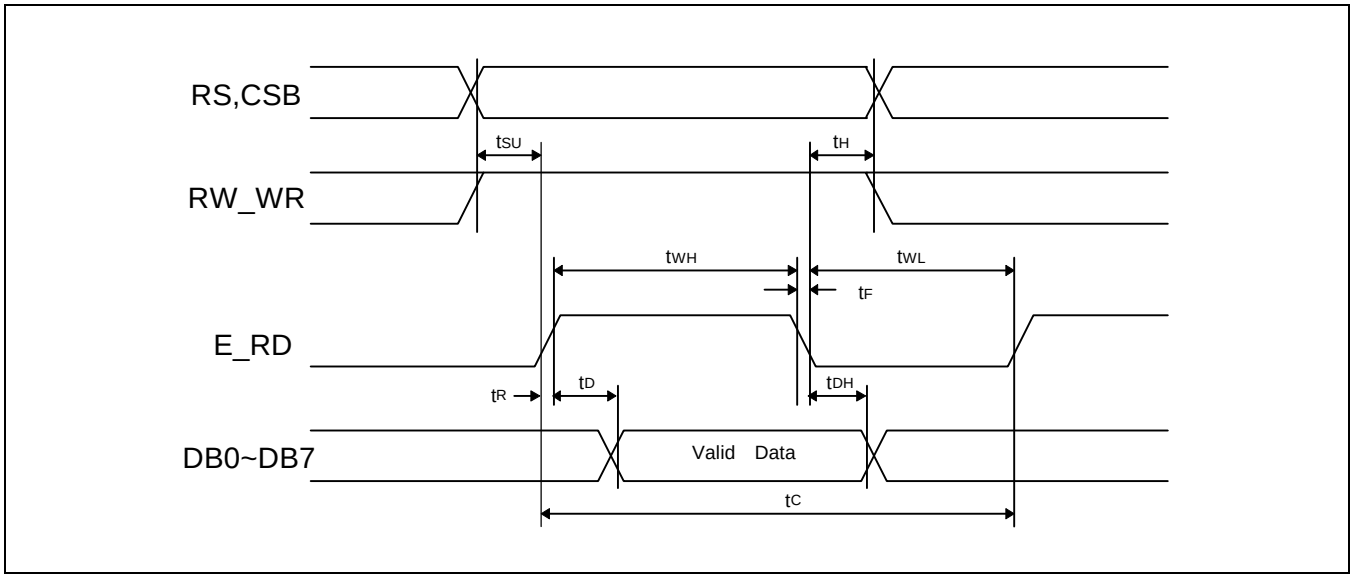


Figure 31. Read Timing Diagram (6800-series MPU Interface)

Parallel Write Interface Mode (80 Mode)

(V_{DD} = 2.4 to 3.6V, Ta = – 30 to + 85°C)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
RW_WR cycle time	t_C	650	–	–	ns
Pulse rise / fall time	t_R, t_F	–	–	25	
RW_WR pulse width high	t_{WH}	150	–	–	
RW_WR pulse width low	t_{WL}	450	–	–	
RS and CSB setup time	t_{SU1}	60	–	–	
RS and CSB hold time	t_{H1}	30	–	–	
DB setup time	t_{SU2}	100	–	–	
DB hold time	t_{H2}	50	–	–	

(V_{DD} = 3.6V to 5.5V, Ta = – 30 to + 85°C)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
RW_WR cycle time	t_C	350	–	–	ns
Pulse rise / fall time	t_R, t_F	–	–	25	
RW_WR pulse width high	t_{WH}	250	–	–	
RW_WR pulse width low	t_{WL}	100	–	–	
RS and CSB setup time	t_{SU1}	40	–	–	
RS and CSB hold time	t_{H1}	10	–	–	
DB setup time	t_{SU2}	40	–	–	
DB hold time	t_{H2}	10	–	–	

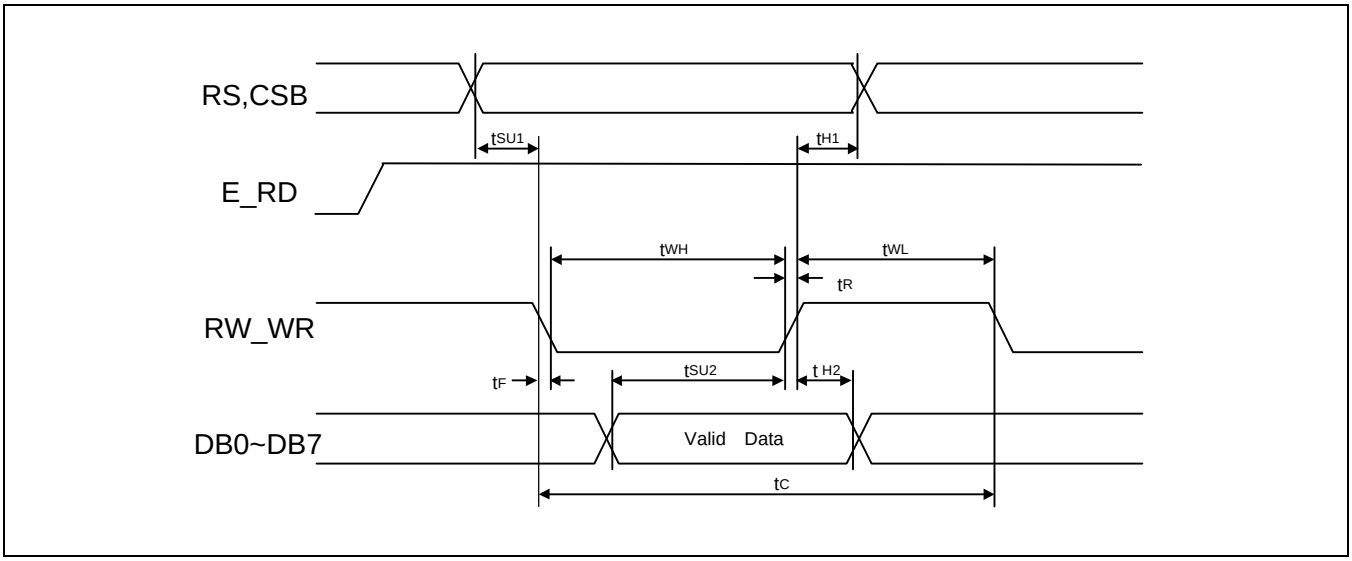


Figure 32. Write Timing Diagram (80-series MPU Interface)

Parallel Read Interface (80 Mode)

(V_{DD} = 2.4V to 3.6V, Ta = – 30 to + 85°C)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
E_RD cycle time	t_C	650	–	–	ns
Pulse rise / fall time	t_R, t_F	–	–	25	
E_RD pulse width high	t_{WH}	450	–	–	
E_RD pulse width low	t_{WL}	150	–	–	
RS and CSB setup time	t_{SU}	60	–	–	
RS and CSB hold time	t_H	30	–	–	
DB output delay time	t_D	100	–	–	
DB output hold time	t_{DH}	50	–	–	

(V_{DD} = 3.6V to 5.5V, Ta = – 30 to + 85°C)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
E_RD cycle time	t_C	650	–	–	ns
Pulse rise / fall time	t_R, t_F	–	–	25	
E_RD pulse width high	t_{WH}	450	–	–	
E_RD pulse width low	t_{WL}	150	–	–	
RS and CSB setup time	t_{SU}	60	–	–	
RS and CSB hold time	t_H	30	–	–	
DB output delay time	t_D	100	–	–	
DB output hold time	t_{DH}	50	–	–	

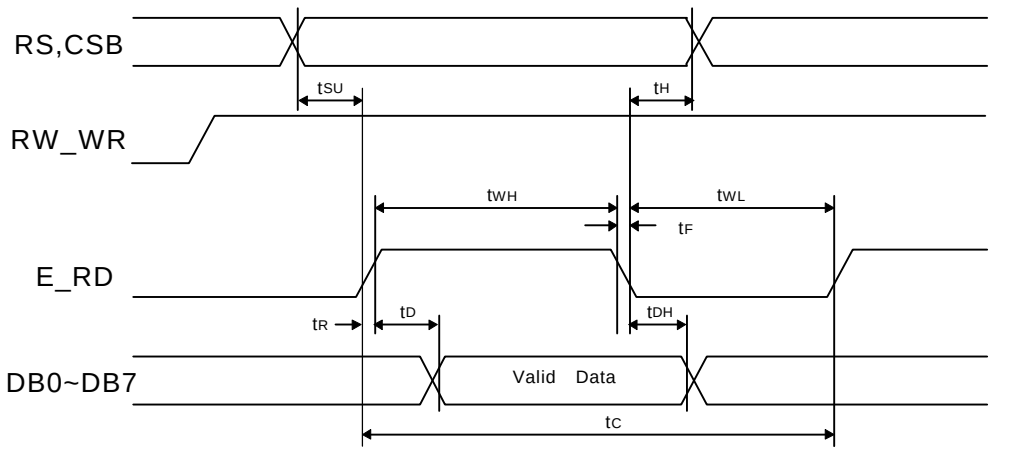


Figure 33. Read Timing Diagram (80-series MPU Interface)

Clock Synchronized Serial Mode

(V_{DD} = 2.4V to 3.6V, Ta = – 30 to + 85°C)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
SCL clock cycle time	t_C	1000	–	–	ns
Pulse rise / fall time	t_R, t_F	–	–	25	
SCL clock width (High, Low)	t_W	300	–	–	
CSB setup time	t_{SU1}	150	–	–	
CSB hold time	t_{H1}	700	–	–	
RS data setup time	t_{SU2}	50	–	–	
RS data hold time	t_{H2}	300	–	–	
SI data setup time	t_{SU3}	50	–	–	
SI data hold time	t_{H3}	50	–	–	

(V_{DD} = 3.6V to 5.5V, Ta = – 30 to + 85°C)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
SCL clock cycle time	t_C	600	–	–	ns
Pulse rise / fall time	t_R, t_F	–	–	25	
SCL clock width (High, Low)	t_W	200	–	–	
CSB setup time	t_{SU1}	100	–	–	
CSB hold time	t_{H1}	400	–	–	
RS data setup time	t_{SU2}	40	–	–	
RS data hold time	t_{H2}	200	–	–	
SI data setup time	t_{SU3}	40	–	–	
SI data hold time	t_{H3}	40	–	–	

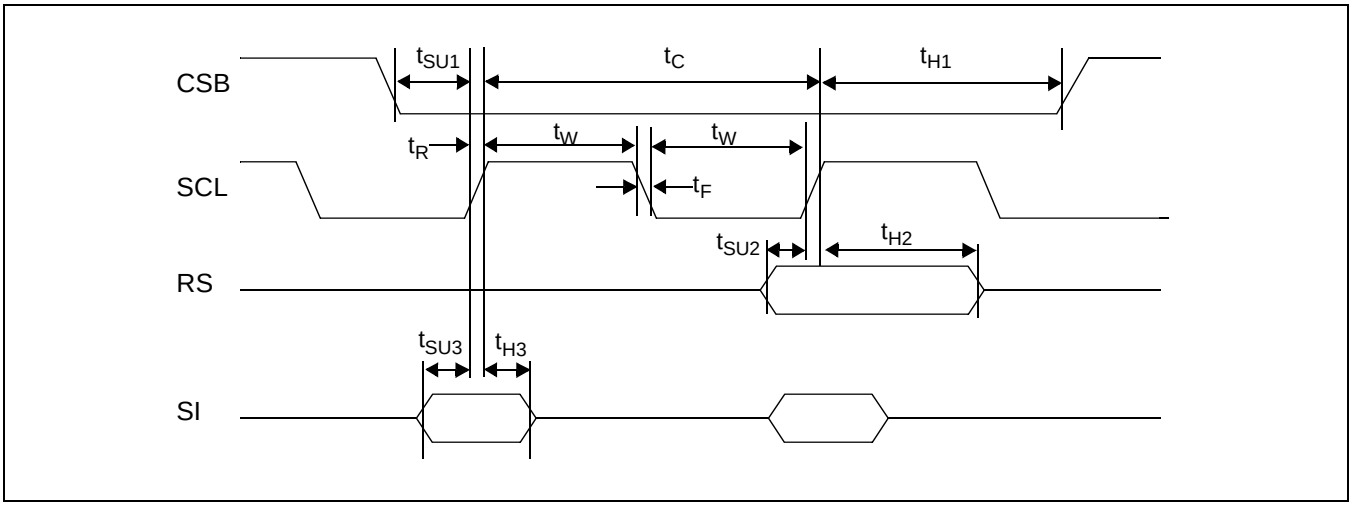


Figure 34. Clock Synchronized Serial Interface Mode Timing Diagram