

SERVO CONTROLLER for VCR

KA8334B is a servo controller with built-in digital servo function and analog amplifiers, can select the head specifications and search speed that is able to correspond to multi function VCR.

60 - QFP - 1414A

ORDER INFORMATION

DEVICE	PACKAGE	OPERATING TEMPERATURE
KA8334B	60 QFP	- 10 °C ~ + 75 °C

FEATURES

- Using the limit amplifier for D-FG signal, the AM variation is minimum.
- Built-in D-PG amplifier.
- 4HD switching logic output.
- Wide aspect VISS write, rewrite.
- Head switching point is controlled by the analog M.M. & the serial data 8 bits.
- Contains a C-FG frequency doubling block.
- ASB(assemble) mark writing & detecting.
- 9H & 12H mode selection
- 6.5H detect output between video head switching and V-sync.
- The D-P / D & C-P/D outputs are fixed by serial data.
- SW D & SW E are controlled by serial data.
- The output of skip data (When CTL signal is skipped.) & Compensation of Capatan phase.
- 4 step switching for P.CTL schmitt width.
- ½ VDD is charged to the capacitor of P/D filter when supply voltage is applied.
- Wide aspect discretion data (full mode & letterbox mode) writing

MAXIMUM RATING ($T_a = 25\text{ }^{\circ}\text{C}$)

	Parameter	Symbol	Value	Unit
1	Power supply	VCC	6.0	V
2	Operating voltage	V _{OPR}	4.5 ~ 5.5	V
3	Storage temperature	T _{STG}	- 40 ~ 125	°C
4	Operating temperature	T _{OPR}	- 10 ~ 70	°C
5	Power dissipation	P _T	500	mW

ELECTRO - STATIC DISCHARGE

	CONDITION	VALUE	UNIT
ALL PIN	R = 1.5K C = 100pF	+ / - 1500 and over	VOLT

Previous condition: Human Body Electrostatic Mode 1

ELECTRICAL CHARACTERISTICS (Ta = 25 °C, Vcc= 5V)

Parameter	SYM-BOL	TEST CONDITIONS	SPECIFICATIONS			Unit	APPLICATION TERMINAL
			MIN	TYP	MAX		
Quiscent current	I _{CC}	No load Pin23 & Pin 33 Sum	8.0	30	42	mA	23,33
2 value output voltage	V _{OL}	No load	-	0.0	0.05	V	40 ~ 43.45 51 ~ 57
2 value output voltage	V _{OH}	No load	4.9	5.0	-	V	40 ~ 43.45 51 ~ 57
2 value output voltage	V _{IL}	Load current = 2mA	-	0.6	1.2	V	40 ~ 43.45 51 ~ 57
2 value output voltage	V _{IH}	Load current = 2mA	3.8	4.4	-	V	40 ~ 43.45 51 ~ 57
PULL UP output voltage	V _{OL}	No load	0.0	0.1	0.3	V	34
PULL UP output voltage	V _{OH}	No load	4.9	5.0	-	V	34
PULL UP output voltage	V _{IL}	Load current = 1mA	-	0.6	1.2	V	34
PULL UP resistance	R _H		6.0	9.0	13.0	kΩ	34
3 value output voltage	V _{OL}	No load	0.0	0.2	0.4	V	44

ELECTRICAL CHARACTERISTICS (Continued)

Parameter	SYM-BOL	TEST CONDITIONS	SPECIFICATIONS			Unit	APPLICATION TERMINAL
			MIN	TYP	MAX		
3 value output voltage	V _{OM}	No load	2.3	2.5	2.8	V	44
3 value output voltage	V _{OH}	No load	4.6	4.8	5.0	V	44
3 value output voltage	V _{IL}	Load current = 1mA	-	0.6	1.2	V	44
3 value output voltage	V _{IH}	Load current = 1mA	3.8	4.4	-	V	44
3 value M level output impedance	R _M		6.0	9.0	13.0	kΩ	44
REC CTL output pin to pin voltage	V _{CTL}	No load, Potential between pin24 & pin 25	4.6	4.8	5.0	V	24, 25
REC CTL output impedance	R _{CTL}	1 ≤ I _{LOAD} ≤ 2mA 24pin & 25pin Sum	-	250	500	Ω	24, 25
2 value input V _{TH}	V _{TH}		1.5	2.5	3.5	V	
2 value input V _{TH}	V _{TH}		1.0	--	4.0	V	49, 50
2 value input pull up resistance	R _{H1}		6.0	9.0	13.0	kΩ	48 ~ 50
3 value input V _{TH}	V _{TH1}	V _{TH} of L / M	1.0	1.4	1.9	V	3, 4
3 value input V _{TH}	V _{TH2}	V _{TH} of M / H	3.1	3.5	4.0	V	3, 4
3 value input voltage	V _M		2.0	2.5	2.9	V	3, 4
3 value input input resistance	R _{M1}		18.5	28.0	42.0	kΩ	3, 4
fsc Amp. Gain	A _{fsc}	Internal OSC	20	-	-	dB	35, 36
fsc input sensivity	V _{fsc}	Internal OSC	-	-	150	mVpp	37
CTLP schmitt input voltage	V _{m31}		2.2	2.5	2.8		31



ELECTRICAL CHARACTERISTICS (Continued)

Parameter	SYM-BOL	TEST CONDITIONS	SPECIFICATIONS			Unit	APPLICATION TERMINAL
			MIN	TYP	MAX		
CTLP schmitt input V _{TH}	VP TH1	normal speed	105	150	180	mV _{OP}	31
CTLP schmitt input V _{TH}	VM TH1	normal speed	-180	-150	-105	mV _{OP}	31
CTLP schmitt input V _{TH}	VP TH2	medium speed search	240	300	360	mV _{OP}	31
CTLP schmitt input V _{TH}	VM TH2	medium speed search	-360	-300	-240	mV _{OP}	31
CTLP schmitt input V _{TH}	VP TH3	high speed search	520	600	680	mV _{OP}	31
CTLP schmitt input V _{TH}	VM TH3	high speed search	-680	-600	-520	mV _{OP}	31
CTLP schmitt input V _{TH}	VP TH4	During VISS detect	900	1000	1100	mV _{OP}	31
PCTL schmitt input V _{TH}	VM TH4	During VISS detect	-1100	-1000	-900	mV _{OP}	31
C.FG Input volt.	VM32		2.2	2.5	2.8	V	32
C.FG schmitt width	VP TH5		105	150	180	mV _{PP}	32
C.FG schmitt width	VM TH5		-180	-150	-105	mV _{PP}	32
D.PG schmitt input V _{TH}	VP TH5	Input external resistor = 100k Ω	350	480	700	mV _{OP}	60
D.PG schmitt input V _{TH}	VM TH5	difference with VP TH5	150	310	520	mV _{OP}	60
D.FG. AMP. Input voltage	VM2		2.2	2.5	2.8	V	2
D.FG AMP input sensivity	VLMA		-	-	10	mV _{PP}	2
D.PG Input voltage	VM60		2.2	2.5	2.8	V	60



ELECTRICAL CHARACTERISTICS (Continued)

Parameter	SYM BOL	TEST CONDITIONS	SPECIFICATIONS			Unit	APPLICATION TERMINAL
			MIN	TYP	MAX		
Power on reset input V _{TH}	V39TH		2.9	3.5	4.1	V	39
Power on reset input current	IM39		1.0	2.0	5.0	uA	39
Sync input V _{TH}	V46TH	at DC input	1.5	2.5	3.5	V	46
Sync input pin voltage	V46		1.8	2.4	2.8	V	46
Sync input sensitivity	VSYC	DUTY 10% square At coupling cap, measure peak value	50	100	200	mVpp	46
Sync input Input impedance	R46		18.5	28.0	42.0	kΩ	46
D.PG M.M V _{TH}	VMMT	D.PG M.M pin	2.2	2.5	2.8	V	59
CTL P amp gain	ACTL	f=4KHz	37	40	43	dB	24,25,28,30
Drum mix amp gain	AD	f=4KHz	37	40	43	dB	5,6,9
CAP. mix amp gain	AC	f=4KHz	37	40	43	dB	15,20,22
Analog SW off leakage current	ILK		-1.0	0.0	1.0	uA	SWA - SWM
Analog SW on resistance	RASW		-	400	1000	Ω	SWA - SWL

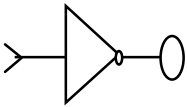
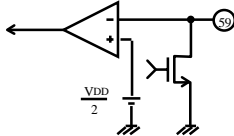
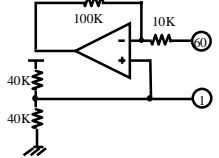
PIN DESCRIPTIONS

Pin No	Function	Descriptions	Input/Output form																				
1	DRUM Common	The common pin of D-FG and D-PG signal. Bias voltage : about 2.5V																					
2	DRUM FG IN	D-FG Input minimum level : 10mV. note) Refer to Head switching timing chart																					
3	DRUM A SELECT	3 value input OPEN = ㄹ																					
4	B	Note)Refer to head switching timing chart																					
		<table border="1"> <thead> <tr> <th>B</th> <th>A</th> <th>H</th> <th>M</th> <th>L</th> </tr> </thead> <tbody> <tr> <td>H</td> <td></td> <td>2 HEAD ①</td> <td>2 HEAD ②</td> <td>2 HEAD ③</td> </tr> <tr> <td>M</td> <td></td> <td>DA4 - ①</td> <td>DA4 - ②</td> <td>DA4 - ③</td> </tr> <tr> <td>L</td> <td></td> <td>DA4-①TEST</td> <td>DA4-②TEST</td> <td>DA4-③TEST</td> </tr> </tbody> </table>		B	A	H	M	L	H		2 HEAD ①	2 HEAD ②	2 HEAD ③	M		DA4 - ①	DA4 - ②	DA4 - ③	L		DA4-①TEST	DA4-②TEST	DA4-③TEST
B	A	H		M	L																		
H		2 HEAD ①	2 HEAD ②	2 HEAD ③																			
M		DA4 - ①	DA4 - ②	DA4 - ③																			
L		DA4-①TEST	DA4-②TEST	DA4-③TEST																			
5	D.MIX OUT																						
6	D.MIX (-)	Drum mix amp, capstan mix amp																					
9	D.MIX (+)	Open loop gain ----->																					
15	C.MIX (+)	At the full feedback, no oscillation																					
20	C.MIX (-)	Output dynamic range: 0~ 5V (No load)																					
22	C.MIX OUT	Output impedance ≤ 2kΩ																					
7	D.F/V OUT																						
11	D.P/D OUT	SW capacitor DA output.																					
14	C.P/D OUT	Output dynamic range: 0.5 ~ 4.3V																					
16	C.F/V OUT	Output impedance ≤ 500Ω																					
8	N.C (GND)	GND Connected.																					
10 (SW I), 12 (SW J), 13 (SW M), 17 (SW H), 18 (SW G), 19 (SW F), 21 (SW E)		Analog switch., Switch resistance ≤ 500ohm Leakage current ≤ 1uA																					
24	CTL Head -	REC CTL ouput																					
25	CTL Head +	Output impedance ≤ 500ohm																					
27	CTL Amp Bias	Open loop gain ----- >																					
28	CTL Amp (-)	At the full feedback, no oscillation.																					
29	SW D	Output dynamic range : 0~5V																					
30	CTL Amp out	Output impedance ≤ 2kΩ																					
31	PCTL IN	Schmitt bias VTH: 4 point. Internal bias = about 2.5																					
32	CFG IN	Schmitt width = ±150mV. Built - in the frequency doubling block.																					

PIN DESCRIPTIONS (Continued)

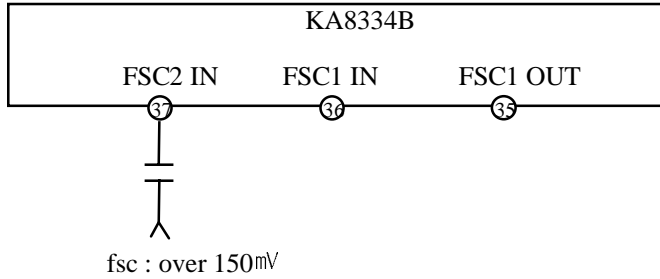
Pin No	Function	Descriptions	Input/Output form												
34	Duty I/O	2 value input/output, pull - up. note) Refer to ㉞ISS-VASS? <table border="1" style="margin-left: 20px;"> <tr> <td></td> <td>ASB Mark</td> <td>At Duty mode</td> <td>At VISS mode</td> </tr> <tr> <td>H</td> <td>No mark, Duty=60%</td> <td>Data=?? Duty=60%</td> <td>VISS undetection</td> </tr> <tr> <td>L</td> <td>Mark, Duty=70%</td> <td>Data=?? Duty=27%</td> <td>VISS detection</td> </tr> </table>		ASB Mark	At Duty mode	At VISS mode	H	No mark, Duty=60%	Data=?? Duty=60%	VISS undetection	L	Mark, Duty=70%	Data=?? Duty=27%	VISS detection	
	ASB Mark	At Duty mode	At VISS mode												
H	No mark, Duty=60%	Data=?? Duty=60%	VISS undetection												
L	Mark, Duty=70%	Data=?? Duty=27%	VISS detection												
35	FSC1 OUT	The internal OSC. block & the external OSC. block is selected by serial data. Built-in clock amp for int osc : gain > 20 dB The external OSC. block sensitivity ≥ 150mV.	—												
36	FSC1 IN														
37	FSC2 IN														
38	N.C	GND Connected.	—												
39	Power on reset	Connects the capacitor (0.047uF).	—												
40	REF 30	Servo reference signal													
41	VFF	Video head switching pulse													
42	AFF	Audio head switching pulse													
43	EFF	Extra head switching pulse													
45	HA-SLT	4-head amp select output	—												
44	VP	Quasi V-pulse 3 value output													
46	Composite Sync.	2 value input : Digital input At PB mode, synchronizes to internal reference, at REC, INST, ASB mode, separated and synchronizes to V sync.													
47	ENV-DET	2 value input Envelop detect input. note) Attention to 4-head logic timing													
48	SUB-H	2 value input 4-head changing logic support input.													
49	Serial Data	2 value input (schmitt) Pull-up resistor = 9 Kohm. Note) Refer to serial input													
50	Serial CLK	2 value input (Schmitt) Pull-up Resistor = 9 Kohm Note) Refer to serial input													

PIN DESCRIPTIONS

Pin No	Function	Descriptions	Input/Output form																																													
51 52 53	Mode D Output E F	<table border="1"> <thead> <tr> <th>BIT</th> <th>4</th> <th>3</th> <th>2</th> <th>1</th> <th>0</th> <th>D</th> <th>E</th> <th>F</th> </tr> </thead> <tbody> <tr> <td></td> <td>0</td> <td>1</td> <td>1</td> <td>1</td> <td>1</td> <td>CFG C/D</td> <td>CTL C/D</td> <td>-</td> </tr> <tr> <td></td> <td>1</td> <td>1</td> <td>1</td> <td>1</td> <td>1</td> <td>CFG</td> <td>CFG30, CTL</td> <td>-</td> </tr> <tr> <td></td> <td>0</td> <td>1</td> <td>1</td> <td>1</td> <td>1</td> <td>-</td> <td>-</td> <td>6.5H DET.</td> </tr> <tr> <td></td> <td>1</td> <td>1</td> <td>1</td> <td>1</td> <td>1</td> <td>-</td> <td>-</td> <td>CTL DET.</td> </tr> </tbody> </table> <p>CFG C/D: CFG count- downed signal output by search speed. CTL C/D: CTL count- downed signal output by search speed. CFG 30(REC) : At REC, the compared signal of CAPSTAN phase input The output of CFG count down 30 Hz (PAL:25Hz) CTL(PB) : At PB, CTL signal (squares) output.</p>	BIT	4	3	2	1	0	D	E	F		0	1	1	1	1	CFG C/D	CTL C/D	-		1	1	1	1	1	CFG	CFG30, CTL	-		0	1	1	1	1	-	-	6.5H DET.		1	1	1	1	1	-	-	CTL DET.	
BIT	4	3	2	1	0	D	E	F																																								
	0	1	1	1	1	CFG C/D	CTL C/D	-																																								
	1	1	1	1	1	CFG	CFG30, CTL	-																																								
	0	1	1	1	1	-	-	6.5H DET.																																								
	1	1	1	1	1	-	-	CTL DET.																																								
54	C - ROT	Color rotation output. note) Refer to ?-head rotation logic																																														
55 56 57	MODE C OUTPUT B A	<table border="1"> <thead> <tr> <th>BIT</th> <th>5</th> <th>4</th> <th>2</th> <th>1</th> <th>0</th> <th>A</th> <th>B</th> <th>C</th> </tr> </thead> <tbody> <tr> <td></td> <td>0</td> <td>0</td> <td>1</td> <td>1</td> <td>1</td> <td>SP</td> <td>SP</td> <td>LP</td> </tr> <tr> <td></td> <td>0</td> <td>1</td> <td>1</td> <td>1</td> <td>1</td> <td>SP</td> <td>EP</td> <td>LP</td> </tr> <tr> <td></td> <td>1</td> <td>0</td> <td>1</td> <td>1</td> <td>1</td> <td>CTL DELAY COUNTER</td> <td>H - OSC</td> <td>NOISE DET.</td> </tr> <tr> <td></td> <td>1</td> <td>1</td> <td>1</td> <td>1</td> <td>1</td> <td>CAP PD REF</td> <td>DRUM FG</td> <td>DRUM PG</td> </tr> </tbody> </table> <p>CTL DELAY COUNTER → Refer to TIME CHART H - OSC → Refer to H - OSC NOISE DET. → Refer to NOISE DET</p>	BIT	5	4	2	1	0	A	B	C		0	0	1	1	1	SP	SP	LP		0	1	1	1	1	SP	EP	LP		1	0	1	1	1	CTL DELAY COUNTER	H - OSC	NOISE DET.		1	1	1	1	1	CAP PD REF	DRUM FG	DRUM PG	
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59	PG M.M	Time constant: 0 - 60 ° DEG Non retriggerable note) refer to ?-Head SW timing?																																														
60	DRUM PG IN	Built-in input amp schmitt. Input resistor : 10kΩ. Feedback resistor: 100kΩ. note) Refer to Head switching timing?																																														

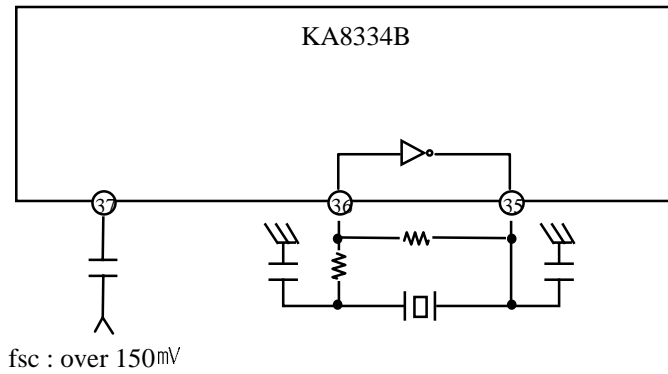
fsc INPUT CIRCUIT

(1) Case 1 : using single system clock



* Serial data selection : FSC2 → ON, FSC1 → OFF (cf. S-DATA table)

(2) Case 2 : using two kinds of system clock (multi-mode)



fsc : over 150mV

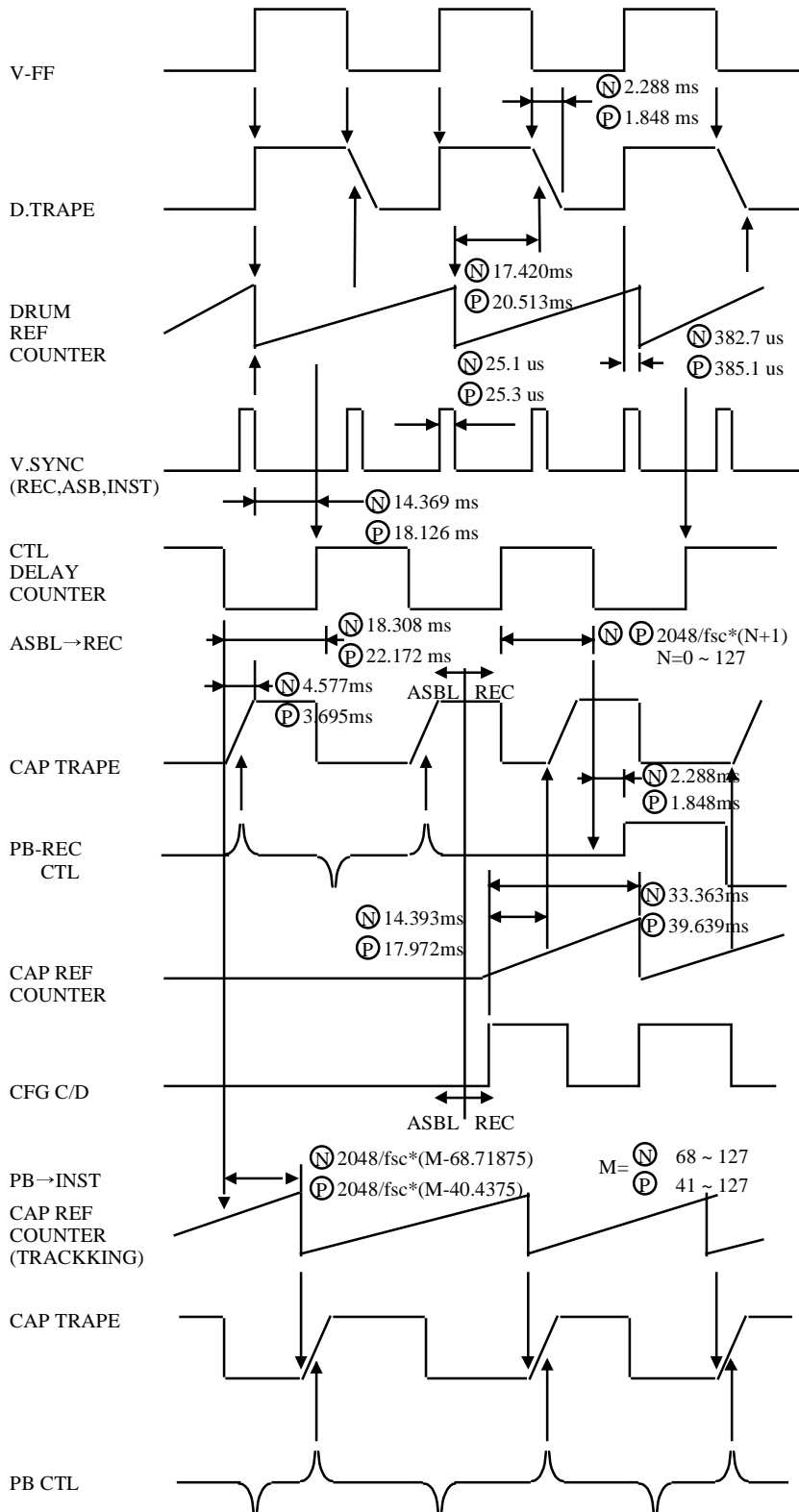
* Serial data selection : FSC1, FSC2

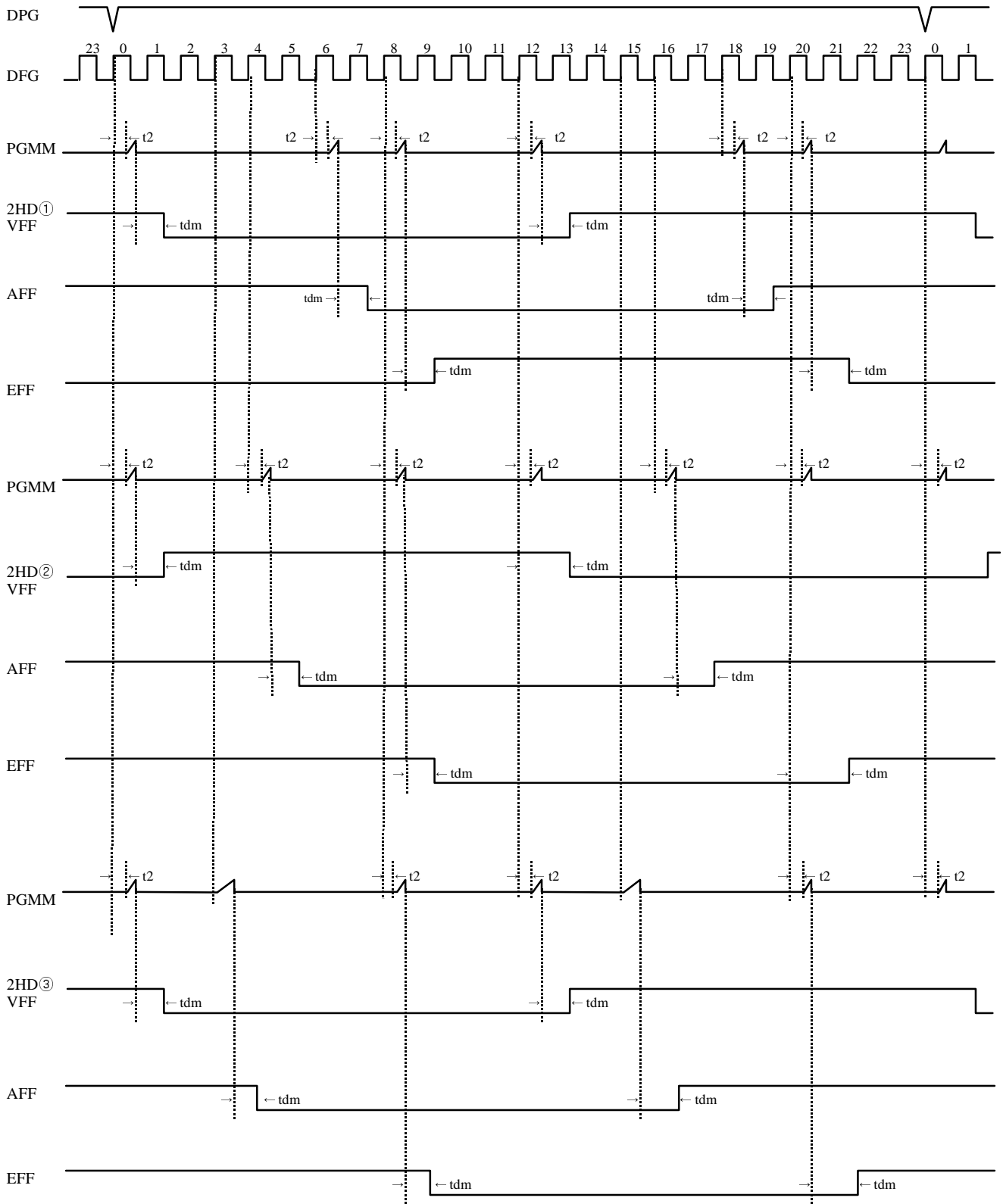
* Oscillation frequency minute adjust by C1, C2 (cf. X-tal electrical characteristics spec)

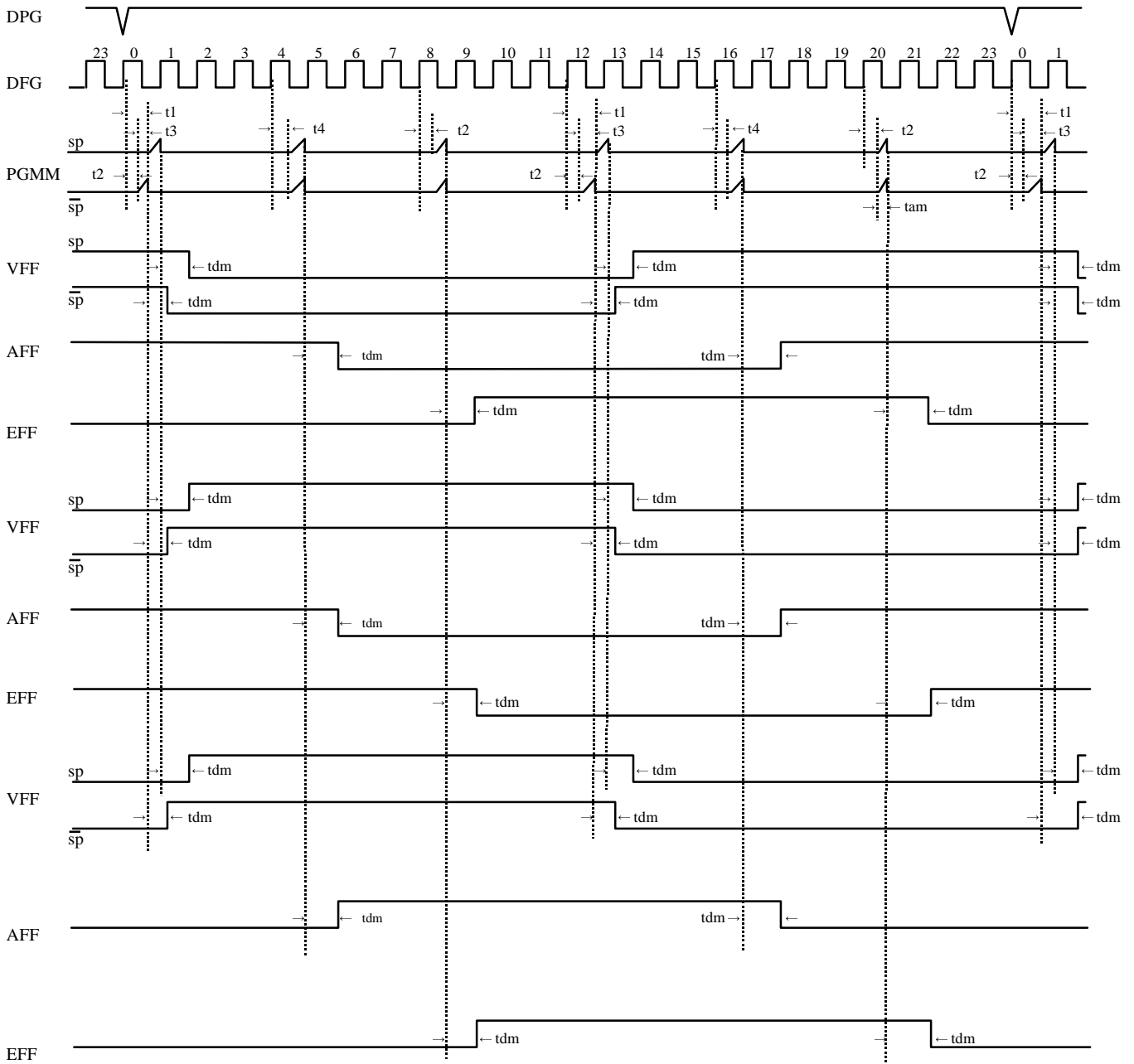
* Amplitude of oscillation frequency adjust by R1, R2

* In case of interference between FSC1 and FSC2, a resistor of several kΩ connection both between pin 37 and capacitor and between pin 36 and R1

TIMING CHART







	t1	t2	t3	t4
NTSC	402.29	277.13	125.16	339.71
PAL	461.93	332.01	129.92	389.80

$tdm = (N+1) * 32 / fsc$
 $N = 0 \sim 255$
 tam : Analog MM Delay Time

(Unit : μs)

FUNCTION GUIDE

1) The constant of DRUM speed block

	DEG freq.	S/H freq.	Counter clock	Counter bit number	FV-Gain	Drum PD ADJ.
NTSC	719.36Hz	719.36Hz	fsc / 2	11 BIT	60.75mV/%	596Hz ~ 906H
PAL	600.00Hz	600.00Hz	fsc / 3	11 BIT	60.13mV/%	496Hz ~ 758Hz

2) The constant of DRUM phase block

		S / W frequency	Counter clock	Counter bit number	Drum PD gain	
					KP 1	KP 2
NTSC	At phase DET	29.97 Hz	fsc / 4	11 BIT	1.092 V/ ms	3.277 V/ms
	At f _H COMP	3.93 KHz	fsc / 4	11 BIT	1.092 V/ ms	3.277 V/ms
PAL	At phase DET	25 Hz	fsc / 4	11 BIT	1.353 V/ ms	4.059 V/ms
	At f _H COMP	3.91 KHz	fsc / 4	11 BIT	1.353 V/ ms	4.059 V/ms

3) The constant of Capstan phase block

		S / W frequency	Counter clock	Counter bit number	Drum PD gain	
					KP 1	KP 2
				NORMAL	NORMAL	NORMAL
NTSC		29.97 Hz	fsc / 8	11 BIT	0.546	1.639
PAL	PB	25.00 Hz	fsc / 8	11 BIT	0.677	2.030
	REC	25.22 Hz				

4) Conversion of CAPSTAN gain

SWH	SWG	SWF	NTSC SP	NTSC LP(9H)	NTSC EP(12H)	PAL SP	PAL LP
OFF	OFF	OFF	SLOW	SLOW	SLOW	SLOW	SLOW
OFF	OFF	OFF	-	X1	X1, 2, 3	-	X1
ON	OFF	OFF	X1, 2	X2 ~ X5	X4 ~ X9	X1 ~ X2	X2 ~ X5
ON	ON	OFF	X3 ~ X8	X16 ~ X17	X10 ~ X27	X3 ~ X8	X6 ~ X17
ON	ON	ON	X9 ~	X18 ~	X28 ~	X9 ~	X18 ~

5) The constant of CAPSTAN speed block

				CFG freq.	S/H freq.	Counter clock	COUNT. BIT Numb	FV gain	
N T S C	Noraml & Search		SP	Refer to apstan F/V frequency	2157.8 Hz	fsc	11 BIT	40.50 mV/%	
			LP		1079.2 Hz	fsc / 2			
			EP		719.2 Hz	fsc / 3			
			9H		479.5 Hz	fsc / 4	11 BIT		45.56 mV/%
			12H		359.6 Hz	fsc / 6	11 BIT		40.50 mV/%
	SLOW	SLOW A	SP	809.1 Hz	1618.2 Hz	fsc	11 BIT	54.0 mV/%	
			LP	404.6 Hz	809.2 Hz	fsc / 2			
			EP	269.7 Hz	539.4 Hz	fsc / 3			
			9H	179.85 Hz	359.7 Hz	fsc / 4	11 BIT		60.74 mV/%
			12H	134.85 Hz	269.7 Hz	fsc / 6	11 BIT		54.0 mV/%
		SLOW B	SP	581.7 Hz	1163.4 Hz	fsc	11 BIT	54.0 mV/%	
			LP	404.6 Hz	809.2 Hz	fsc / 2			
			EP	269.7 Hz	539.4 Hz	fsc / 3			
			9H	179.85 Hz	359.7 Hz	fsc / 4	11 BIT		60.74 mV/%
12H			134.85 Hz	269.7 Hz	fsc / 6	11 BIT	54.0 mV/%		
P A L	Noraml	NORMAL	SP	Refer to apstan F/V C frequency	1513.4 Hz	fsc / 2	11 BIT	35.76 mV/%	
			LP		756.7 Hz	fsc / 4			
	SLOW	SLOW A	SP	567.5 Hz	1135.5 Hz	fsc / 2	11 BIT	47.68 mV/%	
			LP	283.7 Hz	567.5 Hz	fsc / 4			
		SLOW B	SP	378.4 Hz	756.7 Hz	fsc / 2	11 BIT	71.52 mV/%	
			LP	283.7 Hz	567.5 Hz	fsc / 4		47.68 mV/%	

6) Conversion of CTL schmitt VTH

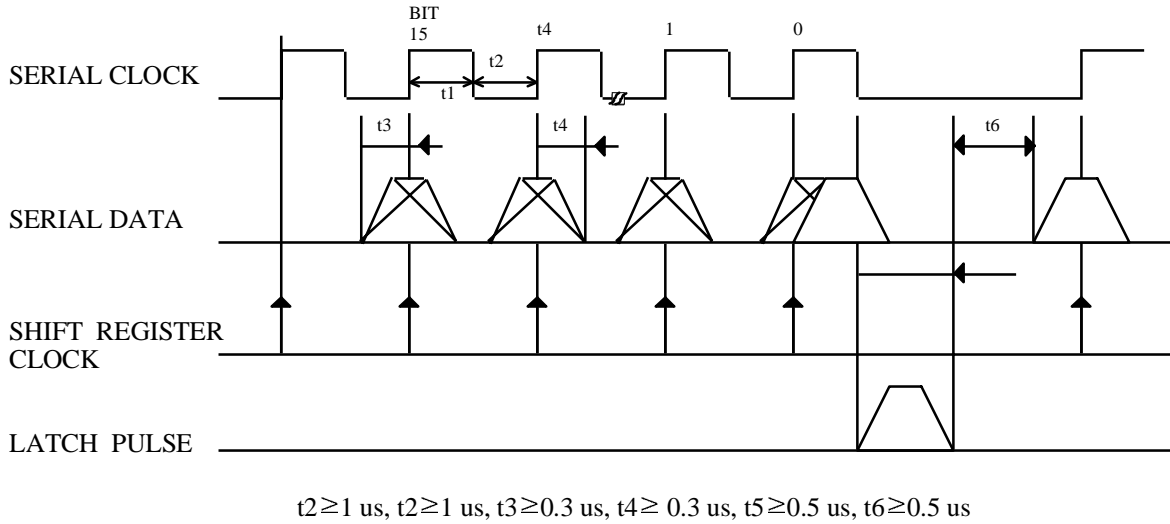
VTH	NTSC SP	NTSC LP(9H)	NTSC EP(12H)	PAL SP	PAL LP
±150 mV	-	SLOW	SLOW	SLOW	SLOW
±30 mV		X1	X1		
±300 mV	SLOW X1, 2	X2, 3, 4, 5	X2, 3, 4, 7	X1, 2	X2, 3, 4, 5
±60 mV					
±600 mV	X3, 4, 5, 7, 8,	X7, 9, 13, 15,	X9, 10, 13, 15	X3, 4, 5, 7, 8,	X7, 9, 13, 15,
±80 mV	9,11, 12,13, 14, 15, 21	17, 21,22, 24, 26	17, 21, 27, 33 35, 39	9,11, 12,13, 14, 15, 21	17, 21,22, 24, 26
±1000 mV	At fixed C.P / D output				
+100mV					



7) Capstan FV center frequency (KHz)

Serial Bit	Forward					Reverse				
	NTSC			PAL		NTSC			PAL	
11 10 9 8	SP	LP	EP	SP	LP	SP	LP	EP	SP	LP
0 0 0 0	1.079	0.539	0.360	0.757	0.378	1.079	0.539	0.360	0.757	0.378
0 0 0 1	2.158	1.079	0.719	1.513	0.757	2.158	1.079	0.079	1.513	0.757
0 0 1 0	3.236	1.618	1.079	2.270	1.135	3.236	1.618	1.079	2.270	1.135
0 0 1 1	4.455	2.158	1.438	3.109	1.513	4.138	2.158	1.438	2.921	1.513
0 1 0 0	5.569	2.697	2.517	3.886	1.891	5.174	2.697	2.517	3.651	1.891
0 1 0 1	7.796	3.898	3.236	5.441	2.720	7.242	3.621	3.236	5.111	2.556
0 1 1 0	10.024	5.012	10.024	6.996	3.498	9.312	4.655	9.312	6.572	3.286
0 1 1 1	20.852	23.169	3.712	14.488	16.098	17.977	19.975	3.449	12.765	14.183
1 0 0 0	12.743	12.743	12.743	8.854	8.854	10.986	10.986	10.986	7.801	7.801
1 0 0 1	24.326	13.901	13.515	16.903	9.659	20.975	11.985	11.652	14.893	8.510
1 0 1 0	15.060	15.060	15.060	10.464	10.464	12.984	12.984	12.984	9.219	9.219
1 0 1 1	21.010	18.535	4.826	15.293	12.878	18.976	15.980	4.483	13.474	11.346
1 1 0 0	17.376	8.353	5.569	12.074	5.830	14.981	7.759	5.173	10.637	5.494
1 1 0 1	19.693	16.218	7.796	13.683	11.269	16.978	13.983	7.242	12.056	9.928
1 1 1 0	SLOW									
1 1 1 1	Refer to ?Constant of CAPSTAN speed block									
Capstan	NTSC					PAL				
PD	Capstan F / V frequency를 about					Capstan F / V frequency를 about				
ADJ	- 7.2% ~ + 8.4%					- 8.0% ~ + 9.6%				

Serial Input Timing Chart



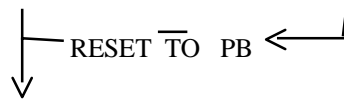
- ① When Serial data is $\bar{0}$ at serial clock negative edge.
Latch pulse in LSI is then generated and the previous 16-bit data is effective.
- ② T_6 is the time when serial data after data latch and clock are both $\bar{0}$ and absolutely specified at over 500ns.
- ③ Serial input is pulled-up of about $10^4 \Omega$. Care should be taken of the time delay of waveform. External pull-up presister is required at higher speed.

Serial Data Input Register

BIT



VISS, VASS	F/R	PB SPEED SECTOR	f _H COMP	PB, REC INST, ASBL	CAP STOP	DRUM STOP	SP/LP/EP	Address = 0
------------	-----	-----------------	---------------------	--------------------	----------	-----------	----------	-------------



VP ON/OFF	SHIFT SITE	SHIFT CH SECTOR	VP SHIFT AMOUNT	VP POSITION DATA	1	0	1
-----------	------------	-----------------	-----------------	------------------	---	---	---

VFF SEL.	REC CTL DELAY DATA (X VALUE)	NTSC /PAL	FSC SEL.	VP SEL.	REF. SEL.	SLOW A/B	0	1	1
----------	--------------------------------	-----------	----------	---------	-----------	----------	---	---	---

PB TRACKING DATA	C PD FIX.	D PD FIX.	MODE OUTPUT SEL.	1	1	1
------------------	-----------	-----------	------------------	---	---	---

HEAD SWITCHING PULSE DELAY DATA	SW E CTL.	SW D CTL.	TIME MODE	WA1 MODE	WA2 MODE	1	1	0
---------------------------------	-----------	-----------	-----------	----------	----------	---	---	---

address

- ① The Servo IC includes a register for the previous 79-bit serial data
The tail end bits (Bit 2-0, or only 0 Bit) are addressed at each register row address and the previous bit becomes input data of register of the address.
- ② All bits of registers are reset during power on.
On preset mode, all bits except for bits selecting PB in mode are 0.
- ③ Each register is automatically reset when the registers of PB speed, f_H compensation, V_H control are implemented into all modes but PB.



10) SERIAL DATA TABLE 1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
													0	0	0	SP
													0	1	0	LP(9H MODE)
													1	0	0	EP(12H MODE)
												0			0	DRUM STOP & CAP P/D FIX
												1			0	DRUM ON
											0				0	CAPSTN STOP
											1				0	CAPSTN ON
									0	0					0	REC
									0	1					0	ASBL
									1	0					0	INST
									1	1					0	PB
								0	1	1					0	NOR
								1	1	1					0	fH compensation on
0	0	0													0	DUTY DET. MODE
0	0	1													0	DUTY DET. MODE VISS REC FF RESET
0	1	0													0	VISS MODE
0	1	1													0	VISS MODE, VISS REC FF RESET
1	0	0													0	VISS MODE, VISS DET FF RESET
1	0	1													0	VISS MODE, VISS DET FF RESET VISS REC FF RESET
1	1	0													0	VISS MODE, VISS WRITE
1	1	1													0	WRITE MODE, VISS REC FF RESET

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	NTSC			PAL	
																SP	LP (9H)	EP (12H)	SP	LP
				0	0	0	0		1	1					0	X1	X1	X1	X1	X1
				0	0	0	1		1	1					0	2	2	2	2	2
				0	0	1	0		1	1					0	3	3	3	3	3
				0	0	1	1		1	1					0	4	4	4	4	4
				0	1	0	0		1	1					0	5	5	7	5	5
				0	1	0	1		1	1					0	7	7	9	7	7
				0	1	1	0		1	1					0	9	9	27	9	9
				0	1	1	1		1	1					0	18	40	10	18	40
				1	0	0	0		1	1					0	11	22	33	11	22
				1	0	0	1		1	1					0	21	24	35	21	24
				1	0	1	0		1	1					0	13	26	39	13	26
				1	0	1	1		1	1					0	19	32	13	19	32
				1	1	0	0		1	1					0	15	15	15	15	15
				1	1	0	1		1	1					0	17	28	21	17	28
				1	1	1	0		1	1					0	SLOW① CAP P/D FIX				
				1	1	1	1		1	1					0	SLOW② CAP P/D FIX, DRUM P/D FIX				
		0													0	FWD				
		1													0	REV				

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
											0	0	1	1	0	WIDE ASPECT NORMAL MODE	
											0	1	1	1	0	WIDE ASPECT NORMAL MODE	
											1	0	1	1	0	WIDE ASPECT 1 ON MODE	
											1	1	1	1	0	WIDE ASPECT 2 ON MODE	
										0			1	1	0	9H, 12H MODE OFF	
										1			1	1	0	9H, 12H MODE ON	
									0				1	1	0	SW D OFF	
									1				1	1	0	SW D ON	
								0					1	1	0	SW E OFF	
								1					1	1	0	SW E ON	
MSB				LSB													
*	*	*	*	*	*	*	*							1	1	0	HEAD SW PULSE DELAY DATA

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
	MSB						LSB										
	*	*	*	*	*	*	*						1	1	1	PB. TRACKING DATA	
																(Mode output CTL)	
																A B C D E	
												0	1	1	1	CFG C/D CTL C/D	
												1	1	1	1	CFG CFG30 (REC)	
																A B C F	
									0	0			1	1	1	SP SP LP 6.5H DET	
									0	1			1	1	1	SP EP LP CTL missing	
									1	0			1	1	1	CTL DELAY COUNTER H-OSC NOISE DET. V SYNC (SYNC. separated)	
									1	1			1	1	1	CAP PD Rf DRUM FG DRUM PG missing CTL signal DET	
								0					1	1	1	C. PD output normal operation P.CTL schmitt 3 value selection	
								1					1	1	1	FIXED C.PD OUTPUT P. CTL schmitt width = ±1000mV	
									0				1	1	1	D.PD output: Normal	
									1				1	1	1	Fixed D.PD output	

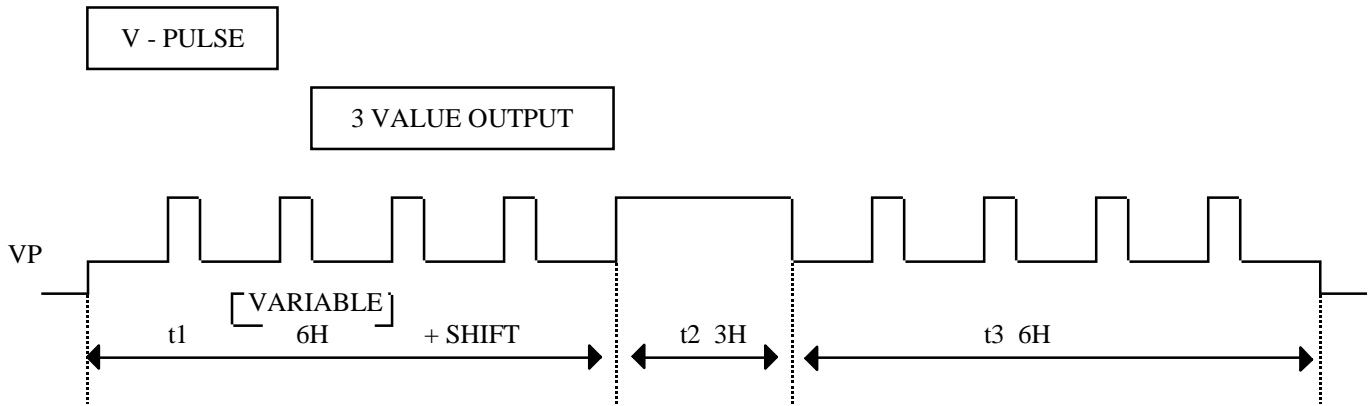
11) SERIAL DATA TABLE 2

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
								MSB				LSB					
								*	*	*	*	*	1	0	1	VP POSITION DATA	
					0	0	0						1	0	1	VP SHIFT 0.0H	
					0	0	1						1	0	1	VP SHIFT 0.5H	
					0	1	0						1	0	1	VP SHIFT 1.0H	
					0	1	1						1	0	1	VP SHIFT 1.5H	
					1	0	0						1	0	1	VP SHIFT 2.0H	
					1	0	1						1	0	1	VP SHIFT 2.5H	
																CH-1 CH-2	
			0	0									1	0	1	VP SHIFT SEL FIX.ED FIX.ED	
			0	1									1	0	1	VP SHIFT SEL FIX.ED SHIFT	
			1	0									1	0	1	VP SHIFT SEL SHIFT FIX.ED	
			1	1									1	0	1	VP SHIFT SEL SHIFT SHIFT	
		0											1	0	1	VP SHIFT Direction (+)	
		1											1	0	1	VP SHIFT Direction (-)	
0	0												1	0	1	VP OFF (L LEVEL OUTPUT)	
0	1												1	0	1	VP 3 VALUE (M LEVEL OUTPUT)	
1	0												1	0	1	VP ON (3 VALUE OUTPUT)	
1	1												1	0	1	VP MONITOR CUT(H LEVEL OUT.)	

12) SERIAL DATA TABLE 3

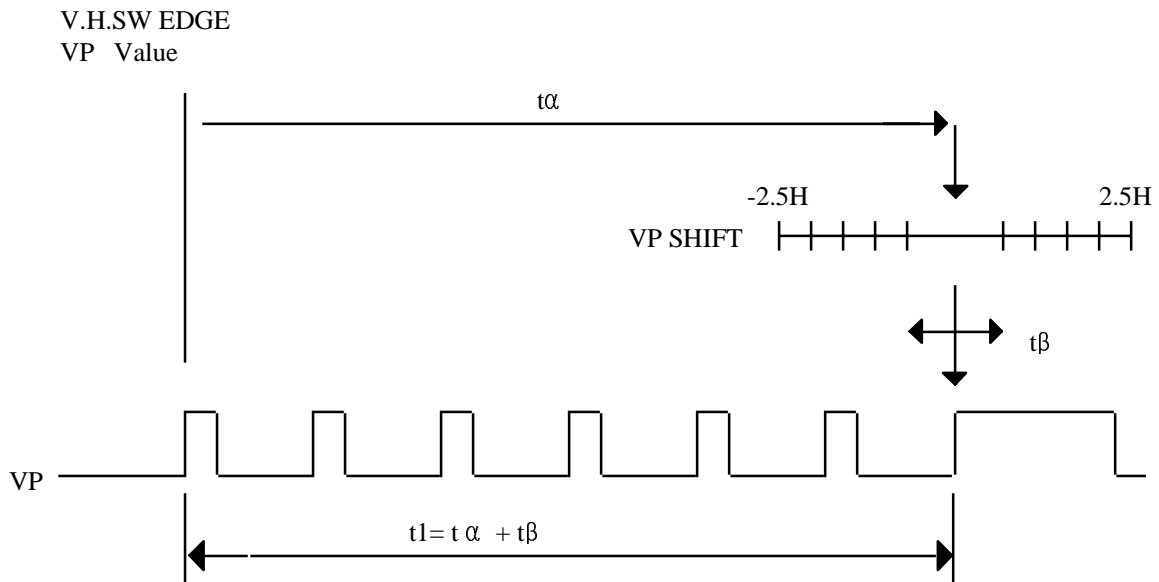
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0			
	MSB					LSB												
	*	*	*	*	*	*	*						0	1	1	REC CTL DELAY DATA (X VALUE COMPENSATION)		
											0		0	1	1	REF SEL NOR		
											1		0	1	1	REF SEL FILD DET		
										0			0	1	1	VP SEL NOR		
										1			0	1	1	VP SEL + 6H		
									0				0	1	1	CLOCK SEL(fsc1:ON, fsc2:OFF)		
									1				0	1	1	CLOCK SEL(fsc1:OFF,fsc2:ON)		
												0	0	1	1	SLOW A		
												1	0	1	1	SLOW B		
								0					0	1	1	PAL		
								1					0	1	1	NTSC		
																	CH1	CH2
0													0	1	1	VFF	SHIFT	SHIFT
1													0	1	1	VFF	FIXED	SHIFT
												0	0	0	1	TEST MODE		

13) V - PULSE



V.Head Switching Pulse Edge

- The output is through PB * VP ON
- Refer to t1 variation? $\frac{1}{2}HIFT$
- When t3 is specified as $Vp+6H$, it is output and when not fixed, t3 will be $\frac{1}{2}$



t α	VP Value
------------	----------

At Slow & X2 Mode, the above channel is variable.
 At the other mode, CH1 & CH2 are simultaneously fixed.

MODE		CH - 1	CH - 2
2 HEAD		FIXED	SHIFT
DA - 4	SP	FIXED	SHIFT
	SP	SHIFT	FIXED

Shift Quantity (By serial data 5 bit = N)

NTSC	64 (41.5-N) / fsc	about 3.0H ~ 11.7H
PAL	64 (43.75-N) / fsc	about 2.9H ~ 9.9H

Fix Quanty = About 6.0H

t β	VP SHIFT
-----------	----------

By serial data, the quantity of VP shift, shift channel and shift direction is varied as follows :

VP Shift Quantity

BIT	13	12	11	10	9	8		3	2	1	Shift Quantity
				0	0	0					0.0 H
				0	0	1					0.5 H
				0	1	0					1.0 H
	-	-	-	0	1	1		1	0	1	1.5 H
				1	0	0					2.0 H
				1	0	1					2.5 H

VP Shift Channel & Shift Direction (?+ ? is delayed direction)

BIT	13	12	11	10	9	8		3	2	1	CH -1	CH -2
	0	0	0	-							FIXED	FIXED
	1											
	0	0	1	-				1	0	1	FIXED	+ SHIFT
	1	0	1	-							FIXED	- SHIFT
	0	1	0	-							+ SHIFT	FIXED
	1	1	0	-							- SHIFT	FIXED
	0	1	1	-							- SHIFT	+ SHIFT
	1	1	1	-							+ SHIFT	- SHIFT

14 - 1) VISS / VASS / ASB MARK.

SERIAL			MODE	REC	ASB	PB / INST	
15	14	13					
1	1	1	VASS	ASB MARK RECORD	ASB MARK DETECT	VASS DATA WRITE	
0	0	0		According to Duty I/O input		VASS record	VASS DATA 1BIT DET. OUTPUT TO DUTY I/O
0	0	1					
0	1	0	VISS	NO ACTION	VISS CODE DETECT	VISS CODE DETECT	
0	1	1		According to Duty I/O input	Latch VISS code output Distinguish between F/F and VISS code		
1	0	0		VASS record	F/F reset		
1	0	1					
1	1	0		VISS CODE WRITE (AUTO)	VISS CODE REWRITE (AUTO)		

14 - 2) VISS / VASS / ASB MARK RECORD.

Wide Aspect	OPERATION	DUTY I/O	CTL DUTY(%)	Remark
NORMAL	ASB MARK RECORD	H (IN)	62.5	-
		L (IN)	70.0	ASB MARK
	VASS DATA RECORD	H (IN)	62.5	-
		L (IN)	30.0	-
	VISS CODE RECORD	H (OUT)	62.5	VISS CODE AUTO RECORD
		L (OUT)	30.0	
WIDE ASPECT 1	ASB MARK RECORD	H (IN)	57.5, 62.5	LLSS PATTERN RECORD
		L (IN)	70.0	ASB MARK
	VASS DATA RECORD	H (IN)	57.5, 62.5	LLSS PATTERN RECORD
		L (IN)	25.0, 30.0	
	VISS CODE RECORD	H (OUT)	57.5, 62.5	VISS CODE AUTO RECORD LLSS PATTERN RECORD
		L (OUT)	25.0, 30.0	

* Wide aspect 2 mode operation is same as that of wide aspect 1 mode, but the record pattern is ?LLLS?

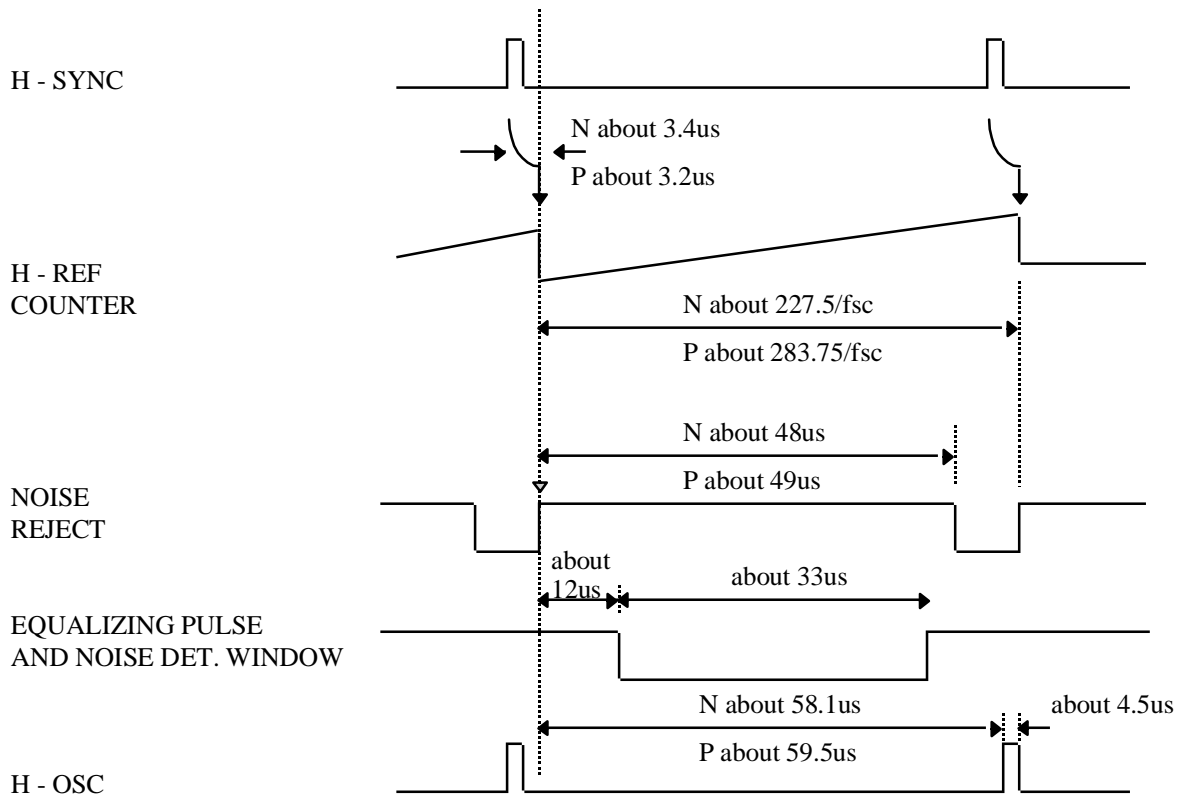
14-3) VISS/VASS/ASB MARK DETECT OPERATION

- Whenever the CTL signal of duty 66.7% over is inputted, the ASB mark is detected and $\overline{\text{ASB}}$ level is outputted to the DUTY I/O.
- Whenever the CTL signal of duty 40.0% below is inputted, the $\overline{\text{VISS DATA 1}}$ is detected and $\overline{\text{VISS DATA 1}}$ level is outputted to the DUTY I/O.
- Whenever the CTL signal of duty 40.0% below is inputted consecutively as much as over 32, $\overline{\text{VISS DATA 1}}$ level is outputted to the DUTY I/O.
- Otherwise $\overline{\text{VISS DATA 1}}$ level is outputted to the DUTY I/O.
- $\overline{\text{VISS DATA 1}}$ means 30.0% and 62.5% duty pulses, $\overline{\text{VISS DATA 2}}$ means 25.0% and 57.5% duty pulses.

15) The usage of C.SYNC

Internal REF synchronizing at PB, SYNC is separated and synchronized by V.SYNC at REC, ASB and INST mode.

16) H - OSC



- . H - OSC is output in quasi-V - PULSE and able to output through mode B output.
- . Even if external H - OSC is stable, there is the jitter of about fsc 1 clock.

17) NOISE DET. & FIELD DET.

REF SEL Mode	NOR PB	f_H Compensation on PB	REC ASBL INST
NOR	- Noise DET. - H - Sync DET.	- Noise DET. - H - Sync DET.	- Noise DET. - V - Sync DET.
FIELD DET.	- Field DET.	- Noise DET. - H - Sync DET.	- Field DET.

In the modes except the field Det. of the previous table, it detects noise in the composite Sync.
The detecting method is as follows :

① Noise Detection

It detects more amount of noise than specified between H sync.

② H - Sync Detection

It detects more jitter of H-sync than specified.

③ V - Sync Detection

It detects whether there is V-sync jitter or not.

If the noise detector is operated (that is, if noise is detected), the operations are as follows :

① High is output through mode C output

② It make the Sync reset from V-sync to REF 30 out of function.

③ It adjusts fH compensation error in fH compensation mode.

18) Operation of SW A ~ K (Refer to Block Diagram)

SW	Description						
A	At CTLP Amp operation <table style="display: inline-table; vertical-align: middle;"> <tr> <td style="font-size: 2em;">[</td> <td>A = OFF</td> </tr> <tr> <td></td> <td>B = ON</td> </tr> <tr> <td></td> <td>C = ON</td> </tr> </table>	[A = OFF		B = ON		C = ON
[A = OFF					
		B = ON					
	C = ON						
B	At CTLP recording <table style="display: inline-table; vertical-align: middle;"> <tr> <td style="font-size: 2em;">[</td> <td>A = ON</td> </tr> <tr> <td></td> <td>B = OFF</td> </tr> <tr> <td></td> <td>C = OFF</td> </tr> </table>	[A = ON		B = OFF		C = OFF
[A = ON					
	B = OFF						
	C = OFF						
C							
D	ON/ OFF is controlled by S-DATA						
E	ON/ OFF is controlled by S-DATA. But, auto ON at slow						
F	Capstan loop gain selection mode SW (Refer to capstan gain selection)						
G							
H							
I	After the fH compensation mode off, it lasts on-stage about 70 ~ 100ms. After the power on reset, on time has 40 ~ 120mS. (But, a 0.047 μ F capacitor should be connected between pin 39 and GND)						
J	At fH compention Mode = ON						
K	At Drum PD ADJ = ON. ON/ OFF is controlled by S-DATA						
L							
M	After the power on reset, on time has 40 ~ 120mS. (But, a 0.047 μ F capacitor should be connected between pin 39 and GND)						

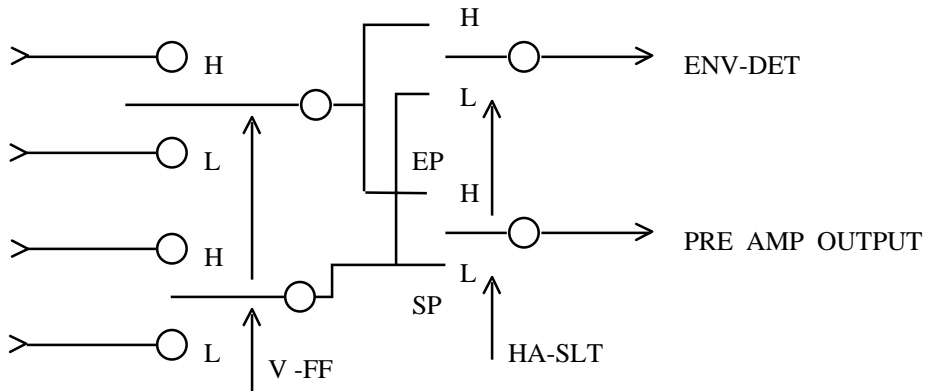


19) 4-Head Selection Logic

MODE		SUB - HL	HA - SLT	C - ROT	REMARK	
DA 4HD	SP	X1	0	0	V - FF	
		X2, SLOW	0	$\overline{V - FF}$	1	
		SEARCH	0	ENV - DET	ENV - DET \oplus V - FF	FSC2 selection
		SEARCH	0	0	V - FF	FSC1 selection
		-	1	ENV - DET	ENV - DET \oplus V - FF	
	EP LP	X1	0	1	$\overline{V - FF}$	
		X2, SLOW	0	V - FF	0	
		SEARCH	0	1	$\overline{V - FF}$	
		SLOW	1	1	$\overline{V - FF}$	
		OUTSIDE OF SLOW	1	1	$\overline{V - FF}$	NTSC
2HD		0	1	V - FF		
		1	1	$\overline{V - FF}$		

* Slow means that operate FORWARD SLOW

※ PRE AMP BLOCK OF KA8334B 4HD SELECTION LOGIC

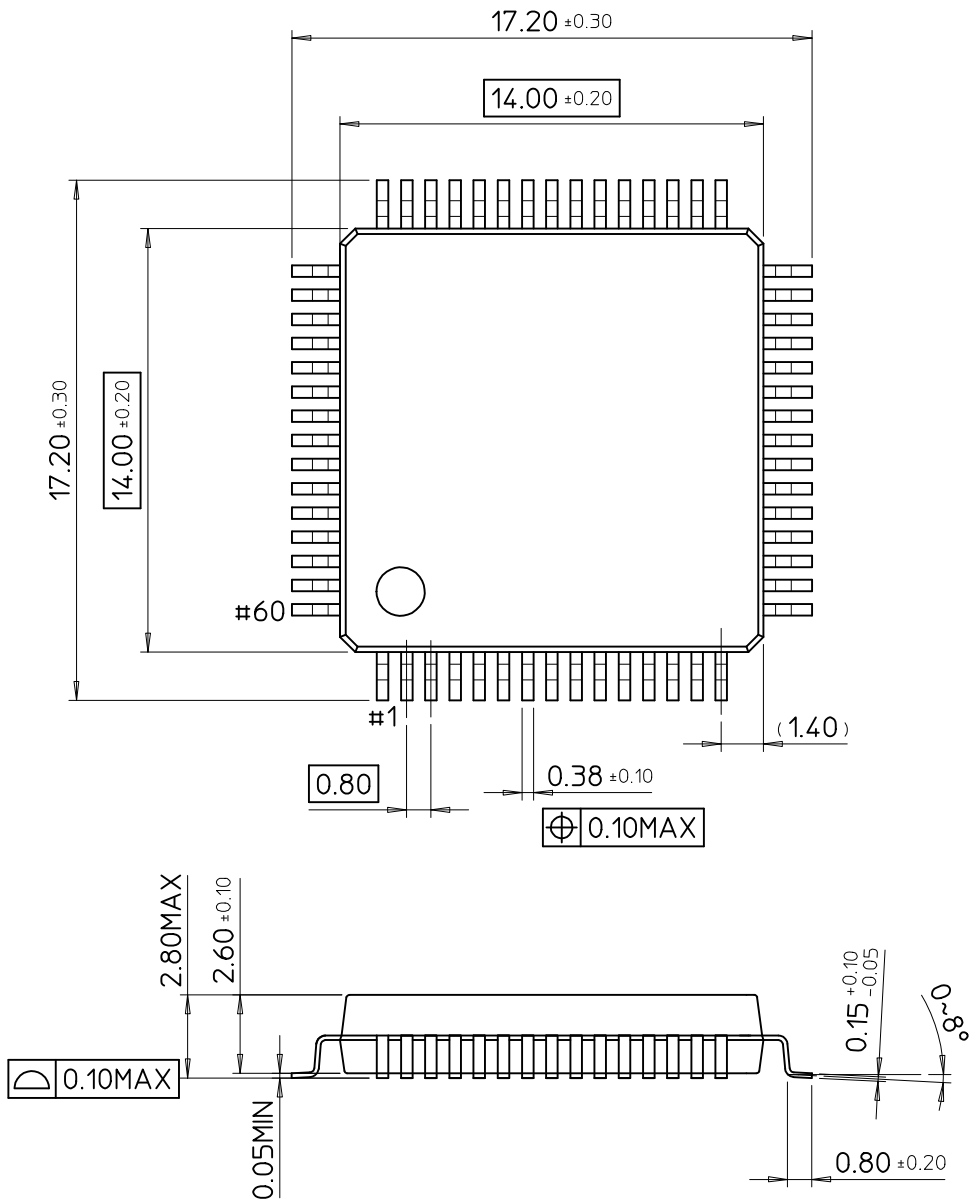


CAP CENTER FREQUENCY OF 9H, 12H MODE

SERIAL BIT	FORWARD		REVERSE	
	NTSC		NTSC	
11 10 9 8	9H MODE	12H MODE	9H MODE	12H MODE
0 0 0 0	0.240	0.180	0.240	0.180
0 0 0 1	0.480	0.360	0.480	0.360
0 0 1 0	0.720	0.540	0.720	0.540
0 0 1 1	0.960	0.720	0.960	0.720
0 1 0 0	1.200	1.260	1.200	1.260
0 1 0 1	1.680	1.620	1.680	1.620
0 1 1 0	2.160	5.012	2.160	4.656
0 1 1 1	5.040	1.856	5.040	1.725
1 0 0 0	5.280	6.371	5.280	5.493
1 0 0 1	5.760	6.758	5.760	5.826
1 0 1 0	6.240	7.530	6.240	6.492
1 0 1 1	3.120	2.413	3.120	2.242
1 1 0 0	3.600	2.785	3.600	2.587
1 1 0 1	4.080	3.898	4.080	3.621
1 1 1 0	SLOW			
1 1 1 1	REFER TO CAPSTAN SPEED CONSTANT			
CAPSTAN PD ADJ	About 7.2% ~ 8.4% of the above frequency			

60-QFP-1414A

Dimensions in Millimeters



SAMSUNG ELECTRONICS CO.,LTD.