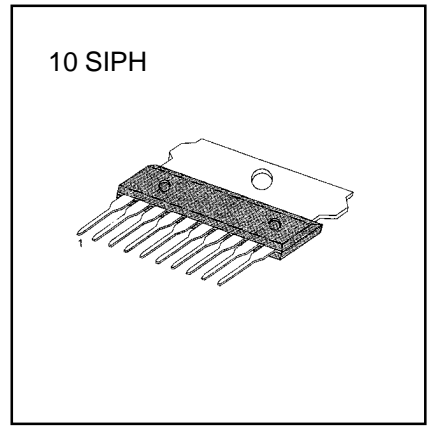


FIXED MULTI-OUTPUT REGULATOR

The KA7630/1 is a multi-output positive voltage regulator designed to provide fixed precision output voltages of 5.1V, 8V (7630) / 9V (7631) at current up to 0.5A and 12V at current up to 1A with external PNP transistor. An internal reset circuit generates a reset pulse when the output 1 decrease below the regulated value.

Output 2 & 3 can be disabled by TTL input. Protection features include over voltage protection, short circuit protection and thermal shut down.



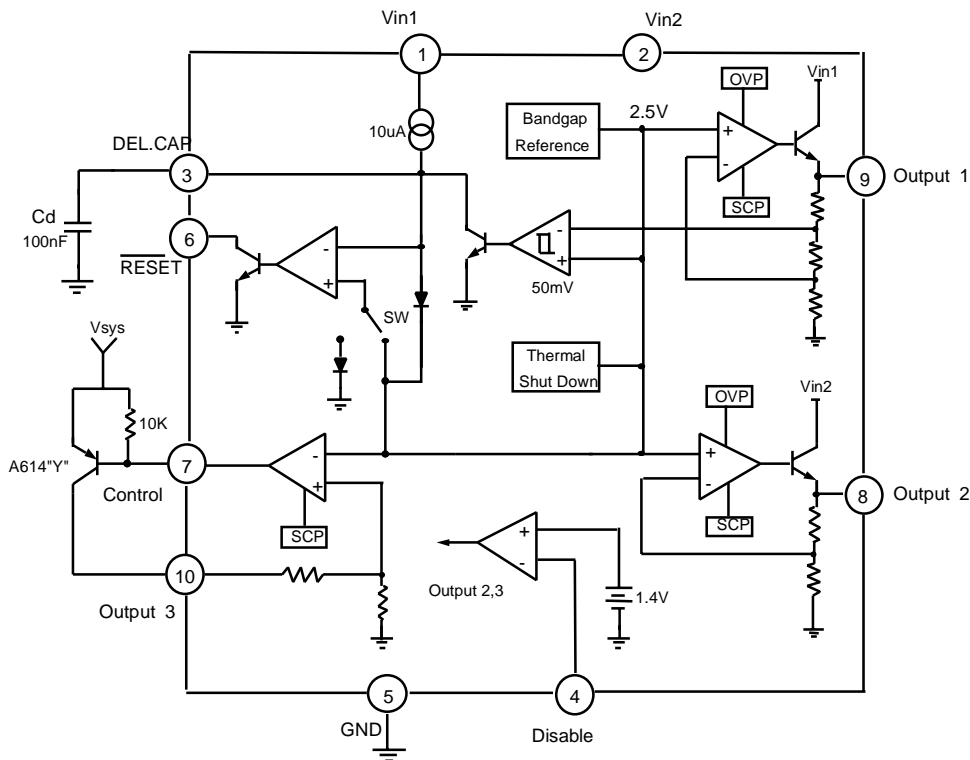
FEATURES

- Output Currents up to 0.5A (output 1 & 2)
- Output Current up to 1A with External Transistor (output 3)
- Fixed Precision Output 1 voltage $5.1V \pm 2\%$
- Fixed Precision Output 2 voltage $8V \pm 2\%$ (KA7630)
- Fixed Precision Output 2 voltage $9V \pm 2\%$ (KA7631)
- Control Signal Generator for Output 3 voltage ($12V \pm 2\%$)
- Reset Facility for Output Voltage 1
- Output 2,3 with Disable by TTL Input
- Current Limit Protection at Each Output
- Thermal Shut Down

ORDERING INFORMATION

Device	Package	Operating Temperature
KA7630/1	10 SIPH	0 ~ 125°C

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Ta = 25 °C)

Characteristics	Symbol	Value	Unit	Remark
DC Input Voltage	Vin	20	V	-
Disable Input Voltage	Vc	20	V	-
Output Current	Io	0.5	A	-
Power Dissipation	Pd	1.5	W	No Heat sink
Junction Temperature	Tj	150	°C	-
Operating Temperature	Topr	0 ~ 125	°C	-

KA7630, ELECTRICAL CHARACTERISTICS

(Refer to test circuit Vin1=7.5V , Vin2=10.5V , Tj=25°C unless otherwise specified)

Characteristics	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage 1	Vo1	Io1=10mA 7.5V < Vin1 < 14V 5mA < Io1 < 500mA	5 4.9	5.1 5.1	5.2 5.3	V
Output Voltage 2	Vo2	Io2 = 10mA 10.5V < Vin2 < 18V 5mA < Io2 < 500mA	7.84 7.7	8 8	8.16 8.3	V
Dropout Output Voltage 1,2	Vd1,2	Io1,2=500mA			2.5	V
Line Regulation 1,2	Δ Vo1,2	7.5V < Vin1 < 14V 10.5V < Vin2 < 18V Io1,2 = 200mA			50 80	mV
Load Regulation 1,2	Δ Vo1,2	5mA < Io1 < 500mA 5mA < Io2 < 500mA			100 160	mV
Output Voltage 3	Vo3	Vsys =13V, Io3 =100mA	11.7	12	12.3	V
Line Regulation 3	Δ Vo3	13V < Vin2 < 18V, Io3 =100mA			120	mV
Load Regulation 3	Δ Vo3	5mA < Io3 < 1A			250	mV

KA7630, ELECTRICAL CHARACTERISTICS

(Refer to test circuit $V_{in1}=7.5V$, $V_{in2}=10.5V$, $T_j=25^\circ C$ unless otherwise specified)

Characteristics	Symbol	Test Conditions	Min	Typ	Max	Unit
Reset Pulse Delay	Trd	Cd = 100nF, Note1		25		ms
Saturation Voltage in Reset Condition	VrL	I6 = 5mA			0.4	V
Leakage Current at Pin 6	IrH	V6 = 10V			10	μA
Output Voltage Thermal Drift	STt	$0^\circ C \leq T_j \leq 125^\circ C$, Note 2		100		ppm/ $^\circ C$
Short Circuit Output Current	Isc1,2	$V_{in1}=7.5V$, $V_{in2} =10.5V$			1.6	A
Disable Voltage High	VdisH	Output 2 Active	2			V
Disable Voltage Low	VdisL	Output 2 Disabled			0.8	V
Disable Bias Current	Idis	$0V < V_{dis} < 7V$	-100		2	μA
Junction Temperature for TSD	Ttsd	Note 2		145		$^\circ C$
Quiescent Current	Iq	Io1=10mA, Output2 Disabled			2	mA
Reset Threshold Voltage	Vr	K=Vo1	K-0.4	K-0.25	K-0.1	V
Reset Threshold Hysteresis	Vrth	Note 1	20	50	100	mV

Note 1. To check the reset circuit ,the reset output is low to discharge the delay capacitor(=Cd). if it's less than $V_{o1}-0.25V$. And the reset output is high when the delay capacitor voltage linearly increased by the interal current source($10\mu A$) if it's more than $V_{o1}-0.2V$. The equations of delay time is same as below.

$$Trd = (Cd \times 2.5) / 10\mu A$$

2. These parameters, although guaranteed, are not 100% tested in production.

KA7631, ELECTRICAL CHARACTERISTICS

(Refer to test circuit $V_{in1}=7.5V$, $V_{in2}=11.5V$, $T_j=25^\circ C$ unless otherwise specified)

Characteristics	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage 1	V_{o1}	$I_{o1}=10mA$ $7.5V < V_{in1} < 14V$ $5mA < I_{o1} < 500mA$	5 4.9	5.1 5.1	5.2 5.3	V
Output Voltage 2	V_{o2}	$I_{o2} = 10mA$ $11.5V < V_{in2} < 18V$ $5mA < I_{o2} < 500mA$	8.82 8.65	9 9	9.18 9.35	V
Dropout Output Voltage 1,2	$V_{d1,2}$	$I_{o1,2}=500mA$			2.5	V
Line Regulation 1,2	$\Delta V_{o1,2}$	$7.5V < V_{in1} < 14V$ $11.5V < V_{in2} < 18V$ $I_{o1,2}=200mA$			50 80	mV
Load Regulation 1,2	$\Delta V_{o1,2}$	$5mA < I_{o1} < 500mA$ $5mA < I_{o2} < 500mA$			100 160	mV
Output Voltage 3	V_{o3}	$V_{sys} = 13V$, $I_{o3} = 100mA$	11.7	12	12.3	V
Line Regulation 3	ΔV_{o3}	$13V < V_{in2} < 18V$, $I_{o3} = 100mA$			120	mV
Load Regulation 3	ΔV_{o3}	$5mA < I_{o3} < 1A$			250	mV
Reset Pulse Delay	Trd	$C_d=100nF$, Note1		25		ms
Saturation Voltage in Reset Condition	V_{rL}	$I_6 = 5mA$			0.4	V
Leakage Current at Pin 6	I_{rH}	$V_6 = 10V$			10	μA
Output Voltage Thermal Drift	STt	$0^\circ C \leq T_j \leq 125^\circ C$, Note 2		100		ppm/ $^\circ C$
Short Circuit Output Current	$I_{sc1,2}$	$V_{in1}=7.5V$, $V_{in2} = 11.5V$			1.6	A

KA7631, ELECTRICAL CHARACTERISTICS(Refer to test circuit $V_{in1}=7.5V$, $V_{in2}=11.5V$, $T_j=25^{\circ}C$ unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Disable Voltage High	VdisH	Output 2 Active	2			V
Disable Voltage Low	VdisL	Output 2 Disabled			0.8	V
Disable Bias Current	Idis	$0V < V_{dis} < 7V$	-100		2	μA
Junction Temperature for TSD	Ttsd	Note 2		145		$^{\circ}C$
Quiescent Current	Iq	$I_{o1}=10mA$, Output2 Disabled			2	mA
Reset Threshold Voltage	Vr	$K=V_{o1}$	K-0.4	K-0.25	K-0.1	V
Reset Threshold Hysteresis	Vrth	Note 1	20	50	100	mV

Note 1. To check the reset circuit , the reset output is low to discharge the delay capacitor(=Cd) if it is less than $V_{o1}-0.25V$. And the reset output is high when the delay capacitor voltage linearly increased by the intercurrent source($10\mu A$) if it is more than $V_{o1}-0.2V$.

The equations of delay time is same as below.

$$Trd = (Cd \times 2.5) / 10\mu A$$

2. These parameters, although guaranteed, are not 100% tested in production.

10-SIPH-A

