ENERAL INTRODUCTION

The KA7531/D is a complete solution for a dimming controller, high power factor, high efficiency electronic ballast. Contained in the KA7531/D are controllers for “boost” type power factor correction as well as for a dimming ballast. The Power factor circuit uses the peak current sensing method with a current fed multiplier and over-voltage protection. This system produces power factors of better than 0.99 with low input current THD at > 95% efficiency. Special care has been taken in the 0.1 design of the KA7531/D to increase system noise immunity by using a high a 0.2 mplitude oscillator, and a current fed multiplier. An over-voltage protection 0.3 comparator stops the PFC section in the event of sudden load decrease. The ballast section provides for programmable starting scenarios with programmable preheat and lamp out-of-socket interrupt times. The IC controls lamp output through frequency modulation using lamp current feedback.

The KA7531/D is designed using Samsung Elec.’s Semi-Standard tile array methodology. Customized versions of this IC, optimized to specific ballast architectures can be made available. Contact Samsung Elec. Co. LTD. or an authorized representative for more

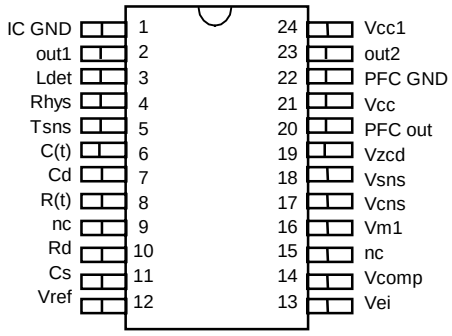
information.

FEATURES

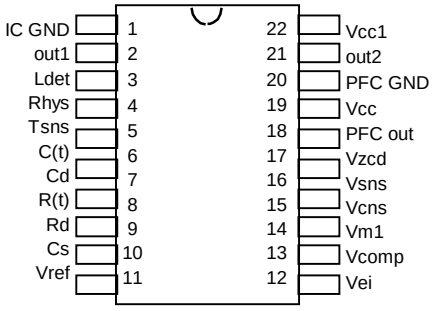
- Complete Power Factor Correction and Dimming Ballast Control on one Chip
- Low Distortion, High Efficiency Boundary Discontinuous Boost, Peak Current Sensing PFC Section
- Programmable Start Scenario for Rapid or Instant Start Lamps and Soft Ignition
- Selectable Variable Frequency Dimming and Starting
- Programmable Restart for Lamp out Condition to Reduce Ballast Heating
- Over-Temperature Shutdown Replaces External Heat Sensor for Safety
- PFC Over-Voltage Comparator Eliminates Output “Runaway” due to Load Removal
- Large Oscillator Amplitude and Current Fed Multiplier Improves Noise Immunity, and Zero Voltage Switching

PIN CONFIGURATION

KA7531D
24-Pin SOP



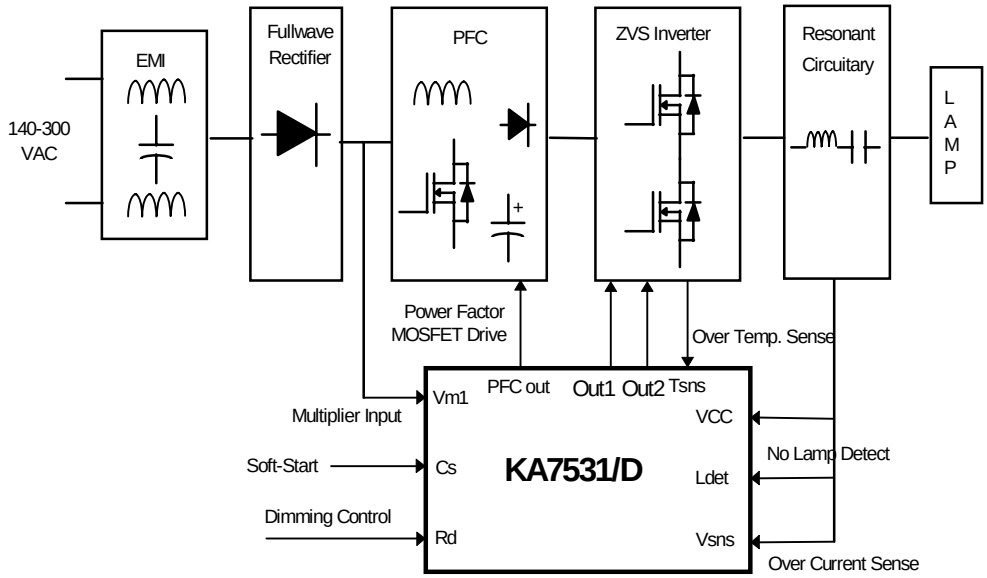
KA7531
22-Pin DIP



SAMSUNG ELECTRONICS

NAME	PIN#		FUNCTIONS
	DIP	SOP	
GND	1	1	IC Ground
Output1	2	2	One of driving outputs of ballast power switching devices. Its' output frequency is dependent on Rt & Ct value. The frequency varies from 50 Khz ± 30 Khz. Normally, the output voltage is 8 V.
Ldet	3	3	Lamp out-of -socket detection input.
Rhys	4	4	Over temperature detecting hysteresis resistor which determined OTP recovery point.
Tsns	5	5	Over temperature detecting input. This threshold voltage is 0.9 V. If the voltage of this point drops down below 0.9 V, the IC will be shutdown.
Ct	6	6	External resistor and capacitor which set internal triangular oscillator frequency determine operating frequency of PFC.
Rt	8	8	
Cd	7	7	Ballast control delay function. The delay time will be determinedby Cd's value. First PFC section operates, then ballast controlsection operates after delay.
Rd	9	10	Dimming control input. This pin can be controlled by sunlight sensing resistor for automatically power intensity adjusting, or be controlled by manual.
Cs	10	11	This capacitor determines soft-start period when lamps turn on at the moment.
Vref	11	12	Internal 5 voltage. If the voltage of this pin drops down to low voltage, the IC will be shutdown. So, this pin can be designed for reset function or remote control function.
Vei	12	13	Inverting input of PFC peak current error amplifier.
Vcomp	13	14	output and compensation node of the PFC average current error amplifier.
Vm1	14	16	Multiplier input of voltage of PFC section. This reference voltage takes from the input rectified mains. The best designed input value is < 2V.
Vcns	15	17	Multiplier input of sensing current of PFC section.
Vsns	16	18	OVP & OCP detecting input. On the normal condition, this pin's voltage is 1.5V ~ 2 V. If this voltage rises to 2.5 V above, the IC will be shutdown.
Vzcd	17	19	Zero current detecting input. This pin detects the zero point of input inductor current , then automatically determines oscillator frequency of PFC section.
PFC out	18	20	Driving output of power switching device in PFC section. Normally, the output voltage is 9 V.
Vcc2	19	21	Positive supply for the PFC section. Normally, the voltage is 20 V.
GND	20	22	PFC section ground.
Output2	21	23	One of driving outputs of ballast power switching devices. Its output frequency is dependent on Rt & Ct value. The frequency varies from 50 Khz ± 30 Khz. Normally, the output voltage is 8 V.
Vcc1	22	24	Positive supply for the IC. Normally, the voltage is 20 V.

SYSTEM BLOCK DIAGRAM (KA7531/D)



Application System (For 2 lamps with 32W each)

❒ Introduction

This application note introduces the design and the application of the Electronic Ballast, which is for driving 2 lamps by means of the KA7531/D, Electronic Ballast controller IC. The features incorporated in this system are described as following :

① Soft - Start function: minimizes the eye-strain and extends lamp life and avoids lamp's flicker caused by high peak-current due to negative-resistance characteristic of fluorescent lamp.

② No-Lamp Detection: offers minimum power dissipation by stopping system operation when any lamp is out-of socket.

③ Overheating Protection function: cuts off system operation to protect the elements from overheating in main power circuit caused by lamp misconnection and characteristic failure of the main power circuit.

④ Emergency shutdown function: cuts off the system operation when lamp is in bad condition r any characteristic failure happens in the ballast system

⑤ Dimming function: controls the light-intensity automatically depending on the amount of sunlight. (Manual control is also available.)

⑥ The main power circuit: includes a half bridge type converter, Zero voltage switching (ZVS) is also available to minimize switching losses and radioactive noises. The power block includes a KA7531/D Power Factor Correction (PFC) IC to get higher efficiency. And IRF 830, power MOSFET is used as a main power switching element. The adopted fluorescent lamp in this system is SILVANIA FLR32 (32W) and the selected operating frequency of main power circuit is 50 [㎑].

❒ Description of Function Block

❶ Brief Introduction

The KA7531/D is a complete solution for a dimmable, high power factor, high efficiency electronic ballast. The KA7531/D consists of a peak current controlled boost Power Factor Correction front end section with a flexible ballast control section. Start-up and lamp-out retry timing are controlled by the selection of external timing components, allowing for control of a wide variety of different lamp types. The ballast control section can be set up to adjust lamp power using frequency modulation (FM).

① Driving control of fluorescent lamp

- Soft-start function : 3-step mode in frequency modulation method
- Zero Voltage Switching (ZVS) in main power circuit : minimizes system power dissipation

② System Protection

- No lamp protection : system is shutdown immediately in case lamp out-of-socket is detected
- Overheating protection : system will be shutdown when main power elements are overheated
- Emergency shutdown : system will be shutdown in case of any emergency or systematic hazard.

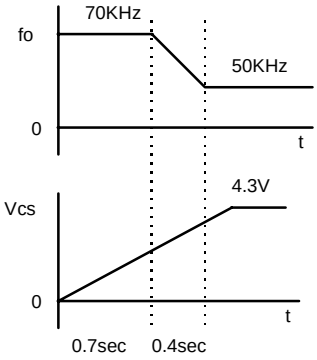
③ Dimming Control of fluorescent lamp

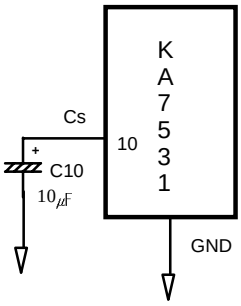
- Dimming control : controls the fluorescent lamp intensity.

❷ General Description of Function Block

① Soft-Start

The 3-step-soft-start function is that first preheats filament for 0.7 [sec] with a 20Khz operating frequency higher than normal operating frequency of IC (50Khz), and then, decreases the operating frequency to 50Khz in about 0.4[sec], at last, keep on its' normal operating frequency at 50Khz stably.





$$C = i \frac{dt}{dV} \quad ....(1)$$

i=17 ㎂ is charged through the capasitor

dV = Cs is charged to 4.3V which is standard voltage .

dt = the charging time to 4.3 V is 1.1[sec]

using by , C= i dt /dv

(FIG 1)

In this system, frequency modulation method is used to avoid rapid current flow caused by negative-resistance characteristics while lamp was drived. Pre-heating, Soft-start and Full-Power, so called, 3-step mode is available to drive lamp. 3-Step mode of controller is described as follows:

- < Preheating >

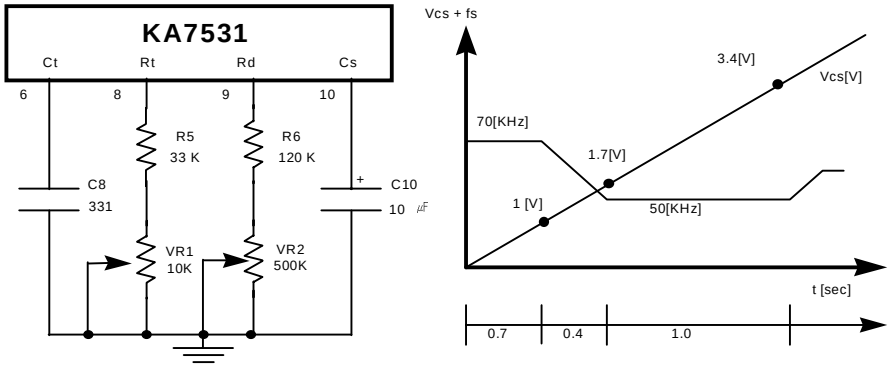
  During the preheating period of 0.6[sec], the charged voltage of C10 (10㎌) of controller pin 8 is in a range of 0 ~ 1.0 [V].

- < Soft - start >

  The controller starts the lamp which decreasing output frequency from preheating level to full-power level and avoids rapid current from lamp. During soft-start period of about 0.4 [sec] the charged voltage of C10 (10㎌) will be in a range of 1.0 ~ 1.7 [V].

- < Full - power >

  Full-power is available for constant lamp-starting and to operate the controller by the established frequency at Rt (R5, VR1) of pin 6. During this period of about 1 [sec], the charged voltage of C10 (10㎌) is in a range of 1.7 ~ 3.4 [V].



(FIG 2)

- Time establishment of 3-step mode

  ic : Current amount of Cs (17㎂)

  Cs : Soft-start capacitor (C10)

  dv : Electrical potential of Cs, which determines the time range in the 3-step mode (Vcs).

  dt : Charging time of Cs

Thus the fundamental becomes.

ic = Cs × dv / dt

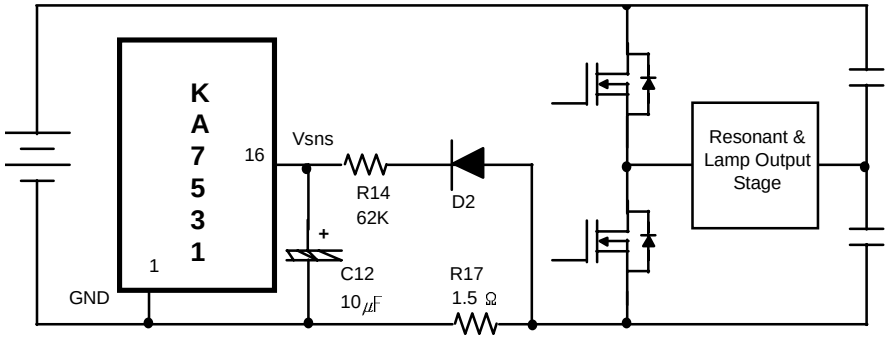
The time establishment of 3-step mode is dependent on the value of Cs.

If Cs (C10) remains 3.4[V] for about 2 seconds the ic will be 17㎂.

Therefore, if dv is 3.4 and dt is 2, Cs will be 10 [㎌] according to the above formula.

❷ Over Current Protection

In this function, when input current becomes higher than its normal condition, the over current sensing resistor will achieve high value, above 2.5 V, IC will be shutdown automatically to protect the system from being subjected to excessive currents if the load should change suddenly (lamp removal).

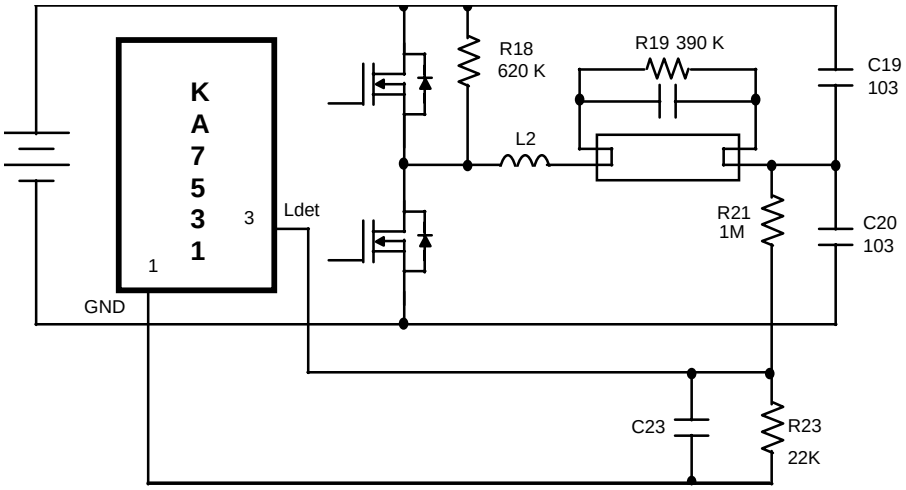


(FIG 3)

In the normal state, after removal of over-current state, IC's output is on-state. To make output on-state, IC's internal atch must be removed. In order to get above function, UVLO must be changed from off-state to on-state .

❸ No-Load Protection

The KA7531/D have a function of sensing lamp in-socket or out-of-socket. In case of no load, this system has a protection circuit to keep system from damage, and to let IC shutdown. When the in-socket state changes from 1 lamp to 2 lamps, IC reset function will operate to restart by 3-step-soft -start . And also new inserted lamps strikes after filament preheating.

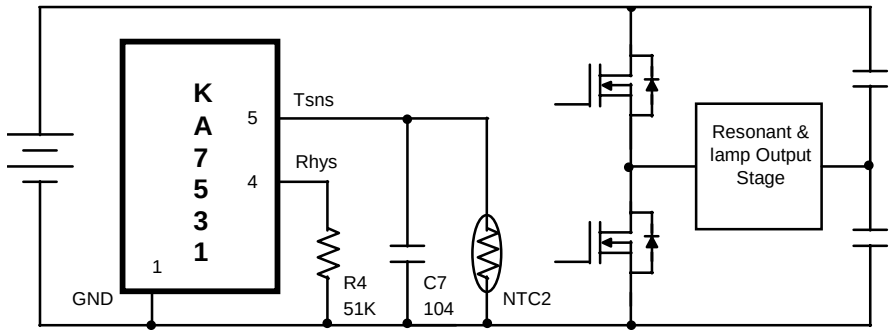


(FIG 4)

When the pin3 voltage becomes lower than 1.4 V, the outputs of driving ballast will be shutdown. In the state of lamp insertion, DC voltage is devided by R18, R19, R21, R23. DC link voltage in R23 is supplied to pin3 (Ldet) more than 1.4V.

④ Over Temperature Protection

This function is designed to protect system by shutdown of IC's output. Using a NTC (negative temperature coefficient) as a sensing component, this system senses an emitting heat state of power switching components, when sensed temperature is more higher than specified temperature, the IC will be shutdown as soon as possible.



(FIG 5)

In this circuit, If pin5 voltage Tsns is less than 0.9V, IC's output is shutdown. Once the system is shutdown, this system will restart with temperature hysteresis characteristics which depends directly on pin4 voltage. This circuit is designed for shutdown at 85℃ and restart at 50℃. The NTC has a value of 50kΩ at the temperature of 25℃.In this system, "503AT" NTC with resistance of 50kΩ at 25℃ is used. Table 1 shows the relationship between NTC resistance and temperature

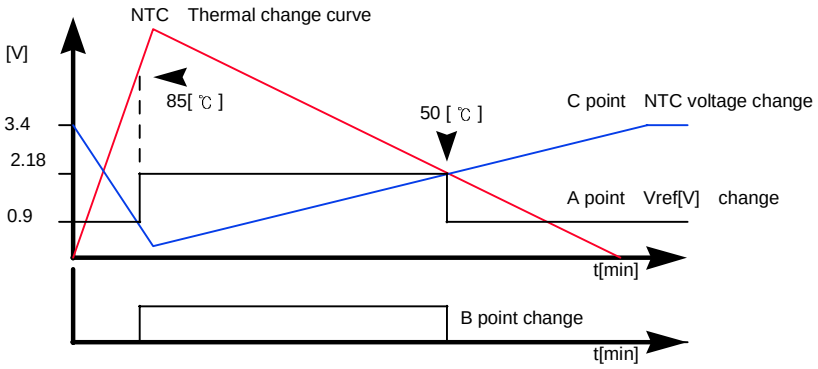
Table 1. * reference : resistance and NTC' temperatures

T ℃ / NTC	20	25	30	40	50	60	70	80	85	90	100	110	B 25/85
503AT[kΩ]	62.5	50.0	40.2	26.4	17.7	12.1	8.48	6.02	5.10	4.34	3.18	2.37	4060
202AT[kΩ]	24.9	20.0	16.1	10.6	7.18	4.94	3.46	2.46	2.09	1.78	1.31	0.98	4013
103AT[kΩ]	12.0	10.0	8.31	5.82	4.16	3.02	2.22	1.66	1.45	1.26	0.97	0.75	3435

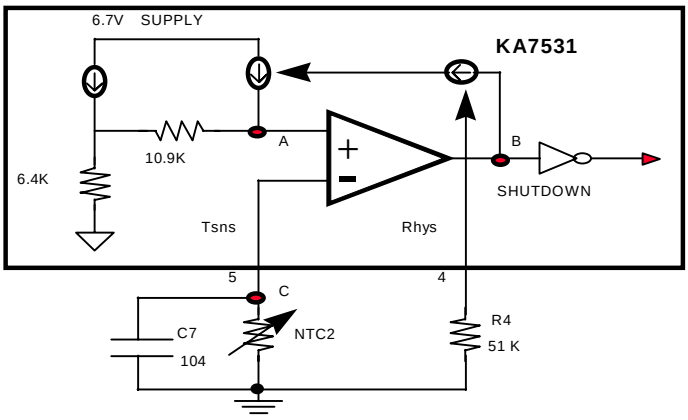
In order to re-operate the system at 50℃, which was shutdown at 85℃, the built-in comparator's Vref should be 2.18 V when NTC has a resistance of 17 kΩ at 50℃. According to table 2, the Rhys (R4) is 56 kΩ when Vref is 2.18[V]. Therefore Rhys (R4) of 56[kΩ] is available to re-operate the system at 50℃. Fig.7 shows the internal comparator's output variation which depends on NTC's thermal change and Vref variation by Rhys resistance.

Table 2. The relationship between Rhys and Vref

Rhys [kΩ]	27	26	28	30	31	34	41	56	68	70	———
Vref [V]	3.58	3.49	3.35	3.21	3.14	2.97	2.65	2.18	1.95	1.91	———



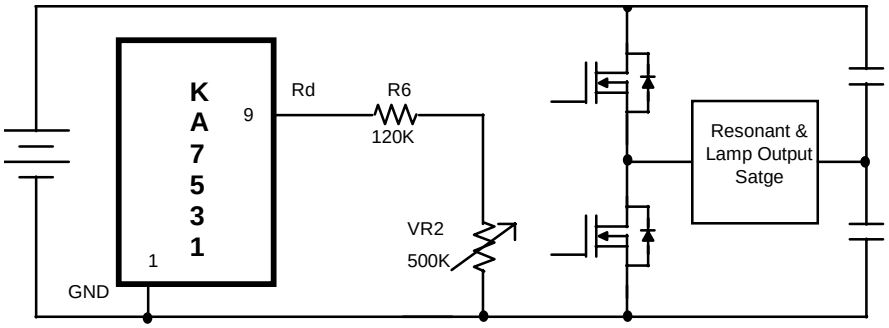
(FIG 6)



(FIG 7)

⑤ Dimming Control

Current flowing into Rd is controlled by adjustable VR2 (500K). And this makes output frequency variable. In the end, dimming control is possible.



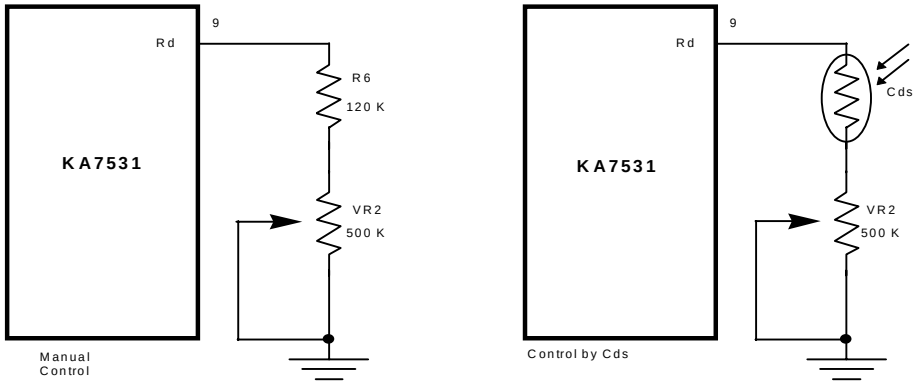
(FIG 8)

Lamp Dimming adjusts the outputs for constant light intensity (Auto / manual control methods are both available).This function can be achieved by means of output frequency modulation by adjusting the resistance of the controller pin 9. With automatic dimming control system, the optical element, Cds, which has a variable resistor with the light, can be used as the dimming resistor of pin 9.If the dimming function is not required, open the dimming resistor of Rd (R6) and set its value at over 500[kΩ]. Application circuit for manual dimming control is designed in this system with the variable resistor using VR2 instead of Cds. (Table 3 shows the correlation among dimming resistor Rd, output frequency fo , and the output power Pw of the controller pin 9) .

Table 3. < Correlation of Rd-fo-Pw >

Rd [kΩ]	356.6	278.2	215.9	138.2	106.2	81.4	70.3	66.2	62.1	60.6
fo [kHz]	50	52	54	60	63.5	68	71	72.5	74	74.6
Pw [W]	64	62	60	55	50	43	35	30	20	16

Cds, the selected optical element should have a negative-resistance characteristics depending on the amount of lighting.



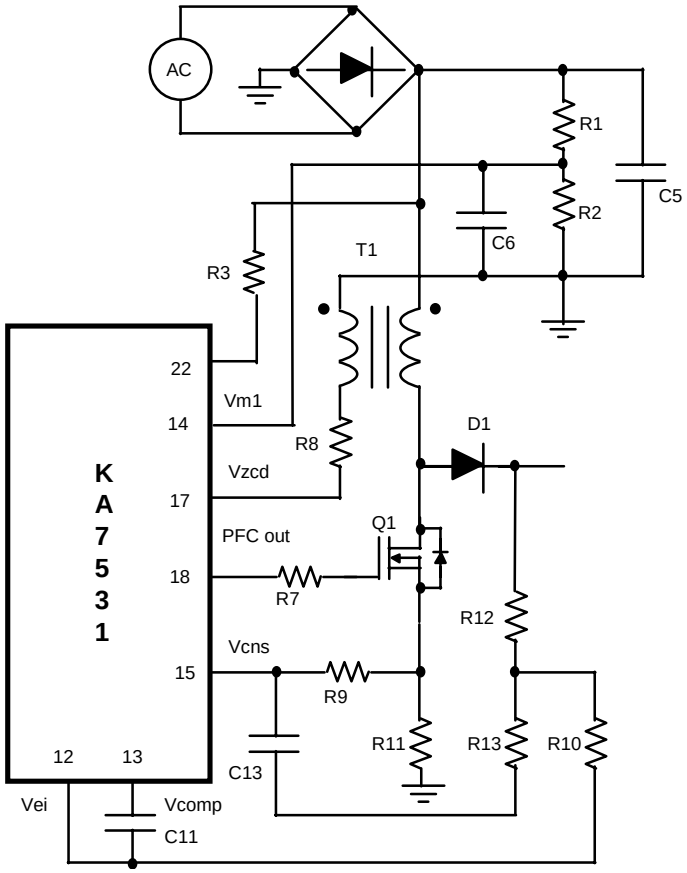
(FIG 9)

⑥ Power Factor Correction (PFC)

The Power factor circuit uses the peak current sensing method with a current fed multiplier and over-voltage protection. This system produces power factors of better than 0.99 with low input current THD at > 95% efficiency. Special care has been taken in the design of the KA7531 to increase system noise immunity by using a high amplitude oscillator, and a current fed multiplier. An over-voltage protection comparator stops the PFC section in the event of sudden load decrease. Refer to Application Note of KA7525 for additional design information about PFC.

omparison table of KA7531 PFC section and KA7525

IC	Pin Number							
KA7531 PFC Section	12	13	14	15	17	18	19	20
KA7525	1	2	3	4	5	7	8	6



Pin 12 (INV) leads to the inv. input of the error amplifier and to the over-voltage protection (OVP). A resistive divider will be connected between the regulated output voltage and INV pin. The typical voltage feedback input threshold is 2.5V and the precise over-voltage alarm level current is 40mA. R7 and R8 will be selected as follow :

$$R12/R13 = (VO / 2.5V) \pm 1$$

$$R12 = \Delta VOUT / 40\ \mu A$$

Pin 13 (COMP) is the output of the error amplifier (and one of the two inputs to the multiplier). A feedback compensation network, placed between this pin and INV(1), can reduce the frequency block gain to get better output voltage ripple. Typically this compensation is just a capacitor that makes possible to reduce the gain for the low frequency output ripple (to minimize the third harmonic distortion) sustaining an high DC gain. A simple criterion, to define the capacitor value, is to set the bandwidth (BW) from 20 to 30Hz.

$$BW = 1/ (2 \pi \times R12 / / R13 \times C comp)$$

$$C comp \geq 1/ (2 \times \pi \times R12 / / R13 \times BW)$$

This pin can be used also to disable the IC. For this function see Appendix A.

Pin 14 (MULT) is the second multiplier input. It has to be connected, through a resistive divider, to the rectified mains.

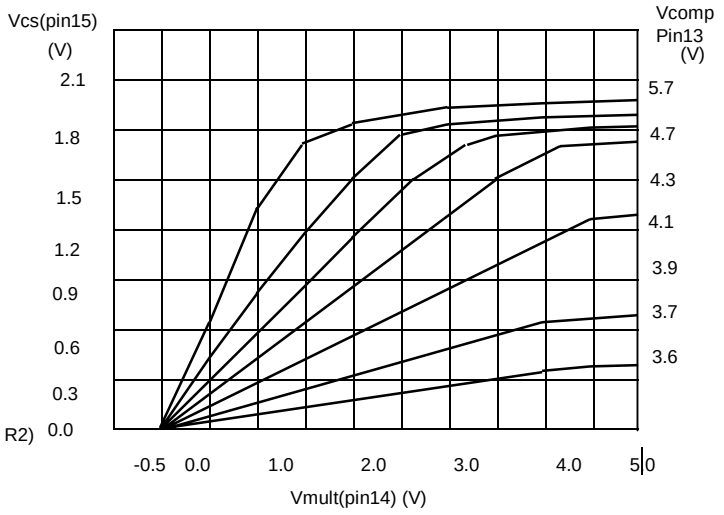
The feature of the multiplier is described by the relation:

$$xcs = k \times (V comp \pm 3.5V) \times V mult$$

where:
VXCS (Mult.out) is the Input ref. to current-sense;
k is the multiplier gain;
Vcomp is the Comp. Output;
Vmult is the multiplier input.
In the application circuit:

$Vmult = (Vin \times R2) / (R1+R2)$

$Vmultpk = (Virms \times \sqrt{2} \times R2) / (\overline{R1} + R2)$



The Mult. gain k can vary point to point. Above diagram shows the typical multiplier characteristics family in variable inputs condition. The output of the multiplier controls the peak current flowing in the sense resistor, each cycle of operation.
The best value of Pin14 is < 2V.

Pin 15 (C.S) is the input (inv.in) for the current sense comparator, the instantaneous Mosfet current is converted in a proportional voltage signal by an external sense resistor. Comparing this signal with the threshold set by the multiplier output, as the current exceed the set value, the power mosfet will be turned off by the reset signal until next set by the PWM latch. An internal circuit (Zero-current comparator) ensures that the PWM latch can't be set until the signal on pin 15 (C.S) disappear. The sense resistor (Rs) values calculated as:

$$R \leq V xcspk / I Rspk$$

where: V xcspk cannot exceed 1.6V max. value

$$I Rspk = (2 \times \sqrt{2} \times \overline{Pi}) / Virms$$

Pin 17 (ZCD) is the input to the zero current detector. The ZCD pin has to be connected, through a limiting resistor, to the auxiliary winding of the booster inductor. To perform the ZCD (zero-coil current detecting) function the chip processes the inductor signal and turns on the external Mosfet as the voltage at the pin crosses the threshold level 2.3 V to 1.1V (negative sensitive edge).

Pin 18 (PFC output), output of the driver, this pin is able to drive an external Mosfet with 400mA (source and sink).

Pin 19 (Vcc). Input for the supply voltage, this pin is externally connected to a filter capacitor. The minimum start up supply voltage has to be reached. (It depends on the version, see electrical characteristics on the data sheet). If the supply decreases below VCCoff the device recognizes the under-voltage condition and stops driving the external Mosfet.

Pin 20 (GND), this pin is the common reference of the circuitry.

⑦ Internal OSC. Frequency Generation

$$f = \frac{1}{T}$$

$$T = t_{ch} + t_{dch} = \frac{Ct \times dV}{¡^{ct}} + 0 \quad \text{---------- (1)}$$

tch : Ct charge time

tdch : Ct discharge time

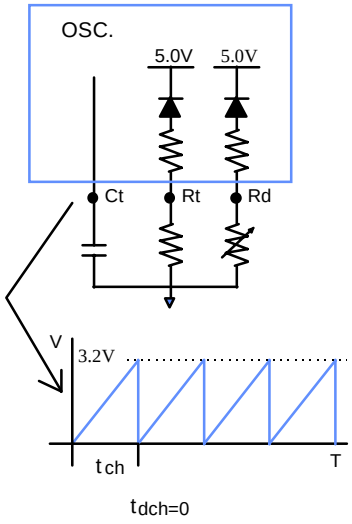
dV : Ct Charge voltage = 3.2[V]

¡ct : Ct Charge current

$$¡^{ct} = \frac{(5V - 0.7V)}{(7K + Rt)}$$

¡rd : Dimming current

$$¡^{rd} = \frac{(5V - 0.7V)}{(12K + Rd)}$$



1) OSC. Frequency, when Soft-start

$$T = \frac{Ct \times dV}{¡^{ct} + 43\,\mu A} \quad \text{---------- (2)}$$

2) OSC. Frequency, when normal operating

$$T = \frac{Ct \times dV}{¡^{ct}} \quad \text{---------- (3)}$$

3) OSC. Frequency, when dimming

$$T = \frac{Ct \times dV}{¡^{ct} + ¡^{rd}} \quad \text{---------- (4)}$$

⑧ Pin 22 Design Circuit

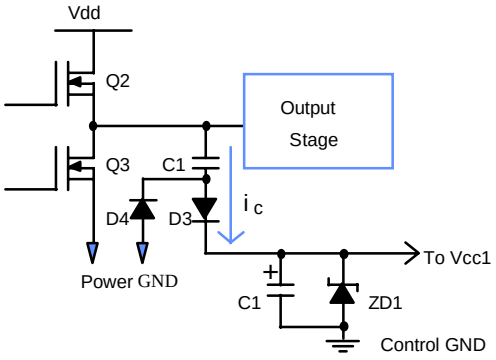
ic = IC operating current

dv = Vdd

dt = 1/switching frequency

$$ic = \frac{C1 \times dv}{dt} \quad \text{----- (1)}$$

$$C1 = \frac{ic \times dt}{dv} \quad \text{------ (2)}$$



⑨ Series Resonant parallel Loaded Converter for Fluorescent Lamp Design Rules

Vlamp: Lamp Voltage
Ilamp: Lamp Current
Rlamp: Lamp impedance

V_{BDmin} : Lamp brackdown voltage.
Vrf : Filament voltage = 3.5 - 4.5[V]
Rf : Filament resistance = 4[Ω]

QL: Lamp resonant loop factor
Zo: Loop equivalent input impedance
Ct: Equivalent resonant capacitance
LS: Resonant inductance

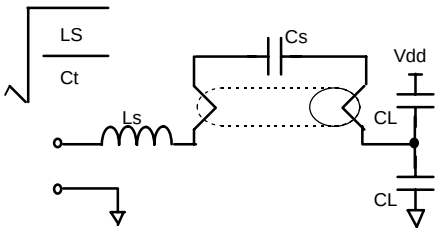
QL Determine

$$QL = \frac{Vlamp}{(\sqrt{2}/\pi) \times Vdd}$$

$$Rlamp = Vlamp / Ilamp$$

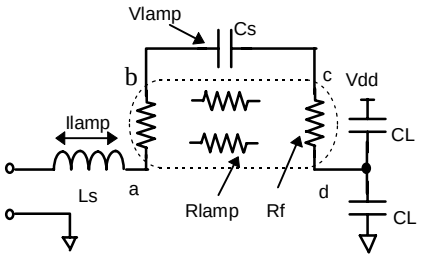
Zo Determine

$$Zo = \frac{Rlamp}{QL} = \sqrt{\frac{LS}{Ct}}$$



fo : Resonant Frequency Determine

$$fo = \frac{1}{2\pi \times \sqrt{LS \times Ct}}$$



LS, Ctotal Determine

$$LS = Zo^2 \times Ct$$

$$Ct = \frac{1}{2\pi \times fo \times Zo}$$

CL, CS Determine

$$CLmax = \frac{Vdd \times (2/\pi)}{(\omega O^2 - \omega S^2) \times LS \times V_{BDmin}}$$

$$CL = \frac{Vrf}{Rf \times \omega s \times Vlamp}$$

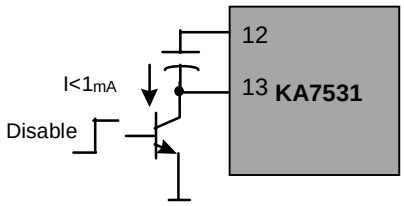
$$Cs = \frac{CL \times Ct}{CL - Ct}$$

❒ **APPENDIX A**

• **Disable Function**

The PFC section of KA7531/D allows an easy mode to be disabled. If for some reason, the system using PFC section needs to disable this function, the best way is to force Pin13 (E/A output) to a voltage below 2.5V (see fig A1). That allows also to reduce the supply consumption of the IC during the disable so the startup circuit is able to re-start the system once the disable condition is re-moved.

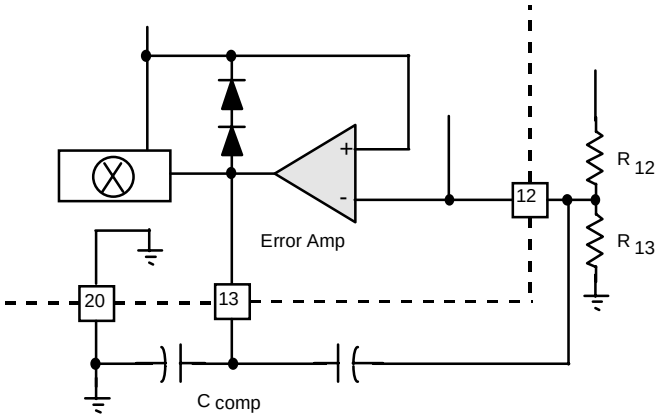
Figure A1: KA7531 Disable Function



• **Error Amp Compensation**

The Error Amp output is a high impedance node and is susceptible to noise pickup. To minimize pickup, compensation capacitor Ccomp must be connected as close to Pin 13 as possible with a short, heavy ground returning directly to Pin 20. When operating at high ac line, the voltage at Pin 13 may approach the lower threshold of the Multiplier, ≈ 2.0 V. If there is excessive ripple on Pin 13, the Multiplier will be driven into cut-off causing circuit instability, high distortion and poor power factor. This problem can be eliminated by increasing the value of Ccomp .

Figure A2: KA7531 Error Amp. Comp.



❒ Functions Comparison table (KA7531 / KA7522 / KA7521)

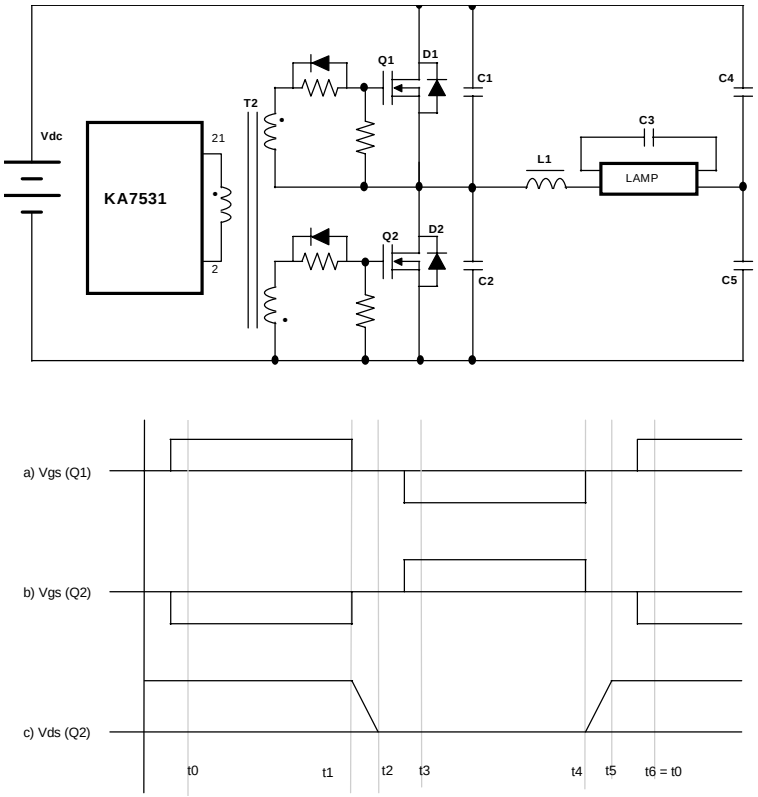
As follows, A comparison table of a series “PFC + PWM” dimming control Ics (KA7531 / KA7522 / KA7521) is described. KA7531 is the advanced new product with best characters and functions.

Parameter	KA7521	KA7522	KA7531	Remark
1. P. F. C	about 0.67	about 0.67	over 0.99	
2. Soft-Start Function	○	○	○	
3. Input Voltage Variation Protection	AC 220V -20% +50%	AC 220V ± 50%	AC 220V ± 20%	
4. Over-Voltage Protection	○	○	○	
5. Emergency System Protection	○	○	○	
6. Over-Heating Protection	○	○	○	
7. Non-lamp Detection	○	○	○	
8. Dimming Control	100% ~ 10%	100% ~ 10%	100% ~ 10%	
9. ZVS-Driving	○	○	○	
10. ZVS Guard Control	-	○	-	
11. Current Feedback Control		○	-	
12. Lamp reset	- -	○	-	Preheating function while lamp setting on Power-on stage
13. Input limit & Brown out	-	○	-	
14. Low Temperature sense for preheating time control	-	○	-	

* KA7521 and KA7524 are constructed in a single construction of KA7531

❒ Basic Operation Principles of the Main Power Switch

The following figure illustrates the main power circuit of Ballast using a serial resonant type converter. DC-link voltage source Vdc can be obtained by rectifying the AC 220V voltage. MOSFET switches Q1 and Q2 are alternately turned on / off by the controller in the half -bridge inverter. This switching voltage is applied to resonance tank (L1 and C3). Resonance current runs through inductor L1 and then fluorescent lamp is discharged. Fluorescent lamp with negative resistance characteristics can easily be treated as a simple resistor after discharge is completed. When the voltage is in zero state between the drain and the source, Zero Voltage Switching is available with the free wheeling diode internally attached in MOSFET which allows minimization of power loss. C1 and C2 charge or discharge only during the switching period which can minimize switching noise and finally reduce EM1.



❒ SYSTEM ANALYSIS IN EACH MODE

The above figure shows each period waveform of the main power circuit. The voltage waveform between the gate and the source can be set according to the operation of control IC's gate driving circuit. The following describes the prior state before a new period starts. When the current Ir flowing through the resonant circuit is negative and the also running through the MOSFET free wheeling diode D1, MOSFET Q2 will turn on the output signal of the controller gate driver. However, the resonant current cannot flow into the drain of Q2 because the current or is still flowing in a negative direction.

➠ Mode 1. (t0 ~ t1)

When the direction of current Ir running through the resonant circuit changes to the positive, the current path will change from D1 to Q1. In this mode, DC-link voltage (Vdc) provides power via MOSFET Q1 and accumulates energy in the resonant circuit.

➠ Mode 2. (t1 ~ t2)

When MOSFET Q2 is turned off, the current Ir flows through C1 which is connected with MOSFET in parallel. As a result of the continuous change of C1, MOSFET Q2 Vds becomes zero. The system changes to (or remains in) mode 3 .

➠ Mode 3. (t2 ~ t3)

If the voltage of MOSFET Q2 drops to zero in this resonant circuit, the pre-wheeling function can be performed because diode D2 conducts and supplies the resonant current Ir. In this mode, when the direction of Ir changes to negative, Q2 must be turned on so that MOSFET Q2 can implement zero-voltage-switching.

➠ Mode 4. (t3 ~ t4)

When the direction of Ir changes to negative, current flows through Q2 so that Free-Resonance occurs at the resonant circuit. At that time the capacitor C5 can be used as a power source.

➠ Mode 5. (t4 ~ t5)

When Ir is free-resonance, Q2 will be turned off by the controller and the current Ir flows by discharging capacitor C1. Therefore, the Vds of MOSFET Q2 will increase to the level of DClink voltage, Vdc.

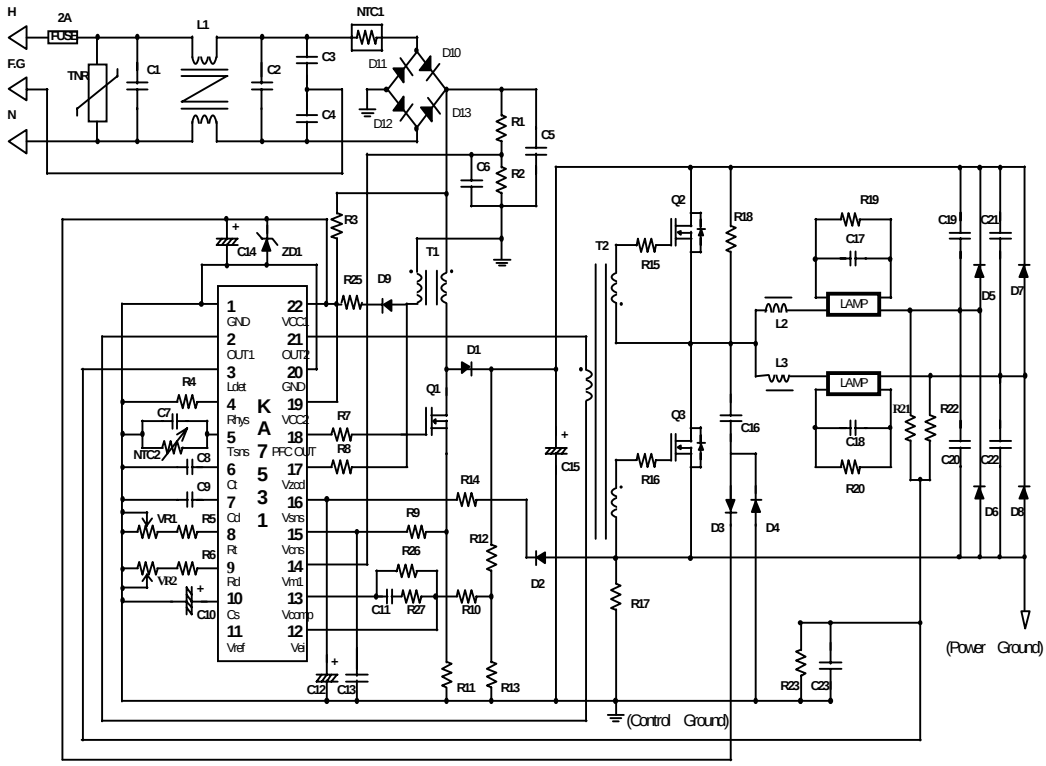
➠ Mode 6. (t5 ~ t6)

After the voltage of MOSFET Q2 rises to the level of the DC-link voltage, D1 will be turned on and Ir will flow into Vdc. In this mode, energy regeneration of the resonant circuit can be implemented through D1. Because D1 is on, the controller generates the control signal for zero-voltage-switching. After MOSFET Q1 is turned on and the direction of Ir changes to the positive, Ir flows through the drain of Q1.

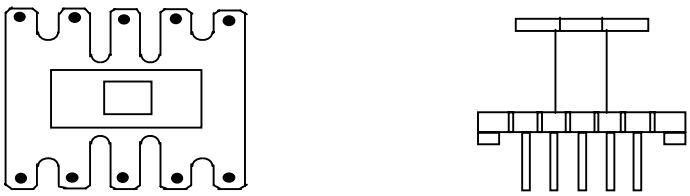
❒ Typical Application Circuit

his design is a version of Samsung's KA7531 220V ballast Demo-Board. The KA7531 D/B 220V is also designed for operating over the range of 250 to 300 VRMS, this power factor corrected 64W electronic ballast, with dimming range capable of a 10 : 1 intensity change, with optimized to power two parallel-connected fluorescent lamps, and displays all the features of Samsung's KA7531 ballast controller IC. The mode of operation used for preheat, striking and dimming of the lamps is the widely accepted variable frequency, non-overlapping inverter topology.

KA7531 APPLICATION CIRCUIT



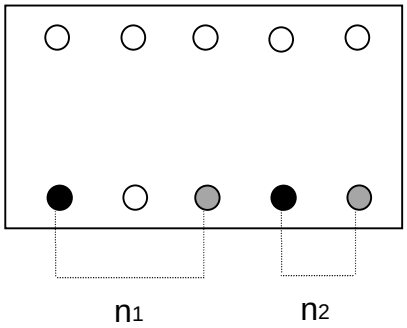
❒ Transformer Specification



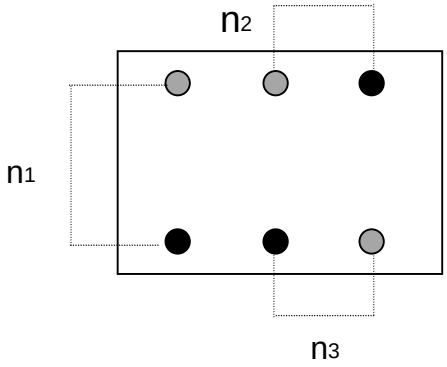
Selected magnetic core type: TDK H7C1 EI 28 for T1, L2, L3

Selected magnetic core type: TDK H7C1 EE 1619 for T2

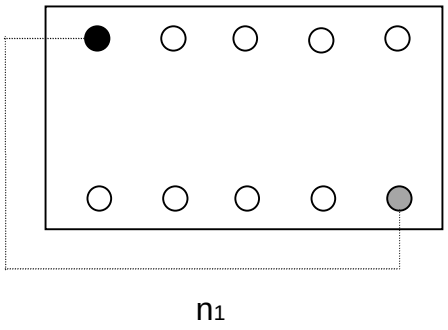
T_1: EI 28



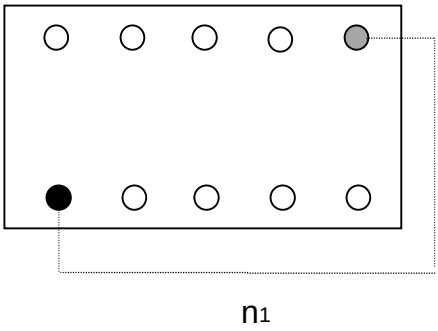
T_2: EE 1619



L_2: EI 28



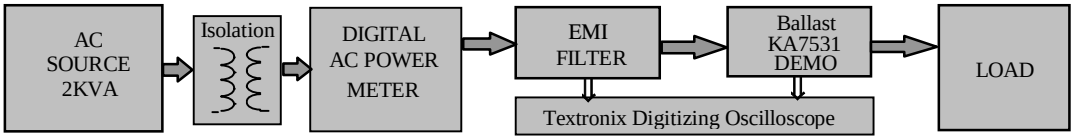
L_3: EI 28



ITEM	Φ	n1	n2	n3	n1(value)	Remark
T1	0.35	70 T	8 T	---	1.3 mH	
T2	0.25	32 T	24 T	24 T	---	
L2, L3	0.35	120 T	---	---	2.5 mH	

❒ Demo-Board Evaluation Results

To evaluate the PFC demo-board performance, the following parameters have been tested: PF (power factor), A_THD (percentage of current total harmonic distortion), V_THD (percentage of voltage total harmonic distortion),H3...H9 (percentage of current n harmonic amplitude), Vcf (voltage crest factor), Acf (current crest factor), Pi (input power).
Test results are shown below : (testing condition: Temp = 25℃)



Vi (V)	Pi (W)	PF	A_THD %	V_THD %	AH3 %	AH5 %	AH7 %	AH9 %	Pi (VA)	Acf	Vcf	
160	76.25	0.995	9.5	1.2	7.9	3.2	0.72	1.75	76.53	1.52	1.39	
180	77.65	0.992	12.22	1.2	9.8	3.8	2.1	0.8	78.05	1.64	1.41	
220	76.27	0.991	12.6	1.2	9.3	1.6	1.7	0.6	76.94	1.62	1.41	
260	74.53	0.986	15.2	1.2	11.9	2.6	0.7	0.3	75.52	1.66	1.42	
280	75.53	0.983	17.02	1.2	14.7	2.8	0.5	0.15	76.7	1.82	1.44	

Testing Notice*:*

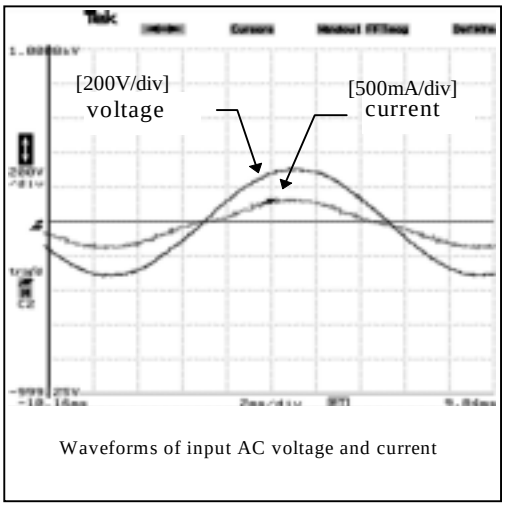
- ➨ Isolation must be used in order to get the correction PFC and clear waveforms of the ballast set.
- ➨ Dimming control function must be tested on full output power. (VR1 for adjusting full output power, VR2 for adjusting dimming control)
- ➨ Both of the R11 and R2 will have an effect on PFC, waveforms, devices heating and input AC voltage range of ballast sets sensitively. (If R11 is 1Ω and R2 is 10KΩ , the devices heating decreases to 33 ℃, PF increases to 0.994, but the input AC voltage range reduces from 190VAC to 270VAC, the waveforms becomes little bad. If R11 is 1Ω and R2 is 6.2KΩ , the devices heating increases to 47 ℃, PF decreases to 0.991, but the input AC voltage range enlarges from 7.160VAC to 280VAC, the waveforms becomes better. If R11 is 0.5Ω and R2 is 10KΩ , the devices heating increases 8.to more than 50 ℃, PF decreases to 0.989, but the input AC voltage range enlarges from 140VAC to 300VAC, and the 9.waveforms also becomes little bad.)
- ➨ The voltage of Pin14 of KA7531 must be designed below 2V, this pin voltage will directly have an effect on system PF and waveforms.
- ➨ PCB layout designing must abide the following rules: short connecting in PFC part, reduce ground jump line, thicken the ground line and device source line, symmetry.

❒ Parts List

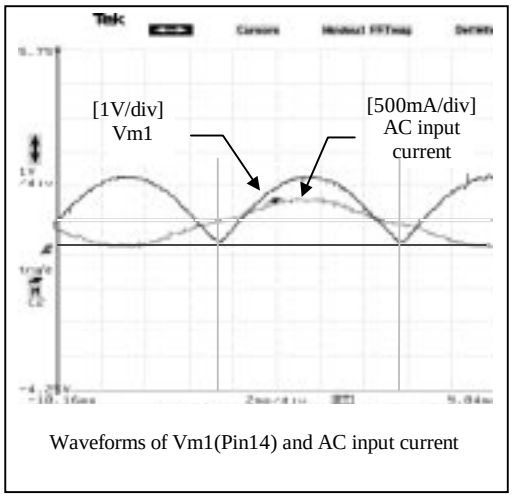
ITEM	VALUE	ITEM	VALUE	ITEM	VALUE
R1	1 MΩ 1/2W	C1	0.1 μF 630V	TNR	12G471K
R2	6.2 kΩ 1/2W	C2	0.1 μF 630V	NTC1	10D - 11
R3	100 kΩ 1/2W	C3	4700 pF 250V	NTC2	KTD5 - 350 (50 kΩ)
R4	51 kΩ	C4	4700 pF 250V		
R5	39 kΩ	C5	563 630V	D1	1N4937
R6	120 kΩ	C6	103 40V	D2 - D4	1N4148
R7	27 Ω	C7	104 16V	D5 - D8	1N4937
R8	22 kΩ	C8	331 10V	D9	1N4937
R9	330 Ω	C9	103 10V	ZD1	18V 1W
R10	150 kΩ	C10	10 μF 35V		
R11	0.68 Ω 1W	C11	104 16V	Q1 - Q3	IRF830
R12	1 MΩ 1/2W	C12	10 μF 35V		
R13	5.6 kΩ 1/2W	C13	332 10V	L1	BSF-2125
R14	62 kΩ	C14	10 μF 35V	L2, L3	EI28
R15	51 Ω	C15	47 μF 250V	T1	EI28
R16	51 Ω	C16	152 630V	T2	EE1619
R17	1.5 Ω	C17	682 1600V		
R18	620 kΩ	C18	682 1600V		
R19	390 kΩ	C19	103 630V	IC	KA7531
R20	390 kΩ	C20	103 630V		

R21	1 MΩ	C21	103 630V	FUSE	2 A / 300V
R22	1 MΩ	C22	103 630V		
R23	22 KΩ	C23	103 10V		
R26	2.2 MΩ	C24	47 uF 250V		
R27	2.2 KΩ				
R25	10 Ω / 1W				
VR1	10 KΩ				
VR2	500 KΩ				

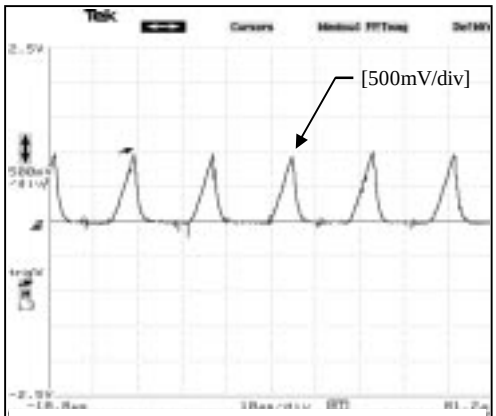
❒ Demo-Board Testing Waveforms



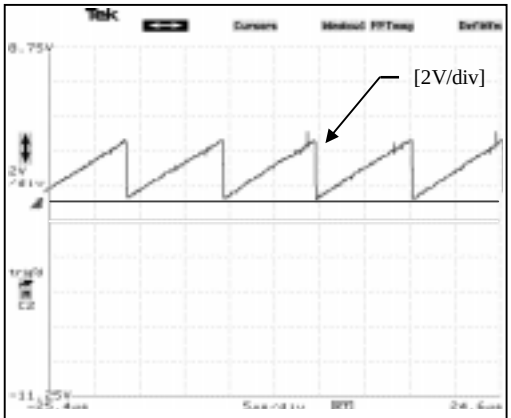
Waveforms of input AC voltage and current



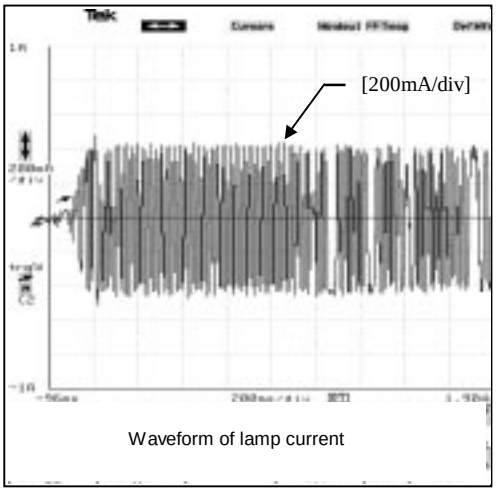
Waveforms of Vm1(Pin14) and AC input current



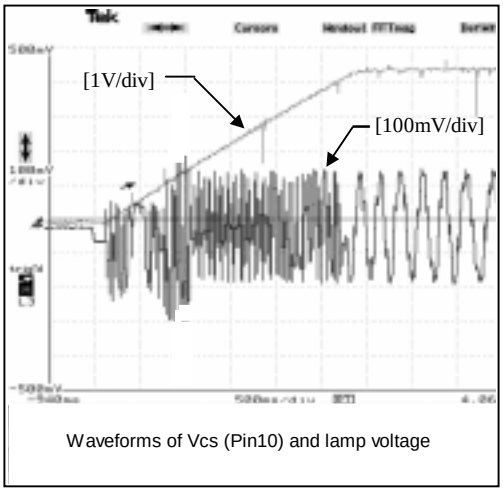
Waveform of multiplier input of current (Pin15)



Waveform of Pin 6



Waveform of lamp current



Waveforms of Vcs (Pin10) and lamp voltage

❒ **PCB Layout**