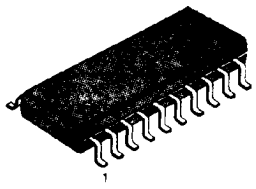
3-PHASE DRUM MOTOR DRIVER

KA3081D is a bipolar integrated circuit and used to drive 3-phase brushless DC motor in full wave mode using 1-Hall sensor.
KA3081D uses 1-Hall for commutation and PG generation.
It is a special circuit for soft switching using 1-Hall reduces the EMI and eliminates snubber. The FG is generated by BEMF.

20-SOP-300



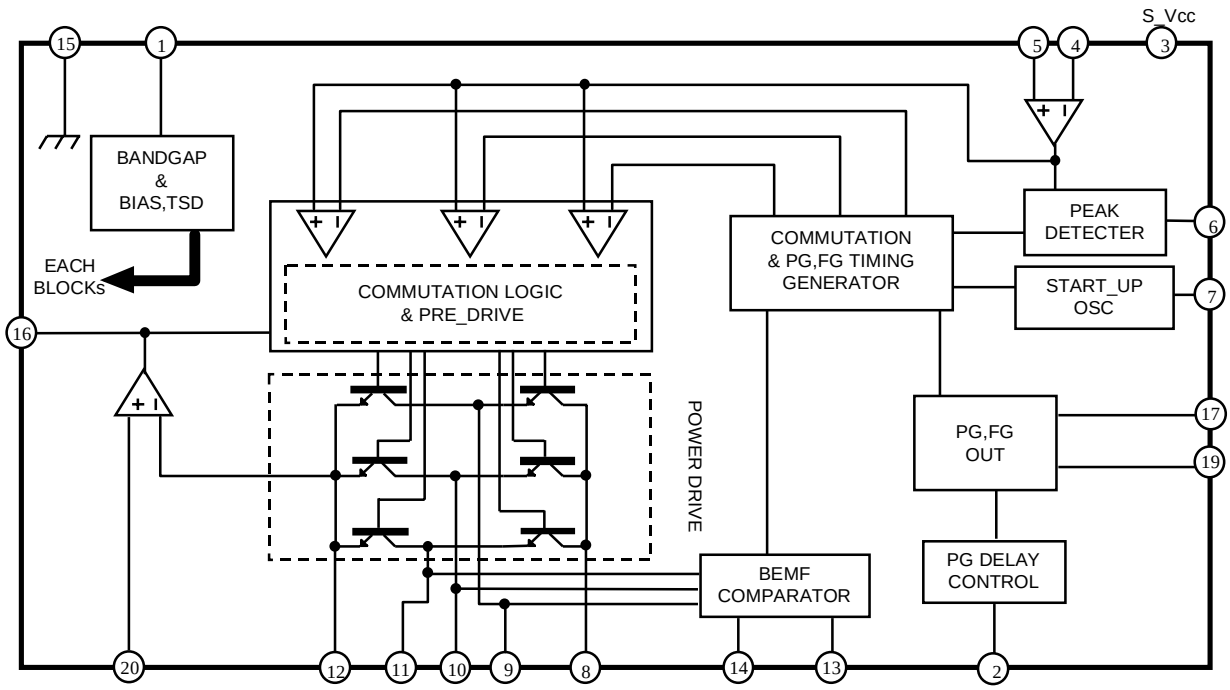
FEATURES

- Commutation FG, PG is executed by 1-Hall
- Soft switching at output terminal reduces swiching impulse
- 3-phase full wave
- Voltage Reference(uses Band Gap Circuit)
- Built-in Thermal Shut-Down(TSD) Circuit

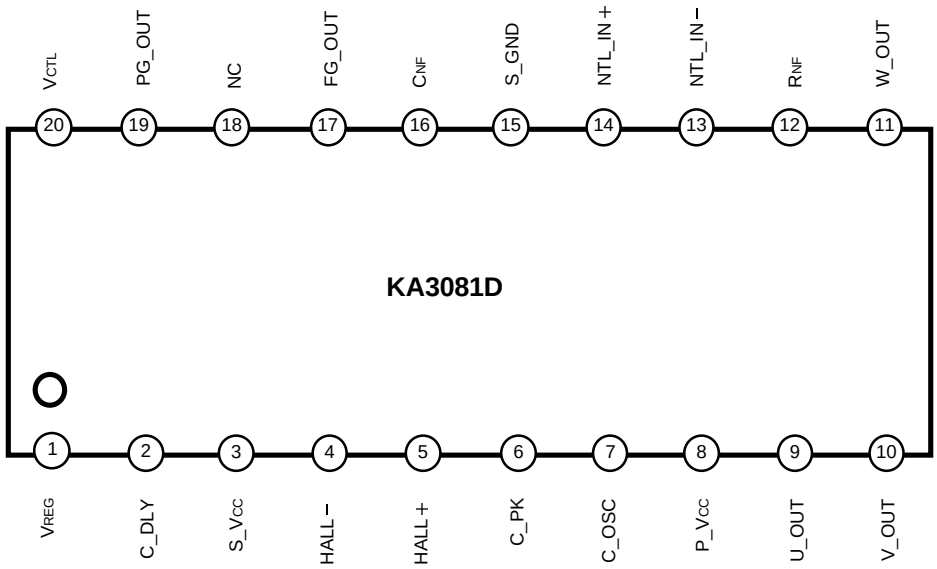
ORDERING INFORMATION

Device	Package	Operating Temperature
KA3081D	20-SOP-300	- 20°C ~ + 75°C

BLOCK DIAGRAMS



PIN CONFIGURATIONS



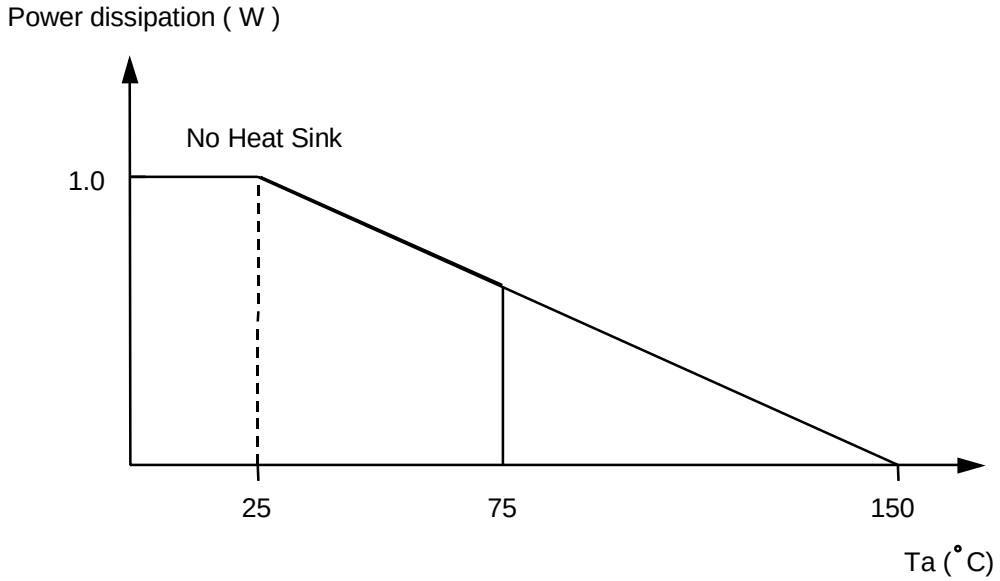
PIN DESCRIPTIONS

Pin no.	Symbol	Description	Pin no.	Symbol	Description
1	V_{REG}	Regurator Output	11	W_OUT	W-phase Output
2	C_DLY	PG. Delay	12	R_{NF}	Output Current Censing
3	S_V_{CC}	Signal V_{CC}	13	NTL_IN-	Input from The Neutral Point of The Motor Coils.
4	HALL-	HALL - Input	14	NTL_IN+	Input from The Neutral Point of The Motor Coils.
5	HALL+	HALL+ Input	15	S_GND	Signal Ground
6	C_PK	Peak Detector of Hall Signal	16	C_{NF}	Phase Compensation
7	C_OSC	Start-up Oscillator	17	FG_OUT	FG.Output
8	P_V_{CC}	Power V_{CC}	18	NC	--
9	U_OUT	U-phase Output	19	PG_OUT	PG.Output
10	V_OUT	V-phase Output	20	V_{CTL}	Output Current Control

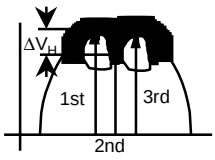
ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristics	Symbol	Value	Unit	Remark
Supply Voltage(Signal)	V_{CC}	20	V	---
Output Current	I_{OMAX}	1.0	A/phase	
Regulator Output Current	I_{REGMAX}	10	mA	
Power Dissipation	P_D	1.0	W	No Heat Sink
Junction Temperature	T_j	150	°C	---
Operating Temperature	T_{OPR}	- 20 ~ + 75	°C	Ambient Temperature(Ta)
Storage Temperature	T_{STG}	- 40 ~ + 155	°C	

POWER DISSIPATION CURVE



ELECTRICAL CHARACTERISTICS (Measured in test circuit ; Vcc=12V, Ta = 25°C)

Characteristics	Symbol	Test Conditions	Min	Typ	Max	Unit
TOTAL						
Supply Voltage	V_{CC}		8.0	--	18	V
Supply Current(1)	I_{CC1}	V_{CC}=12V,V_{REG}=open,V_{CTL}=0V	--	11.2	17	mA
Supply Current(2)	I_{CC2}	V_{CC}=18V,V_{REG}=open,V_{CTL}=0V	--	11.5	17	mA
REGURATOR						
VREG Output Voltage(2)	V_{REG2}	V_{CC}=12V,I_{REG}=0mA	4.7	5.0	5.3	V
VREG Output Voltage(5)	V_{REG5}	V_{CC}=12V,I_{REG}=10mA	4.7	5.0	5.3	V
START-UP OSCILLATOR						
C_OSC Operation Frequency	OSC_{FEQ}	C_OSC=47nF	6	8	10	Hz
C_OSC Charging Current	$OSC_{\_ICH}$	C_OSC=47nF	-0.5	-2	-3.5	uA
C_OSC Discharging Current	$OSC_{\_IDC}$	C_OSC=47nF	1	3	5	uA
C_OSC Low Threshold Voltage	$OSC_{\_THL}$	C_OSC=47nF	0.2	0.5	0.8	V
C_OSC High Threshold Voltage	$OSC_{\_THH}$	C_OSC=47nF	2.7	3.0	3.3	V
VOLTAGE CONTROL						
VCTL Start Voltage	$VCTL_{\_ST}$	V_{CTL}=0~2V When I_O=25mA	1.01	1.26	1.51	V
VCTL Input Voltage Range	$VCTL_{\_IN}$	V_{REG}	0	--	V_{REG}	V
VCTL Input Bias Current	$VCTL_{\_BI}$	V_{CTL}=2.0V	--	1.0	1.5	uA
Gain	GM	R_{NF}=0.47Ω,V_{CTL}=0~2V	0.38	0.45	0.52	A/V
HALL INPUT						
*Input Hall signal MIN.Voltage	V_{H_MIN}		300	--	--	mVp-p
*PG Hall 1'st MIN.Voltage	V_{H_P1}		60	--	--	mVp-p
*PG Hall 2'nd MIN.Voltage	V_{H_P2}		55	--	--	mVp-p
*PG Hall 3'rd MIN.Voltage	V_{H_P3}		75	--	--	mVp-p
*PG Hall 1'st-2'nd Level	ΔV_H		5	--	--	mVp-p
FG(Frequency Generator), PG(Phase Generator)						
FG,PG High Level	$FG\_PG_{\_H}$	--	4.5	--	--	V
FG,PG Low Level	$FG\_PG_{\_L}$	--	--	--	0.5	V

ELECTRICAL CHARACTERISTICS (Measured in test circuit ; V_{CC}=14V, Ta = 25°C)

Characteristics	Symbol	Test Conditions	Min	Typ	Max	Unit
TDS						
*Temp. Threshold	$TSD_{\_T}$	--	130	150	--	°C
*Temp. Hysteresis	$TSD_{\_H}$	--	20	30	--	°C
OUTPUT						
Output Saturation Voltage(Upper)	V_{SU1}	V_{CTL}=4V,I_O=600mA,R_{NF}=0.47Ω	--	1.0	1.5	V
Output Saturation Voltage(Under)	V_{SD1}	R_L=10Ω	--	0.4	0.7	V
NTL_IN - Input Voltage Range	V_{NTL_IN-}	--	0	--	V_{CC}	V
CNF. Voltage	V_{CNF}	V_{CTL}=2V	1	--	--	V
C_PK Frequency	$CPK_{\_FRQ}$	C_PK=100Ω+0.1uF	0.8	1	1.2	KHz
C_PK Voltage Level	CPK_v	C_PK=100Ω+0.1uF HALL-=0.25V	0.4	--	--	Vp-p
C_DLY						
C_DLY Charging Current	I_{C_DLY}	C_DLY=6nF	-20	-30	-40	uA

Note : The mark, * , in the chart means items calculated and approved in design not the items proven by actual test results.

APPLICATION INFOMATION

1. ORGANIZATION OF SYSTEM

The figure 1-1 shows concept of soft switching for 3-phase output with a hall sensor.

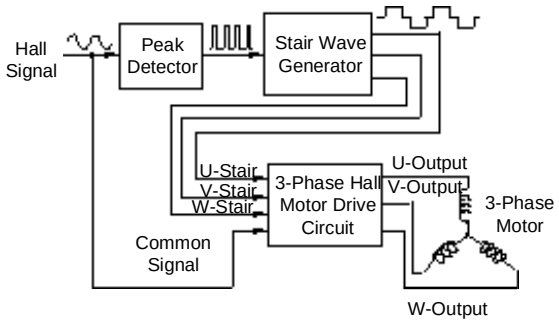


Figure 1-1

(1) Peak Detector
Gets hall signals from hall sensor and generates clock pulses from the peak points of the hall signal.
(2) Stair Wave Generator
Generates 3 stair wave signals with 120 degree different wave angles out of the clock pulses made from the peak detector.
(3) 3-Phase Motor Drive Circuit
Controls output currents to operate 3-phase motor using the voltage difference between the 3 stair wave signals and FG hall signal. It's circuit for switching.

2. STRUCTURE OF BLDC.MOTOR

Sub-magnet takes hall signal and go through 6 gradual wave filtering steps purifying) in order to operate 3-phase motor with one hall. For wave purification, the ratio between main-magnet and sub-magnet should maintain 1 main versus 3 subs as shown in the figure 2-1.

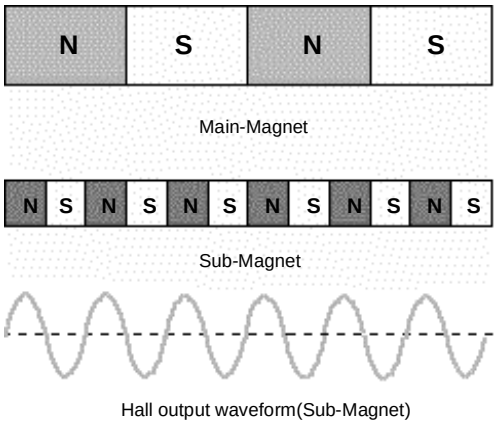
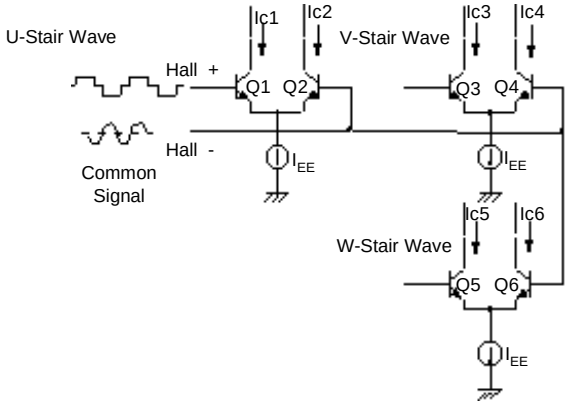


Figure 2-1

3. PRINCIPLE OF OPERATION

Input circuit of 3-phase motor drive with soft-switching function is shown as the figure 3-1.



* Hall- : Hall Common Signal taken from sub-magnet.
* Hall+ : Stairwave signal with 120 degree wave angle difference from one hall signal.

Figure 3-1

Next the figure 3-2 shows Common signal(Hall signal) and each individual Stairwave at its own position.

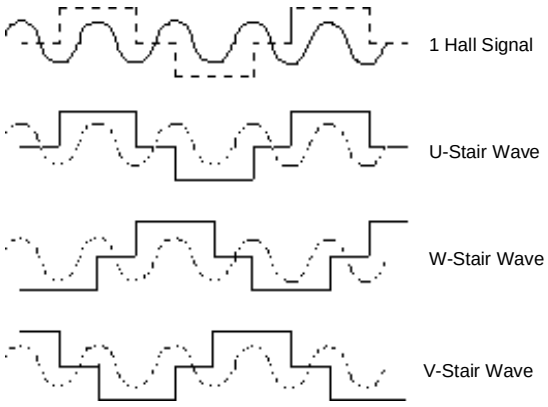
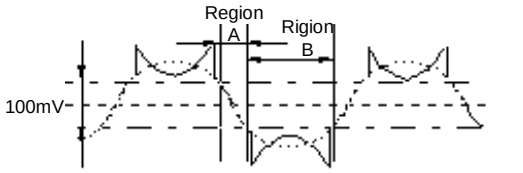
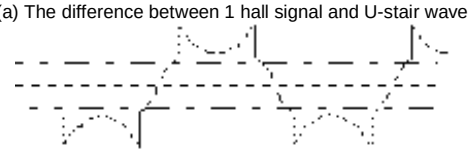


Figure 3-2

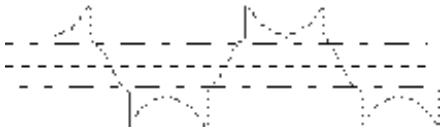
And the figure 3-3 shows Hall signal and the difference of each Stairwave at its position.
The section where the difference between hall signal and Stairwave is within 100mV referring to hall bias shows the same as 3-phase motor drive with 3 halls in the figure 3-3.
The other sections keep constant state regardless of hall signal size because output current is controled by current source in input terminal the figure 3-1.



(a) The difference between 1 hall signal and U-stair wave



(b) The difference between 1 hall signal and V-stair wave



(c) The difference between 1 hall signal and W-stair wave

Figure 3-3

4. PEAK DETECTOR

The signals used to operate motor are hall signals and stairwave made from peak detectors's output.
The peak detecter is constructed with the following circuit (the figure 4-1).

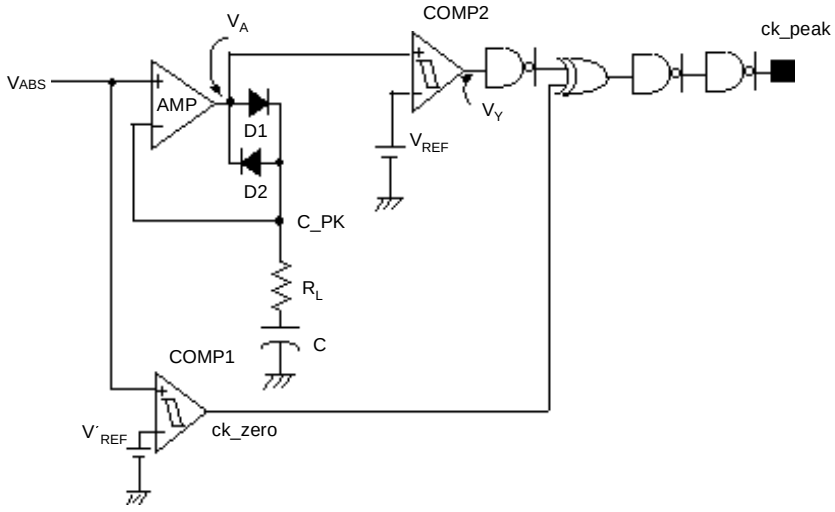


Figure 4-1

V_{ABS} in the figure4-1 is a signal from twice amplified hall signal and hall bias at 2.5volt as standard voltage as you see in the figure 4-2.

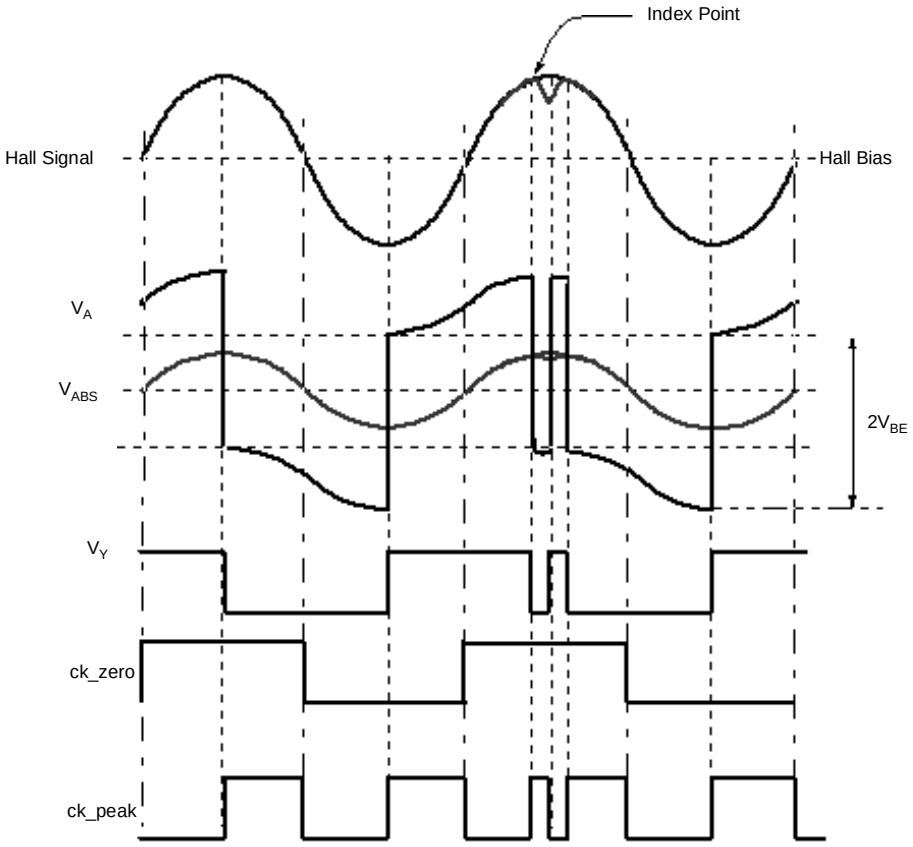


Figure 4-2

V_{ABS} goes into COMP1 and AMP after that. Zero-Crossing is done to the V_{ABS} signal into COMP1 to output ck-zero wave seen in the figure 4-2. And V_{ABS} signals into AMP comes out as Va signal by following mechanism (1), (2) and (3).

(1) When V_{ABS} increases from the lowest point to highest point.
C-PK follows V_{ABS}'s shape by R_L and C and become charged. AMP outputs the same way.
(2) When V_{ABS} decreases from the highest points.
C-PK remains maximum status with no discharge path is available while D1 and D2 are off until the voltage difference with V_{ABS} is more than offset of AMP. Then, V_A which is output of AMP become deceased. When there is voltage difference more than 0.7V between Va and C-PK, D2 will be on to decease C-PK through emission from C as the same way as V_{ABS} signal. That time, V_A has the shape of V_{ABS} and outputs.
(3) When V_{ABS} increases from the lower to highest point.
C-PK remains its minimum status while V_{ABS} is increasing due to D1 is off. When the voltage difference between C-PK and V_{ABS} is bigger than offset of AMP, V_A which is output of AMP increases. When the voltage difference between V_A and C-PK is more than 0.7V, D1 will be on and discharge from C increases C-PK which will follow the same shape as V_{ABS}. That time V_A with the same shape as V_{ABS} outputs. The final output ck-peak signal is made by outputs of COMP1 and COMP2.

5. checking the index sign

Reversed embodied magnet(magnet with opposite polaris)is needed for sub-magnet to detect motor's index point as the hall signal shown in the figure 4-2.
The peak detector output from compounded magnet generates 2 clock pulses in half cycle.
The first clock pulse is used for filter motor's pulse wave and the other is used as index signal.
The index signal checks commutation of motor once for each rotation and offer reference point for data checking.

6. Drive output

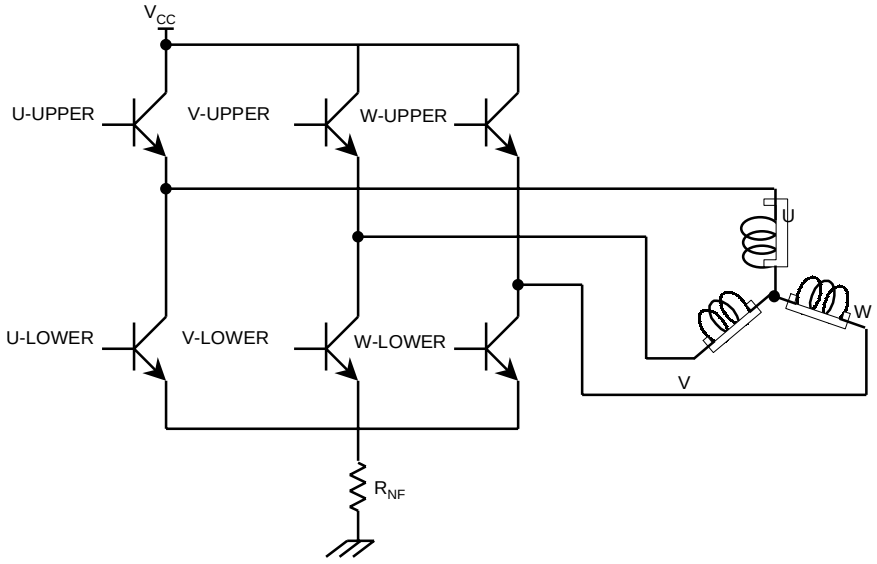


Figure 6-1

The figure 6-1 shows the 3-phase mechanism. When one phase of of upper power TR is on, 1 phase of the other lower TR becomes on and the rest power TR becomes off. This is the way to continuing commutation to right direction to operate motor.
The upper power TRs in output group operate in linear area and the lower group work in saturation area.

7. Voltage control & Current sensing

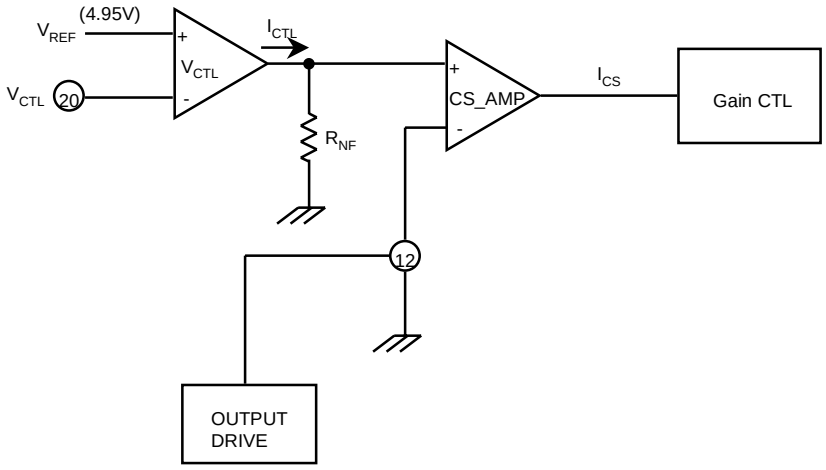


Figure 7-1

The circuit in the figure 7-1 is to outputting I_{CTL} current when V_{CTL}(control voltage from SERVO) becomes bigger than the value of V_{REF}. The V-I characteristic of this circuit is shown in the figure 7-2

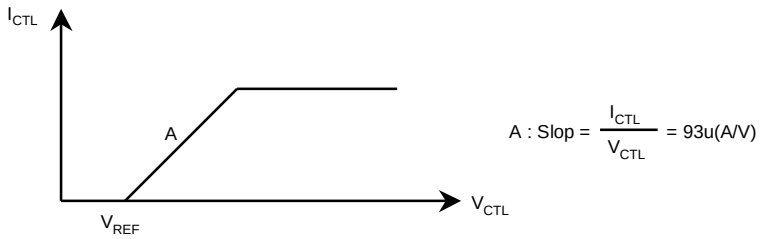


Figure 7-2

The CS-AMP terminal amplifies by getting inputs from output terminal getting I_{CTL} and R_{NF} voltages. R_{NF} resistance feedbacks the current in output terminal.

8. SHIFTOR

The function of this circuit is to delay PG signal generated by FGPG generator using PIN2(C_DLY) aqs shown in the figure 8-1.

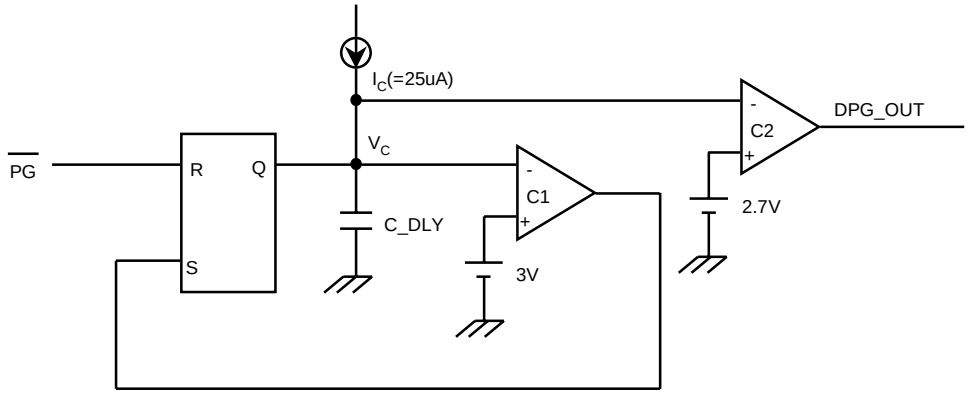


Figure 8-1

The figure 8-2 shows the output wave shapes in each block of the circuit in the figure 8-1.

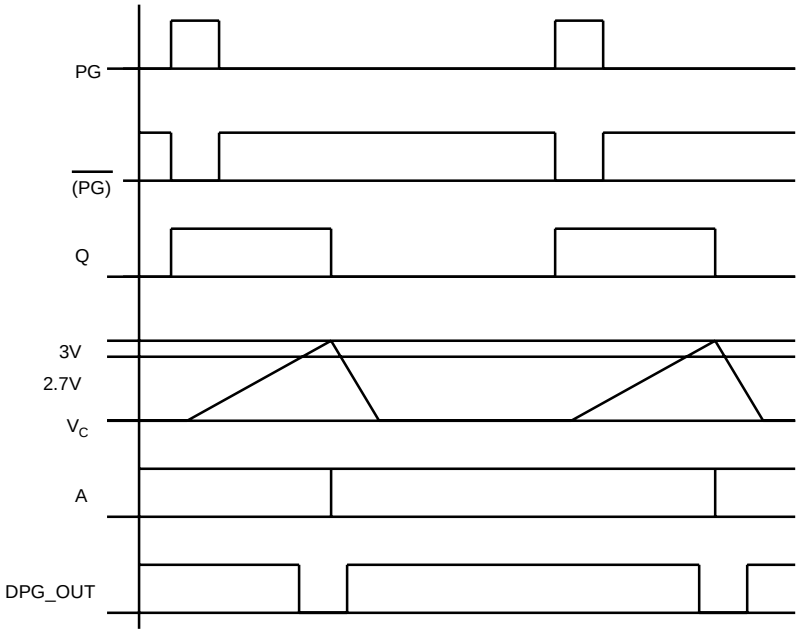
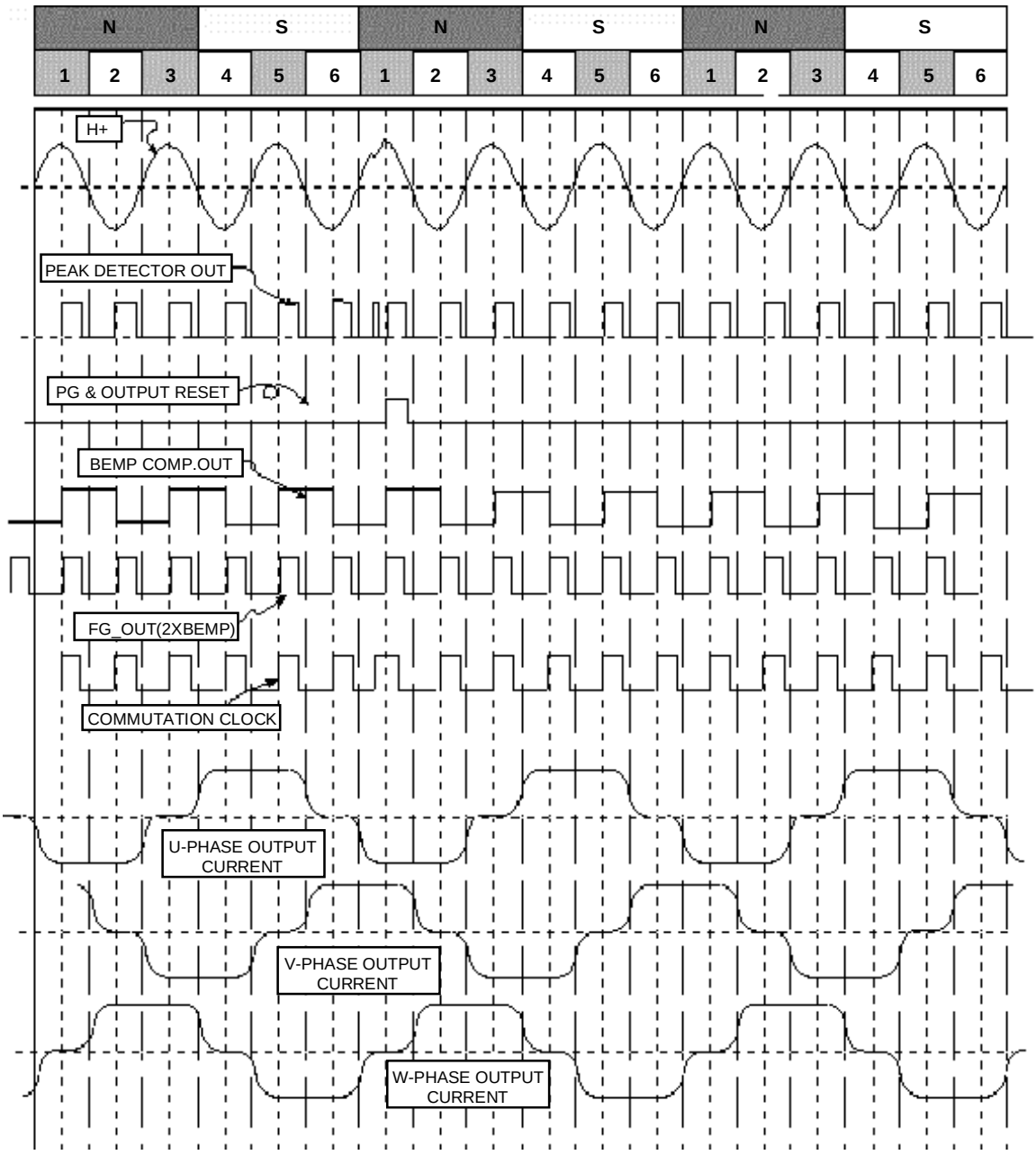
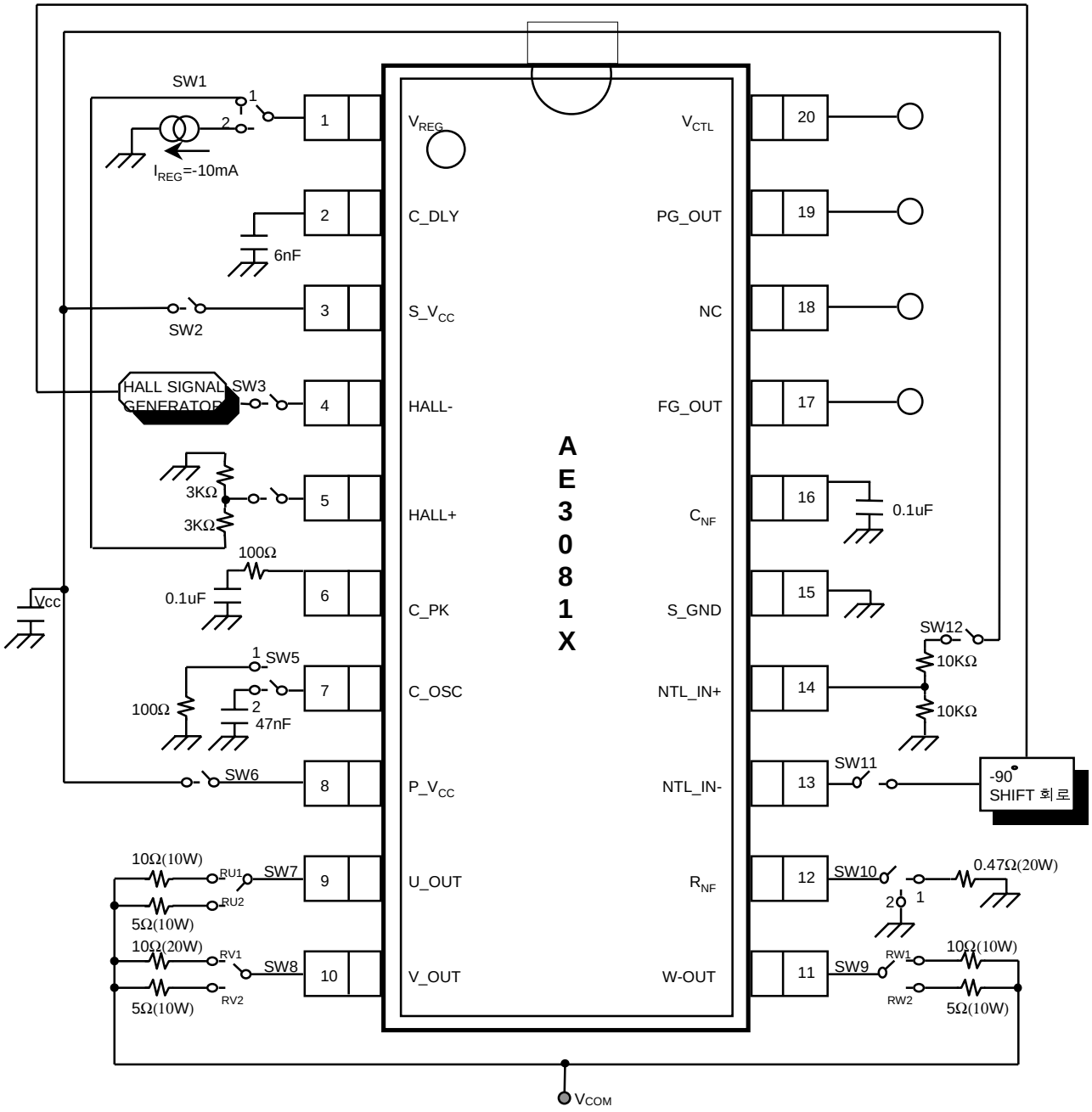


Figure 8-2

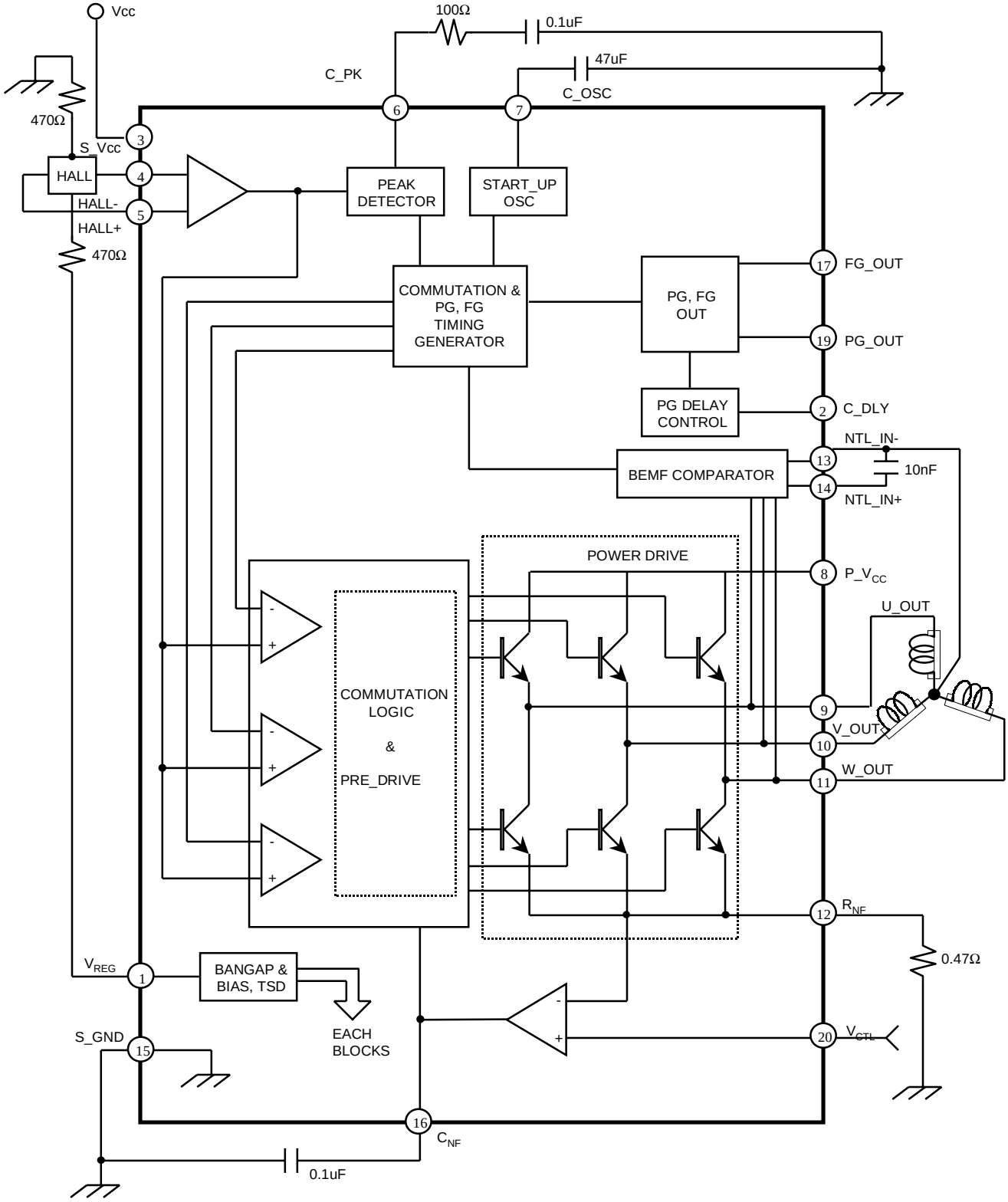
TIMING CHART



TEST CIRCUITS



TYPICAL APPLICATIONS



PACKAGE DIMENSIONS (Unit : mm)

20 - SOP - 300