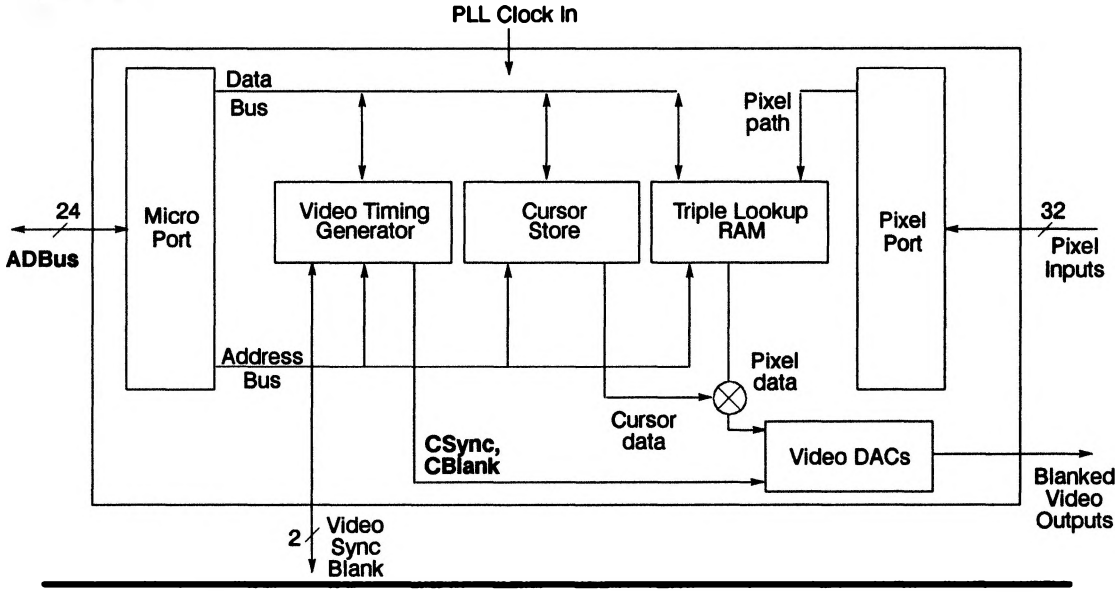
IMS G332
colour video controller

inmos®

Preliminary data



FEATURES

Video rates up to 110 MHz, (135MHz available 1991)
Software configurable video timing generator
64×64×3 colour hardware cursor
Interlaced or non-interlaced video
Generates Studio broadcast standard Sync signals
Supplies blanked analogue video outputs
Internal or external Sync options
Single or synchronous multiple operation

Variable multiplexed pixel input
1, 2, 4 and 8 bit pseudo colour pixels
15 or 16 bits per pixel gamma corrected colour
On chip triple lookup table with anti-sparkle
Triple high speed 8 bit video DACs
CCIR and EIA 343-A compatible

General purpose Video RAM support
Synchronous VRAM Data Transfer strobing
Video RAM Row address auto-increment
Screen width independent of VRAM architecture
On-chip phase-locked loop (PLL)

APPLICATIONS

General purpose raster scan control
CRT Screen control
Colour plotters and printers
Plane-based workstations
Portable personal computers

Three dimensional modelling
Real time animation systems
Computer visualisation
Multiple processor systems
Frame swapping systems
Scene insertion into live camera data

Distributed computing environments

7.1 Introduction

The IMS G332 provides all the necessary functions to control real-time operation of a raster scan video display, using dual-ported video RAMs.

The device consists of a 32 bit variable multiplexed pixel interface, a programmable video timing generator (VTG), a 256 location colour lookup RAM (LUT) with variable addressing modes, triple 8 bit video DACs, a 64×64×2 bit cursor store and 3 location cursor LUT, a programmable cursor positioning/insertion controller, a video memory control system and phase-locked loop clock generator.

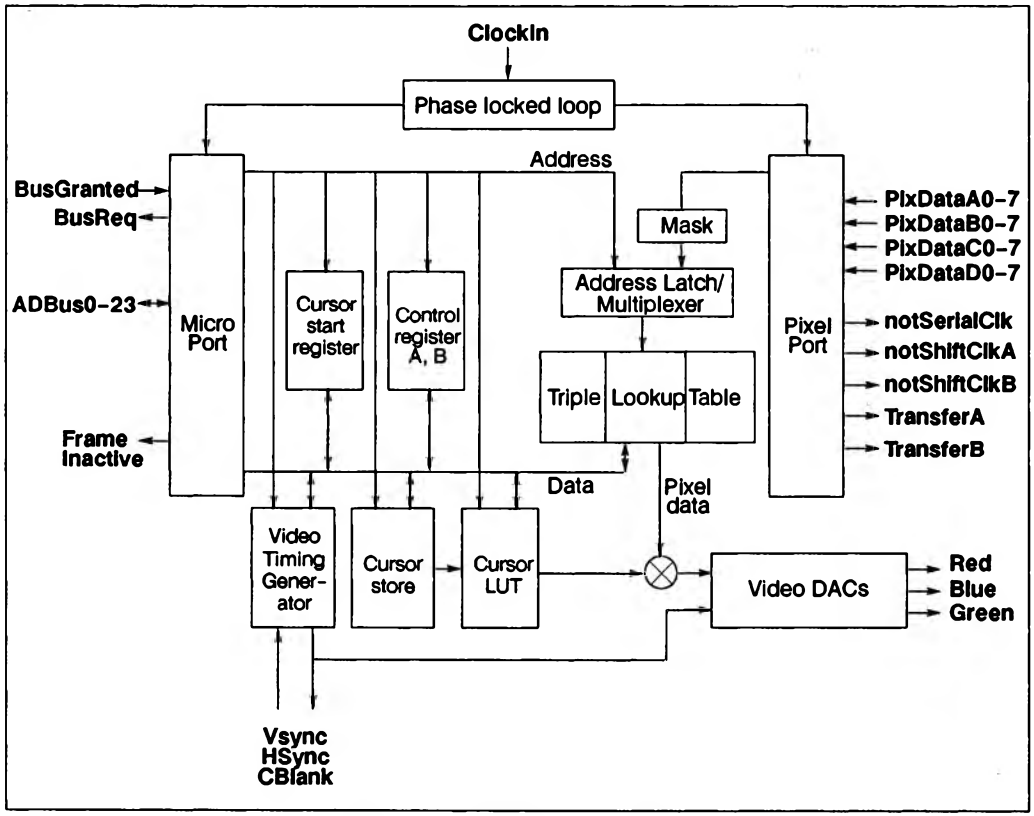


Figure 7.1 IMS G332 Block Diagram

7.2 Pin function reference guide

7.2.1 Micro port

Pin name	I/O	Page No.	Comments
FrameInactive	O	158	Timing signal which is high during vertical blanking.
BusReq **BusGranted**	O I	157	DMA control signals used in conjunction with **TransferA** and **TransferB** when refreshing the VRAM shift registers.
ReadnotWrite **notOutputEnable** **notChipSelect** **Wait**	I I I O	156	Microport control signals. Wait is used to extend cycle times if necessary.
ADBus0-23	I/O	156	Multiplexed address and data bus. All 24 bits are used for data; addresses are supplied either on **ADBus2-11** or on **ADBus3-12** depending on the word width.The port is also used to drive out the 24 bit VRAM transfer address.

7.2.2 Pixel port

Pin name	I/O	Page No.	Comments
notSerialClk	O	159	**notSerialClk** runs at one quarter the video frequency. This signal must be buffered
notShiftClkA **notShiftClkB**	O O	159	VRAM clocks running under the control of the timing generator. The clocks run in anti-phase in interleaved mode; only **notShiftClkA** runs in non-interleaved mode. These clocks must be buffered.
TransferA **TransferB**	O O	157	VRAM shift register transfer strobes. TransferA and B are synchronised to **notShiftClkA** and **notShiftClkB** respectively.
CBlank	I/O	150	**CBlank** is a composite blanking pin. Direction is soft selectable.
PixDataA0-7 **PixDataB0-7** **PixDataC0-7** **PixDataD0-7**	I I I I	159	Pixel input ports A – D. Port A is least significant; port D is most significant. Internally, pixel data is latched synchronous to **notSerialClk.**

7.2.3 Miscellaneous

Pin name	I/O	Page No.	Comments
Reset	I	154	Active high, must be held active with clocks running for at least 500ns.

7.3 Phase locked loop

Pin name	I/O	Page No.	Comments
CapPlus **CapMinus**	N/A	162	Phase locked loop decoupling pins, also used to select external dot rate clock source by connecting **CapPlus** to **CapMinus**.
ClockIn	I	162	Clock input for both PLL and times-one operation.

7.3.1 Video signals

Pin name	I/O	Page No.	Comments
Red **Green** **Blue**	O O O	159, 163	Blanked video outputs. Drive into doubly terminated 75Ω load.
Iref	I	163	Video DAC reference current.
notVSync **notCorHSync**	I/O I/O	155	Digital sync signals for system synchronisation. They are inputs in slave mode and outputs in master mode. They are soft configurable.

7.3.2 Supplies

Pin name	I/O	Page No.	Comments
AVDD **AGND**	N/A N/A	164	**AVDD/AGND** supplies analogue portions of chip.
VDD **GND**	N/A N/A	164	**VDD/GND** supplies digital portions of chip.

7.4 Register function reference guide

Register	Address	Page No.	Comments
Boot Location	#X000	146	Startup location to which must be written the clock multiplication factor, whether PLL or ×1 mode, and the 32/64 bit address alignment selection.
Datapath Registers	#X021 to #X02E	144	Read/write registers containing the screen description parameters. These are accessible only when the timing generator is not running.
Mask Register	#X040	160	24 bit pixel address mask register. Read/write accessible at all times. (Operates only on pseudo colour pixels)
Control Registers	#X060 and #X070	145	Read/write control registers contains configuration information. Unassigned bits must be written with zero and are not valid on read. Read/write accessible at all times.
Top of Screen	#X080		Read/write register giving ability to reprogram the top of screen pointer at any time.
Cursor palette	#X0A1 to #X0A3	161	3×24 bit cursor colour registers. Read or write accessible at all times.
Checksum registers	#X0C0 to #X0C2	161	RGB frame checksums.
Colour Palette	#X100 to #X1FF	160	256 locations of 24 bit colours read/write accessible at all times.
Cursor store	#X200 to #X3FF	161	512 locations of 16 bit words, each containing 8 packed 2-bit pixel colour values.
Cursor position	#X0C7	161	24 bit register storing the x-y position of the cursor.

All other addresses in the range are reserved and must not be written to.

Note: #X = Hexadecimal address.

Word addresses are user-selectable to align with 64-bit or 32-bit words. In 32 bit mode, addresses must be supplied on **ADBus2-11**; in 64 bit mode they must be supplied on **ADBus3-12**. The addresses given above must be multiplied by the appropriate scale factor (4 in 32 bit mode, 8 in 64 bit mode) to obtain the corresponding byte addresses.

7.5 Datapath register allocation

Register	Address	Units	Notes
Half sync	#X021	Screen units	1
Back porch	#X022	Screen units	
Display	#X023	Screen units	
ShortDisplay	#X024	Screen units	
BroadPulse	#X025	Screen units	
VSync	#X026	Half lines	
VPreEqualise	#X027	Half lines	
VPostEqualise	#X028	Half lines	
VBlank	#X029	Half lines	
VDisplay	#X02A	Half lines	
LineTime	#X02B	Screen units	
Line Start	#X02C	Screen units	
MemInit	#X02D	Screen units	
TransferDelay	#X02E	Screen units	2

Notes

1 1 screen unit = 4 pixels horizontally = 1 Serial Clock period.

2 Transfer Delay equates to a real time, and the value will therefore depend on the serial clock period.

7.6 The control registers and boot location

There is provision for two 24-bit control registers, one of which is initially populated.

Bit	Function	Comments
0	Enable VTG	0 = VTG disabled 1 = VTG enabled
1	Screen format	0 = non-interlaced 1 = interlaced
2	Interlace standard	0 = EIA format 1 = CCIR format
3	Operating mode	0 = master mode 1 = slave mode
4	Frame flyback pattern	0 = tesselated sync 1 = plain sync
5	Digital sync format	0 = composite sync 1 = separate sync
6	Analogue video format	0 = composite video + sync 1 = video only
7	Blank level	0 = no blank pedestal 1 = blanking pedestal
8	Blank I/O	0 = CBlank is input 1 = CBlank is output
9	Blank function switch	0 = delayed CBlank at pad 1 = Undelayed ClkDisable, at pad
10	Force blanking (irrespective of bit 11)	0 = no action 1 = screen blanked
11	Turn off blanking	0 = blanking enabled 1 = blanking disabled
12-13	VRAM address increment	see definition (section 7.10.5)
14	Turn off DMA	0 = DMAs enabled 1 = DMAs disabled
15-17	Sync delay	Delays sync and blank by 0 - 7 VTG clock cycles
18	Pixel port interleaving	0 = non-interleaved 1 = interleaved
19	Delayed sampling	see definition (section 7.11.2)
20-22	Bits per pixel	see definition (section 7.11.3)
23	Cursor disable	0 = cursor enabled 1 = cursor disabled

Table 7.1 Control register A bit allocations (Address #X060)

Bit	Function	Comments
0-23	All bits reserved	Write zero

Table 7.2 Control register B bit allocations (Address #X070)

Bit	Function	Comments
0–4	PLL multiplier	Binary coded PLL multiplication factor
5	Clock source select	0 = external (×1) clock 1 = PLL clock
6	Micro port address alignment	0 = 32 bit 1 = 64 bit
7–23	Reserved	Write zero

Table 7.3 Boot location bit allocations (Address #X000)

The boot location must be written on power-up before attempting to access any other locations from the micro port. The timing of this first cycle is asynchronous; the value substituted for the serial clock period in the timing parameters should be the minimum allowable for that device see table 7.8

7.7 Micro port timing reference guide

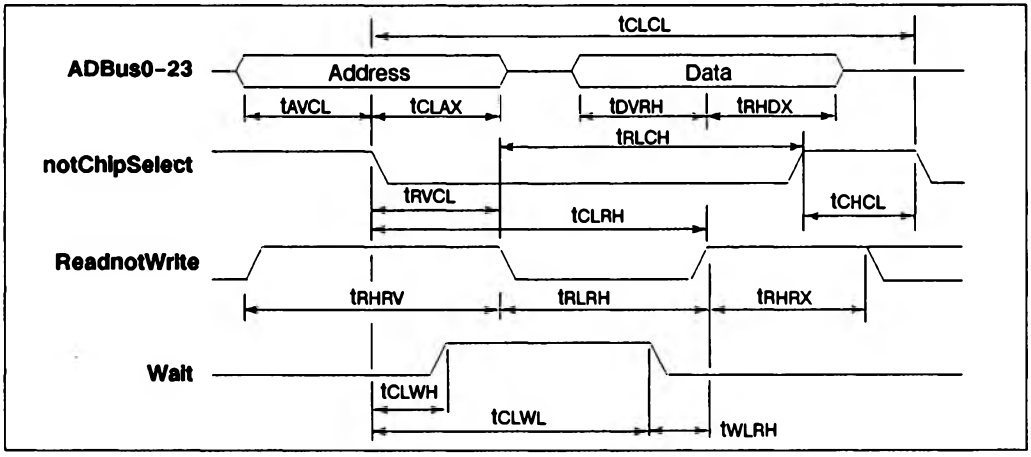


Figure 7.2 Micro port write cycle

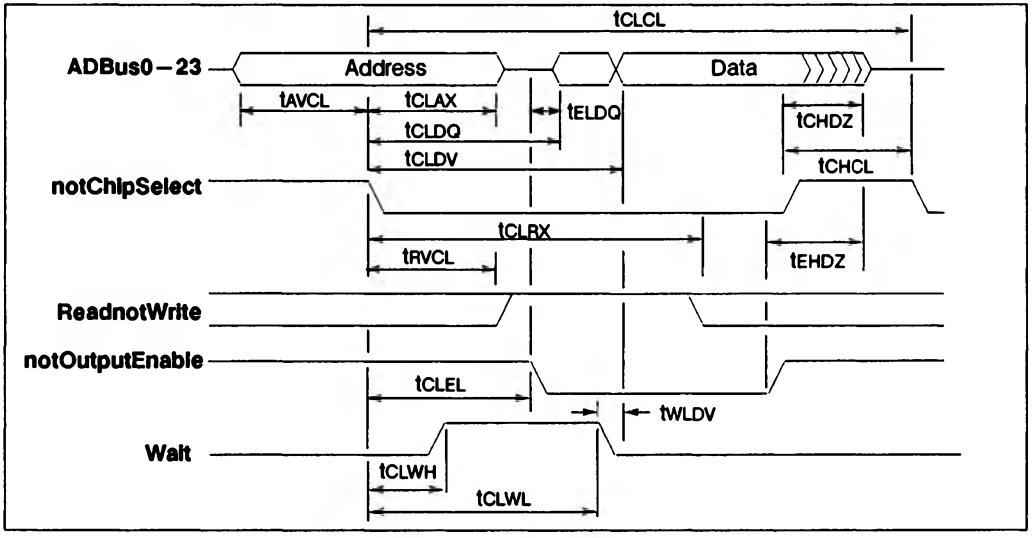


Figure 7.3 Micro port read cycle

Symbol	Description	Min.	Max.	Unit
tAVCL	Address setup time	20		ns
tCLAX	Address hold time	10		ns
tRVCL	**ReadnotWrite** setup time	-1		periods SClk
tCLRH	**ReadnotWrite** hold time	3		periods SClk
tRLRH	**ReadnotWrite** low time	2		periods SClk
tRLCH	**ReadnotWrite** low to **notChipSelect** high	2		periods SClk
tDVRH	Write data setup time	20		ns
tRHDX	Write data hold time	10		ns
tCLCL	Cycle time	4		periods SClk
tCLWH	**notChipSelect** low to wait high	0	20	ns
tCLWL	**notChipSelect** low to wait low	3		periods SClk
tWLRH	**ReadnotWrite** hold time	0		ns
tRHRX	**ReadnotWrite** high time	1		periods SClk
tCHCL	**notChipSelect** high time	2		periods SClk
Note: These figures are not characterised and are subject to change				

Table 7.4 Micro port write cycle parameters

Symbol	Description	Min.	Max.	Unit
tAVCL	Address setup time	20		ns
tCLAX	Address hold time	10		ns
tRVCL	**ReadnotWrite** setup time	-1		periods SClk
tCLRX	**ReadnotWrite** hold time	3		periods SClk
tCHDZ	Output hold time from **notChipSelect**	5	20	ns
tELDQ	Output turn on delay		20	ns
tEHDZ	Output hold time from **notOutputEnable**	5	20	ns
tCLEL	**notChipselect** to **OutptEnable** delay	20		ns
tCLDV	**notChipselect** access time		4 SClk + 10	ns
tCLCL	Cycle time	7		periods SClk
tCLWH	**notChipSelect** low to wait high	0	20	ns
tCLWL	**notChipSelect** low to wait low	4 SClk + 10		ns
tWLDV	Wait to data valid		10	ns
tCHCL	**notCS** high time	2		periods SClk
Note: These figures are not characterised and are subject to change				

Table 7.5 Micro port read cycle parameters

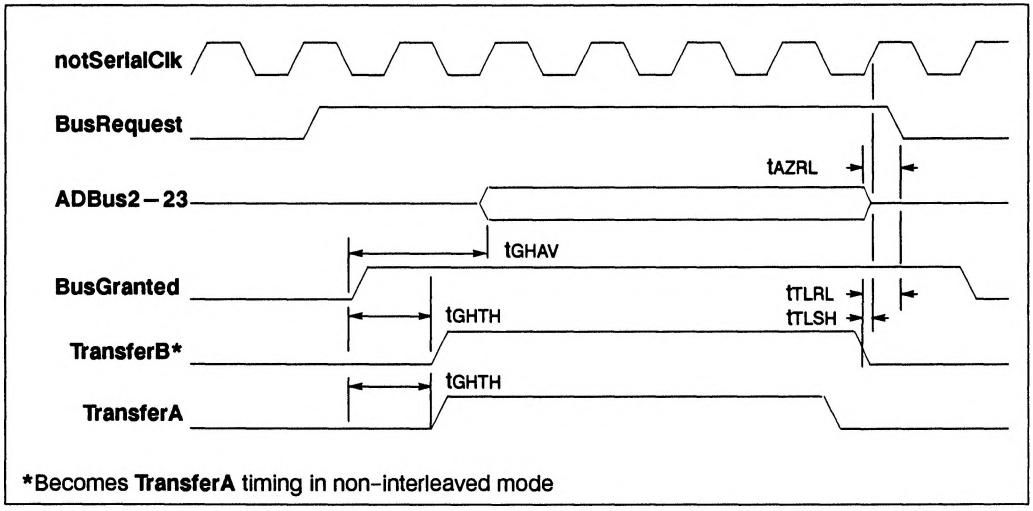


Figure 7.4 Micro port DMA and data transfer timings

Symbol	Description	Min.	Max.	Unit
tSHRH	**notSerialClk** to **BusRequest** skew	-5	5	ns
tGHTH	**BusGranted** high to **Transfer** high	15	30	ns
tGHAQ	**Transfer** address turn on delay	15		ns
tGHAV	**Transfer** address access time		4 SClk + 15	ns
tTLSH	**Transfer** to **notSerialClk** skew	-5	5	ns
tTLRL	**Transfer** to **BusRequest** low	1 SClk	1 SClk + 15	ns
tTLAZ	**Transfer** address hold time	0		ns
tRLCL	**BusRequest** low to **Chipselect** low	0		ns
tAZRL	Address hi-Z to **BusRequest** low	1 SClk-10		ns
Note: These figures are not characterised and are subject to change				

Table 7.6 Micro port DMA and transfer timing parameters

Symbol	Description	Min.	Max.	Unit
tΔSync	**VSync** to **CSync** skew	-5	5	ns
tΔASync	Digital **CSync** to analogue **CSync** skew	TBD	TBD	ns
tΔABlank	Digital **CBlank** to analogue **CBlank** skew	TBD	TBD	ns
Note: These figures are not characterised and are subject to change				

Table 7.7 Micro port **Sync** and **Blank** timing parameters

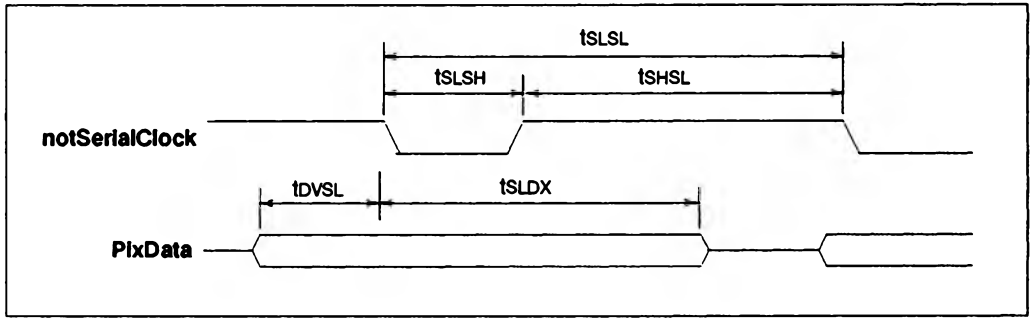


Figure 7.5 Pixel port timing diagram

Symbol	Description	-66	-85	-100	-110	Unit
tSLSL	**notSerialClk** period	61	47	40	36	ns
tSLSH	**notSerialClk** low time	10	10	10	10	ns
tSHSL	**notSerialClk** high time	10	10	10	10	ns
tDVSL	Data set up time	1	1	1	1	ns
tSLDX	Data hold time	9	9	9	9	ns
Note: These figures are not characterised and are subject to change						

Table 7.8 Pixel port timing parameters

7.8 Video Timing Generator

The Video Timing Generator is a programmable finite state machine. It provides composite sync and blanking to the on-chip video DACs, it controls the timing of **BusReq** and **TransferA/B** and it starts and stops **notShiftClkA/B** to control the flow of pixel data. It also provides **FrameInactive** which is asserted during frame flyback enabling the controlling processor to perform screen updates invisibly, and **CBlank** which is asserted during frame or line flyback.

The timing generator can be configured to control an interlaced or non -interlaced monitor, and to generate the synchronising waveforms required by the EIA-343 (NTSC) and CCIR (PAL) studio television standards. These options are selectable in software and are controlled by the contents of the control register. Also controlled by this register is the operating mode of the device. it can be set to free run, in which case it will drive the synchronising signals out, or it can be set into slave mode when it will lock onto externally supplied vertical and horizontal sync pulses.

Programming of the timing generator is achieved by writing a set of screen description parameters to the timing registers. Its resolution is one quarter that of the individual pixels hence the scan lines must be described in 'screen units' of four pixels each. (i.e. a line with 1024 pixels is described as having 256 screen units.)

7.8.1 The display screen

In a raster scan display system, the picture is built up of a number of visible lines, which are displayed and a much smaller number of frame flyback lines, which are blanked. Each of the displayed lines has a single, visible, display period and a blanked line flyback period made up of front and back porch plus line sync. The total linetime is the sum of the displayed and blanked periods.

The frame timing periods are specified in multiples of half a linetime while the line timings are specified in screen units of four pixels duration each.

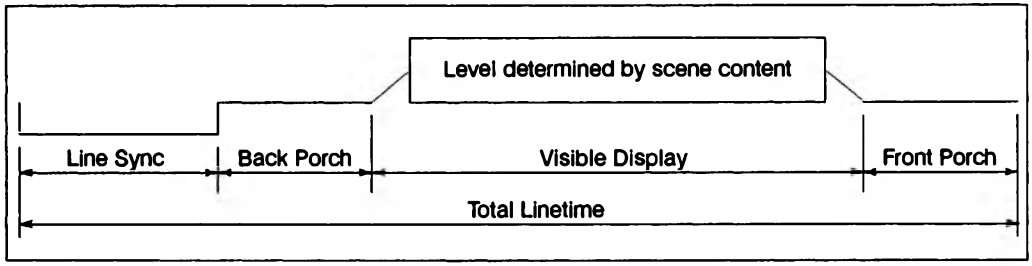


Figure 7.6 Scan line segments

Each displayed scan line of the raster is built up of the sections shown in figure 7.6. The visible portion is contained within the period 'display', so that, if a screen width of 1024 visible pixels (equal to 256 screen units) is required, then 256 is the number written to the 'display' register. For the remainder of the scan, the display is in line flyback and is therefore blanked.

The total linetime is the sum of all the sections of figure 7.6 and this is the number written to the 'linetime' register.

7.8.2 Line timing parameters

The line segments shown in figure 7.6 map directly to timing generator registers with two exceptions. First, the line synchronising pulse is split into two periods of equal duration which are used in immediate succession – the parameter used for this is 'halfsync' – and second, there is no register for frontporch, rather the total line time is programmed into a separate register and the end of the scan line occurs when this time-base period expires.

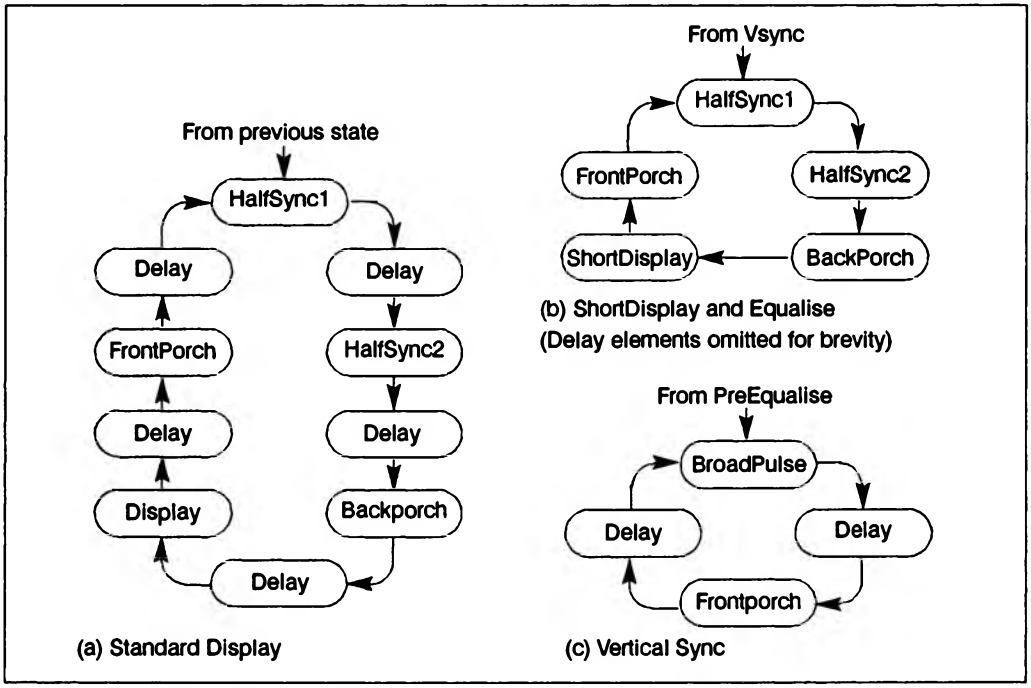


Figure 7.7 Flow diagrams for video timing generator

Figure 7.7 (a) shows the flowchart of a standard displayed or blanked scan line (as distinct from the truncated unscanned lines used in vertical sync and equalisation). The state machine proceeds from one state

to the next according to the delay programmed in by the user; on entering a new state the Sync and blanking outputs are modified depending on which part of the cycle is being executed.

Figure 7.8 (a) shows the relationship of the screen description parameters to a full scan line. Note that front-porch is undefined and halfsync is used twice in succession to construct the line sync pulse.

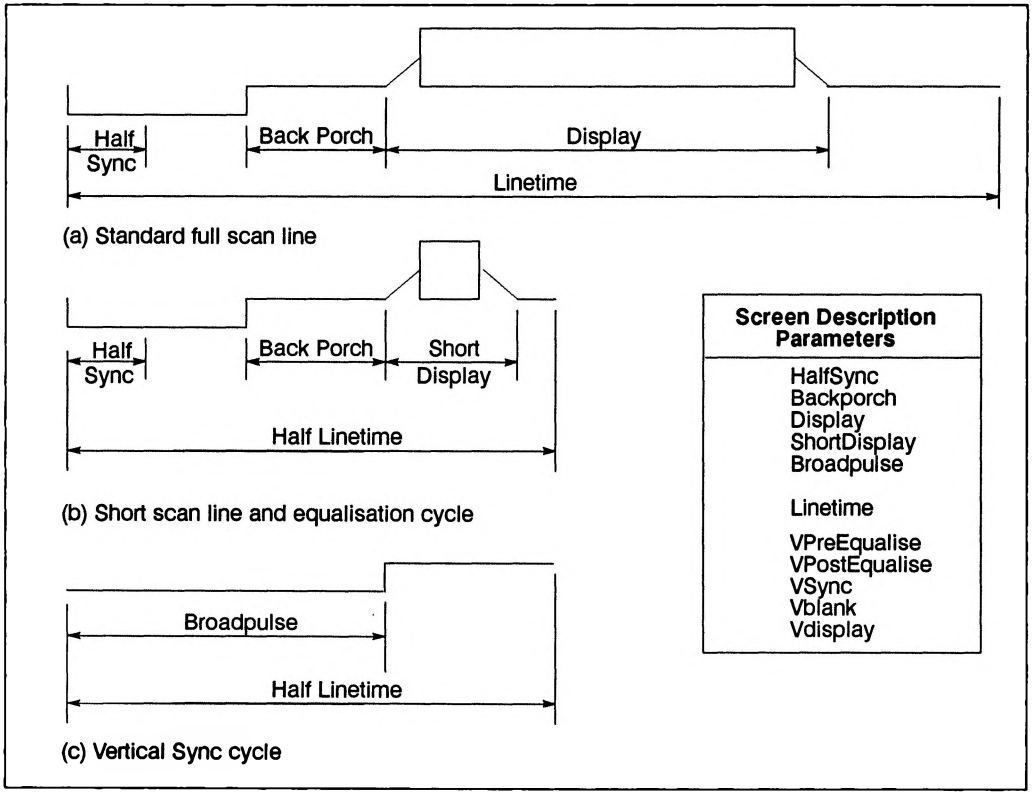


Figure 7.8 Screen description parameter definitions

7.8.3 Frame timing parameters

The G332 generates synchronising signal timings and levels conforming to both broadcast and closed circuit television standards. This means that, as well as being capable of generating the ordinary frame sync patterns associated with non-interlaced computer graphics systems, it is also able to produce tesselated sync signals for an interlaced television system (see figure 7.9).

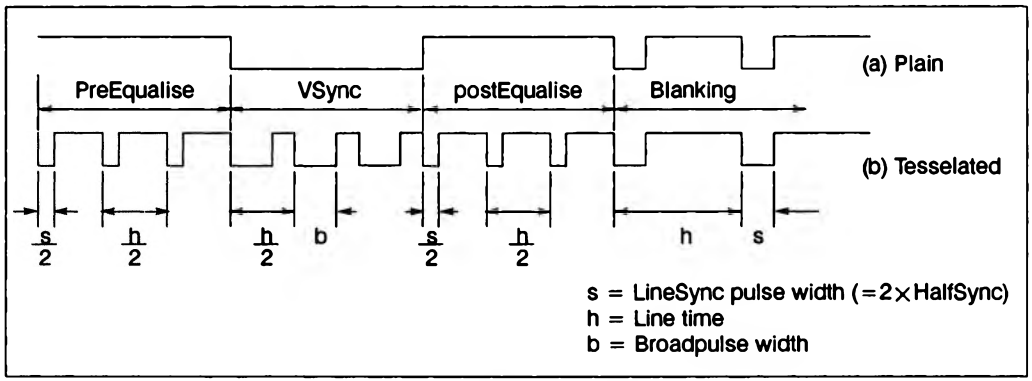


Figure 7.9 Composite Sync frame flyback waveforms

A further requirement of the television standards is that each frame must contain an odd number of scan lines. As a result, the frame timing parameters need to be specified in terms of half line times. Thus a non-interlaced screen of 1024 visible lines has the value 2048 written to the VDisplay register. (An interlaced screen of 625 lines would have 625 in that register since in interlace, the VDisplay register decribes the vertical display *field* rather than the entire frame – see table 7.9).

Screen Type	Lines per Frame	Value in VDisplay Register	Lines per Field
non-interlace	1024	2048	1024
interlace	1024	illegal	illegal
non-interlace	625	1250	625
interlace	625	625	312.5

Table 7.9 Frame programming examples

The duration of preEqualise, postEqualise, VSync and VBlank are also defined as multiples of half lines. The total frame blanking period is the sum of these four.

In order to generate the tesselated equalisation and blanking waveforms shown in figure 7.9(b), some additions to the basic line parameters are needed. The low period during VSync is defined as 'broadpulse' with its duration stored in the 'broadpulse' register. The shorter low period during pre and post equalisation is equal to half the line sync period and hence uses the value stored in the 'halfsync' register.

Reference to figure 7.7(b) and (c) shows that, on entering frame flyback, the state machine loop shortens to give a period of half a linetime. In equalisation, this is achieved simply by substituting 'shortdisplay' for 'display' in the sequence, whereas in vsync the sequence is changed to include only 'broadpulse' and 'frontporch'.

7.8.4 Parameter calculation

Calculation of the frame timing parameters is simple and direct – to produce the flyback waveform in figure 7.9(a) the parameters VSync, preEqualise and postEqualise are set to 3 – and the line parameters are derived from the equations in table 7.10.

During a full line cycle (VBlank, VDisplay)		
Halfsync	=	Horizontal Sync/2
BackPorch	=	BackPorch
Display	=	Display
Linetime	>	(2×HalfSync + BackPorch + Display)
During an equalisation cycle		
ShortDisplay	<	Linetime/2 – (2×HalfSync + BackPorch)
Low period	=	HalfSync
High period	=	Linetime/2 - HalfSync
During a VSync cycle		
BroadPulse	=	Linetime/2 - Pulse width*
Low Period	=	BroadPulse
High period	=	Pulse width

Table 7.10 Screen description line parameter equations

* Note: Pulse width = duration of serration pulse high time

The following restrictions on parameter values must be observed:

- All parameters must be greater than 1.
- Linetime must be an even multiple of the period of **notSerialClk**.
- 2×HalfSync + BackPorch + Display > Linetime/2 > 2×HalfSync + BackPorch.
- The total number of displayed lines in each frame must be a whole number. In interlace, this must be an odd whole number.
- Backporch must exceed TransferDelay by at least one **notSerialClk** period; also it must exceed 16 SClk periods in total.
- Transfer delay must not exceed ShortDisplay.

(The parameter TransferDelay is described in section 7.10.4).

7.8.5 The startup sequence

Reading from and writing to the VTG registers, which are memory mapped, is accomplished while the timing generator is disabled.

On startup, after reset, the host processor must write a configuration pattern to the G332 bootstrap location. The effect of this is to set the PLL multiplication factor, clock source (PLL or external crystal) and microport address alignment. It must then initialise the VTG by writing a 0 to bit 0 in control register A.

Startup sequence:

1 Assert, then deassert **Reset**.
  –Wait 50ns

2 Write configuration pattern to bootstrap location.

3 Write to control register to initialise VTG.

After this the screen parameters and colour table data can be written to the appropriate locations in any order. The processor must then make another write to the control register to enable the VTG which will then start up immediately at the beginning of frame sync. The G332 can be reprogrammed without asserting Reset.

The reprogramming sequence has three steps:

1 Write zero to bit 0 of the control register, disabling VTG.

2 Write to the screen parameter registers chosen for redefinition.

3 Write one to bit 0 of the control register, (redefining modes if necessary by modifying the relevant register bits) and enabling the VTG.

If only the operating mode is to be changed, step 2 only may be omitted, the remainder of the address space is programmed without disabling the VTG. If the clock multiplication factor is to be changed the full startup procedure must be followed, including reset.

7.9 Synchronising and blanking signals

7.9.1 Introduction

The video timing generator produces sync and blank signals to a pattern specified by a combination of the operating mode of the G332 and the screen description parameters. Internally, composite sync and blank are supplied to the three DACs by default. However, both of these functions can be disabled by setting bits 6 and 11 of Control RegisterA, respectively.

The internal sync and blank signals are automatically scheduled according to the operating mode. An additional programmable delay of 0 - 7 serial clock cycles may be added to sync and blank if it is required to add pipeline delays in the pixel path.

7.9.2 Master mode

When running in master (internal sync) mode, the **notVSync** and **notCorHSync** pins are outputs and the G332 drives them active low. Untesselated frame sync always appears on the **notVSync** pin, while the **notCorHSync** pin is switchable to supply one of line sync, plain composite sync, or tesselated composite sync:

Register Bits 5	4	notVSync	notCorHSync	
			notHSync	notCSync
0	0	Plain	-	Tesselated
0	1	Plain	-	Plain
1	0	Plain	Plain	-
1	1	Plain	Plain	-

7.9.3 Slave mode

In slave mode, the **notVSync** and **notCorHSync** pins are designated as inputs, and the G332 will use them to determine when to start a frame. In such a scheme two or more devices can be synchronised together.

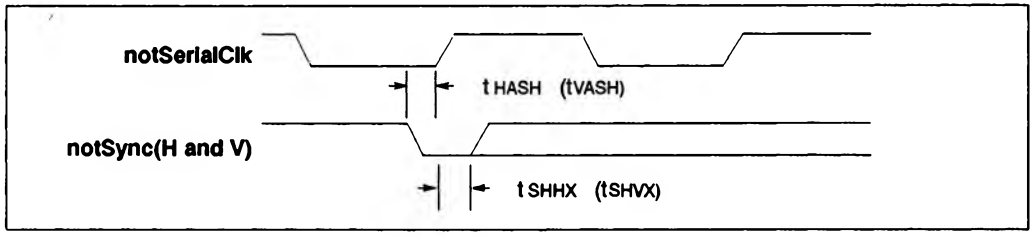


Figure 7.10 External synchronisation

Symbol	Description	Min.	Max.	Unit
tVASH	**notVsync** setup time	SClk/4	3SClk/4	ns
tHASH	**notHsync** setup time	SClk/4	3SClk/4	ns
tSHVX	**notVsync** hold time	0		ns
tSHHX	**notHsync** hold time	0		ns
Note: These figures are not characterised and are subject to change				

Table 7.11 External sync waveform timings

7.10 The micro port

7.10.1 Introduction

The micro port is a bidirectional 24 bit interface, consisting of a multiplexed address and data bus and several control signals. It is used for programming the VTG screen description registers, colour and cursor lookup tables, cursor store, and other registers.

As well as serving as a programming port the interface is also capable of performing a video RAM shift register transfer operation using a fully handshaked DMA. The timing of this operation is synchronous with the pixel port and is arranged so that seamless update of the video RAM shift register is possible.

7.10.2 Word alignment

The IMS G332 is designed for use with 32 and 64 bit processors, and therefore supports both 32 and 64 bit word alignment. With 32 bit alignment selected, the least significant address bit is on **ADBus2**; with 64-bit alignment selected it is on **ADBus3**. This applies both on host processor accesses to the microport and on DMA transfer cycles.

7.10.3 Micro port read/write cycles

Four signals control the flow of address and data in and out of the device on **ADBus0-23**.

Signal	I/O	Function
notChipSelect	I	The falling edge latches the address and samples **ReadnotWrite.** The cycle is initiated. The rising edge terminates the cycle, and tristates the **ADBus** drivers on a read cycle.
ReadnotWrite	I	If this signal is low shortly after **notChipSelect** goes low, the cycle is a write; if it is high the cycle is a read. Additionally on a write cycle, the rising edge of **ReadnotWrite** strobes in the data.
notOutputEnable	I	This signal is used only during read cycles, and enables the read data onto the **ADBus**. It should be kept high at all other times.
Wait	O	Wait eliminates the need for an external wait state generator. It is driven high shortly after **notChipSelect** goes low, and is driven back low when the G332 is ready for write data to be strobed by **ReadnotWrite** or read data is about to become valid on the **ADBus**.

7.10.4 DMA transfer operation

The IMS G332 provides three signals; **BusReq**, **TransferA** and **TransferB**, to control the synchronous reloading of the VRAM shift registers. Both **TransferA** and **TransferB** are used in interleaved mode, **TransferA** only is used in non-interleaved mode.

The G332 asserts **BusReq** to obtain use of the **ADBus** to perform a DMA cycle. The host processor asserts **BusGranted** to acknowledge the request. **TransferA** and **TransferB** (if used) are driven high simultaneously by the G332, and trigger the external generation of RAS, address mux and CAS signals to the VRAMs. **TransferA** goes low synchronous with **notShiftClkA**, and **TransferB** is synchronised to **notShiftClkB**. This performs the transfer operation.

The exact time at which the transfer occurs is critical, since mid-line updates must be seamless. The time taken from assertion of **BusReq** to the transfer taking place is a sum of various system delays, some of which are variable. The parameter **Transfer Delay** (Micro port address #X02D) must be set thus:

Transfer Delay $\geq$ The maximum possible system DMA latency + VRAM access + 4 SClk

The G332 has a further requirement, that:

$$\textbf{TransferDelay} \leq \text{Backporch} - 1$$

to ensure that there is data loaded ready for the first scan line to begin.

Another parameter, **MemInit** (Microport Address #X02C), determines the frequency of DMA transfer cycles. The sum of **MemInit** and **TransferDelay** defines the interval between successive Bus Requests.

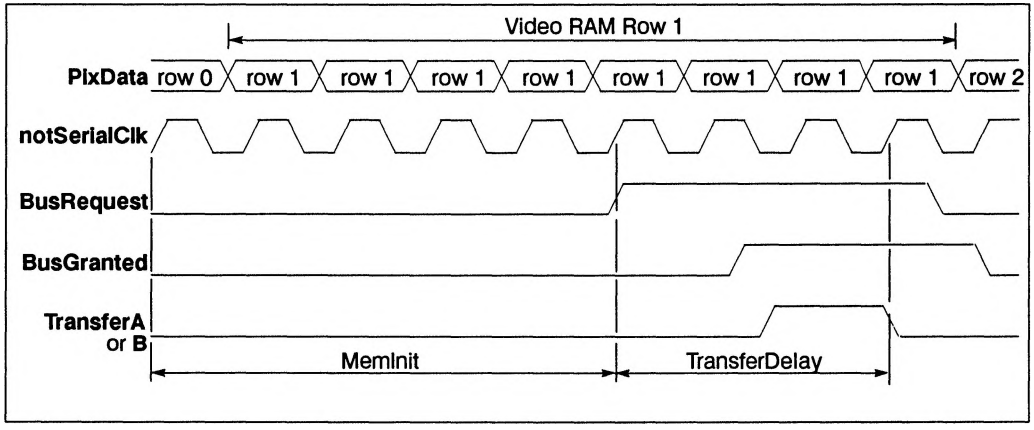


Figure 7.11 Data transfer sequence

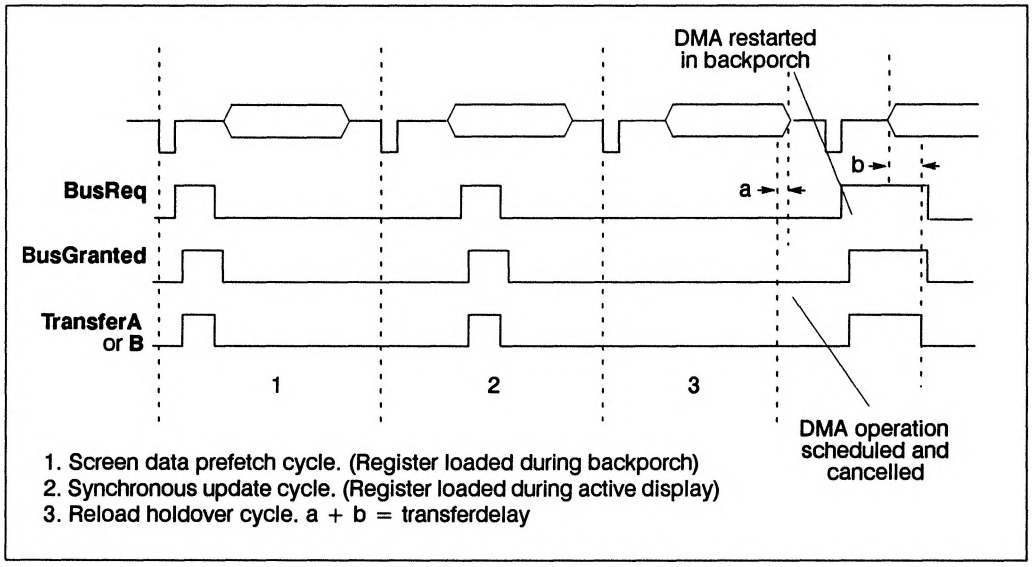


Figure 7.12 Data transfer operational behaviour

Figure 7.11 shows the sequence of events during a synchronised VRAM row transfer operation performed by the G332 which takes place part-way along a display line. That is to say an uninterrupted stream of pixels is maintained during a reload of the shift registers.

7.10.5 VRAM address increment

To allow either the existing VRAM row or column address latches to be used for the row address during DMA transfer cycles, several address increments are provided, both for interlaced and non-interlaced modes. They are selected from Control Register A.

Register Bit			Description	Format	Second field
13	12	1			
0	0	0	Increment by 1.	Non-interlace format.	
0	0	1	Increment by 1.	Interlace format.	Every second field offset by 1.
0	1	0	Increment by 256.	Non-interlace format.	
0	1	1	Increment by 2.	Interlace format.	Every second field offset by 1.
1	0	0	Increment by 512.	Non-interlace format.	
1	0	1	Increment by 512.	Interlace format.	Every second field offset by 256.
1	1	0	Increment by 1024.	Non-interlace format.	
1	1	1	Increment by 1024.	Interlace format.	Every second field offset by 512.

Table 7.12

7.10.6 FrameInactive

A further timing signal, **FrameInactive**, is provided which can be used to convey frame timing information to the host. This signal may be used in multiboard systems where frame swapping is used to implement animation, for example. **FrameInactive** is asserted whenever the timing generator enters frame flyback and is deasserted on entering active display.

7.11 The pixel port

The 32 bit pixel port takes in pixel data from the video RAM and has various modes of operation.

7.11.1 Interleaved/non-interleaved operation

Because of the very high video rates supported by the G332 it is not possible in some situations to supply pixel data fast enough from a single bank of video RAMs. An interleaved mode has been provided to allow two banks of VRAM to be used, each running at half the frequency required when using one bank. 32 bits of pixel data are loaded alternately from one VRAM bank then the other.

In interleaved mode, two **notShiftClk** and two **Transfer** signals are used to control the two banks, the shift clocks running in anti-phase. **notShiftClkA** and **TransferA** control the lower numbered pixels, and not-**ShiftClkB** and **TransferB** control the higher numbered pixels. On DMA transfer cycles both banks have their shift registers reloaded, which means that these cycles are required at half the frequency compared with non-interleaved mode.

In non-interleaved mode only **notShiftClkA** and **TransferA** are used, and true-colour pixel modes are not available.

7.11.2 Pixel sampling

The point at which pixels are sampled by the G332 varies according to the pixel mode selected (refer to section 7.11.3). In 8 bit per pixel non-interleaved mode and 15/16 bit per pixel interleaved mode, pixels are sampled one not serial clock period **(SClk)** after **notShiftClkA** or **B.** In all other modes sampling is optionally delayed by a further 1/2 **ShiftClk**.

7.11.3 Pixel multiplexing

The G332 supports 6 pixel modes in interleaved mode and 4 in non-interleaved mode selected from control register A, as follows:

Non-interleaved mode

Register bits				Bits per pixel	ShiftClk period	MUX ratio	Use of LUT
22	21	20	18				
0	1	1	0	8	1 SClk	4:1	Pseudo colour
0	1	0	0	4	2 SClks	8:1	Pseudo colour
0	0	1	0	2	4 SClks	16:1	Pseudo colour
0	0	0	0	1	8 SClks	32:1	Pseudo colour

Interleaved mode

Register bits				Bits per pixel	ShiftClk period	MUX ratio	Use of LUT
22	21	20	18				
1	0	1	1	16	1 SClk	2:1	Gamma corrected true colour
1	0	0	1	15	1 SClk	2:1	Gamma corrected true colour
0	1	1	1	8	2 SClks	4:1	Pseudo colour
0	1	0	1	4	4 SClks	8:1	Pseudo colour
0	0	1	1	2	8 SClks	16:1	Pseudo colour
0	0	0	1	1	16 SClks	32:1	Pseudo colour

7.11.4 True colour modes (15 and 16 bits per pixel)

Each pair of pixel ports (A and B, and C and D) supply a two-byte pixel value which is split into red, green and blue fields as illustrated below. In 15 bits per pixel mode bits 0-4 are blue, 5-9 are green, and 10-14 are red. In 16 bits per pixel mode bits 0-3 are blue, 4-9 are green, and 10-15 are red.

Each colour field addresses the LUT which may contain a suitable gamma correction table for that colour. The unused LUT address bits in 15 and 16 bit per pixel modes are the lowest order bits, which avoids the need to change the gamma-correction table when switching between true colour modes. If no gamma correction is required the LUT must be written with data = address.

Port	A	A	A	A	A	A	A	A		B	B	B	B	B	B	B	B		C	C	C	C	C	C	C	C		D	D	D	D	D	D	D	D
Bit	0	1	2	3	4	5	6	7		0	1	2	3	4	5	6	7		0	1	2	3	4	5	6	7		0	1	2	3	4	5	6	7
15bpp																																				
Pixel	Pixel 0																		Pixel 1																	
Colour	B	B	B	B	B	G	G	G		G	G	R	R	R	R	R	X		B	B	B	B	B	G	G	G		G	G	R	R	R	R	R	X
Bit	0	1	2	3	4	0	1	2		3	4	0	1	2	3	4	-		0	1	2	3	4	0	1	2		3	4	0	1	2	3	4	-
16bpp																																				
Pixel	Pixel 0																		Pixel 1																	
Colour	B	B	B	B	G	G	G	G		G	G	R	R	R	R	R	R		B	B	B	B	G	G	G	G		G	G	R	R	R	R	R	R
Bit	0	1	2	3	0	1	2	3		4	5	0	1	2	3	4	5		0	1	2	3	0	1	2	3		4	5	0	1	2	3	4	5
Key: R = Red, G = Green, B = Blue and X = bit not used																																				

Figure 7.13 Pixel mapping diagram

7.11.5 Pseudo colour modes (1, 2, 4 and 8 bits per pixel)

The pixel data is latched from ports A, B, C and D in that order. Each pixel is masked by 8 bits of the mask register before the output is used to address all three LUTs which contain the pseudo colour palette.

8 bits per pixel mode:

Each port supplies 1 pixel. Bits 0–7 of the port correspond to LUT address bits 0–7 respectively. All 256 locations in the LUT are used.

4 bits per pixel mode:

Each port supplies 2 pixels. Bits 0–3 of the port are the first pixel displayed, bits 4–7 are the second pixel displayed. Both correspond to LUT address bits 0–3 respectively. Only locations 0 to 15 of the LUT are used.

2 bits per pixel mode:

Each port supplies 4 pixels. Bits 0–1 of the port are the the first pixel displayed, bits 6–7 the last pixel displayed. Each pair of pixel inputs corresponds to LUT address bits 0–1. Only locations 0 to 3 of the LUT are used.

1 bit per pixel mode:

Each port supplies 8 pixels. Bit 0 of the port is the first pixel displayed, bit 7 the last pixel displayed. Each pixel input corresponds to LUT address bit 0. Only locations 0 and 1 of the LUT are used.

7.11.6 Mask register

(micro port address #X040)

The 24 bit mask register masks the pseudo colour pixel inputs to the three LUTs. Bits 0–7 mask the blue data, 8–15 the green data, and 16–23 the red data. Setting a bit in the mask register to zero causes the corresponding LUT address bit to be set to zero.

7.12 Hardware cursor

The G332 hardware cursor consists of a 64×64×2 bit RAM, addressed as a sequence of consecutive 16 bit words. Each word is formatted into 8 pixels as below, and is randomly addressable at any time.

Pixel	7		6		5		4		3		2		1		0	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Cursor position is held in a single 24 bit register as an x-y location relative to the top left of the screen. The position defined is that of the topmost, leftmost pixel of the cursor. The most significant half of the cursor position word (bits 12-23) is its x-address (horizontal position) and the least significant half (bits 0-11) is its y-address (vertical position). The cursor position is held in the CursorStart register at microport address #X0C7. The x-address and y-address are two's complement values in the range -64 to 2303.

The 2 bit cursor pixels address a 3 location cursor look-up table as follows:

Pixel value	Format
0 0	Cursor transparent. Background colour displayed.
0 1	Colour from cursor LUT location 1
1 0	Colour from cursor LUT location 2
1 1	Colour from cursor LUT location 3

The cursor is enabled/disabled via bit 23 in Control RegisterA.

7.13 Anti-sparkle colour palette

The IMS G332 includes a 256×24bit colour look-up table which is mapped directly into the micro port address space. Complete colour values are written by a single write cycle on the micro port. In order to minimise picture disturbance whilst a colour palette entry is being accessed, the previous pixel is repeated at the DACs.

7.14 Checksum registers

There are three 24 bit checksum registers, one for each colour channel. Their purpose is to facilitate testing the device and systems containing it. The checksum is located directly before the DACs, and after the colour and cursor palettes. The checksum value is dependent on the cursor position and whether or not interlaced mode is selected, but independent of sync modes and flyback patterns.

The checksum registers are reset by the falling edge of **FrameInactive**. They accumulate only those pixels which are visible on the screen, i.e. those pixels which are unblanked. The registers should be read during the first part of frame flyback. At the end of this period they are being reset, and at other times they are being accumulated and are consequently invalid.

The checksum registers are addressed from the microport as 24 bit words containing low, middle and high bytes, as follows:

Micro port address	Bits 16-23	Bits 8-15	Bits 0-7
#X0C0	Red bits 0-7	Green bits 0-7	Blue bits 0-7
#X0C1	Red bits 8-15	Green bits 8-15	Blue bits 8-15
#X0C2	Red bits 16-23	Green bits 16-23	Blue bits 16-23

7.15 Clocks

The IMS G332 has two alternate clocking schemes. The primary clocking system uses a phase locked loop (PLL) on the chip to multiply up the low frequency (<10MHz) input clock to the required video data rate. Alternatively a full dot-rate clock may be supplied (×1 mode).

7.15.1 PLL mode

In PLL mode, a 1μF capacitor must be connected between **CapPlus** and **CapMinus.** A ceramic capacitor is preferred, with an impedance of less than 3Ω between 100kHz and 10MHz. If a polarised capacitor is used, the negative terminal must be connected to **CapMinus**. Total PCB track length should be less than 50mm.

The multiplication factor is determined from the binary value written to bits 0..4 of the boot location (#X000). Values from 5 to 31 are permitted. Also, the clock source select bit (bit 5) in the Boot Location (#X000) must be set to a '1'.

ClockIn must be derived from a crystal oscillator; RC oscillators are not sufficiently stable. ClockIn must not be distributed through a long chain of buffers. Clock edges must be monotonic and remain within the specified voltage and time limits.

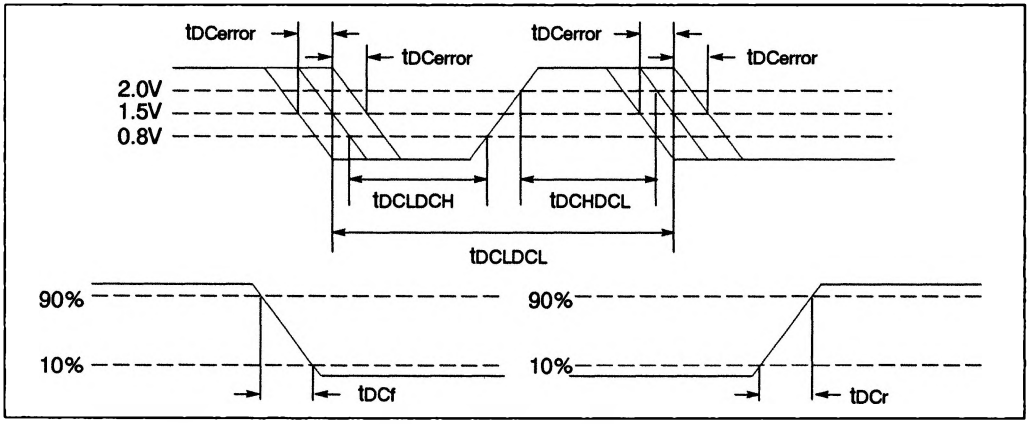


Figure 7.14 ClockIn timing

Symbol	Parameter	Min.	Nom.	Max.	Units	Notes
tDCLDCH	ClockIn pulse width low	20			ns	
tDCHDCL	ClockIn pulse width high	20			ns	
tDCLDCL	ClockIn period	100		200	ns	1
tDCerror	ClockIn timing error			±0.015	%	2
tDCr	ClockIn rise time			10	ns	3
tDCf	ClockIn fall time			8	ns	3
Note: These figures are not characterised and are subject to change						

Table 7.13 ClockIn timings in PLL mode

Notes

1 Measured between corresponding points on consecutive falling edges.

2 Variation of individual falling edges from their normal times.

3 Clock transitions must be monotonic within the range **VIH** to **VIL.**

Note: These figures are not characterised and are subject to change.

7.15.2 'Times 1' mode

The external ×1 clock can be selected in one of two ways. Either the terminals **CapPlus** and **CapMinus** should be shorted together, or the clock source select bit in the boot location should be written to a '0'.

7.16 The video DACs

7.16.1 General

The video DACs have 8 bit resolution, and are designed to drive a doubly terminated 75Ω transmission line and produce analogue outputs compatible with RS170 and RS343 video standards.

The DACs work by sourcing a current proportional to their digital input. The DAC unit current for each digital increment is defined by an external Iref current source;

$$1\ \text{DACunit} = \text{Iref}/120$$

The video information output by each gun ranges from 0 to 255 units under the control of the digital input from the colour palette or the pixel pin.

A sync pedestal of 108 DAC units and a blanking pedestal of 20 DACunits are provided. The sync pedestal allows superposition of the sync timing signals on the video outputs. The blanking pedestal ensures that no visible trace appears on the screen during flyback.

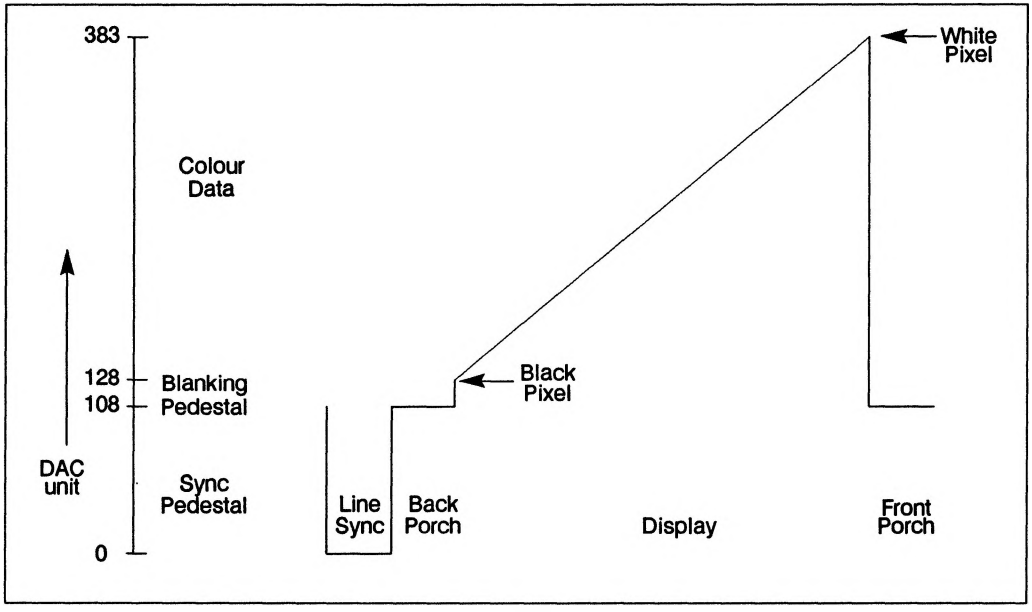


Figure 7.15 DAC output levels

7.16.2 DAC characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes (1)
	Resolution	8	8	8	bits	
VO(max)	Output voltage			1.5	V	2
IO(max)	Output current			34	mA	VO≤1V
	Full scale error			± 5	%	2, 3
	Sync pedestal error			±10	%	2
	Blank level pedestal error			±10	%	2
	DAC to DAC correlation error			± 2.5	%	2, 4
	Integral Linearity error			± 1	LSB	2, 5
	Glitch Energy		75		pVSec	2, 6, 7
Iref	Reference current	7		10	mA	
Vref	Reference voltage	VDD −3V		VDD	Volts	
Note: These figures are not characterised and are subject to change						

Notes

1 All voltages with respect to **GND** unless specified otherwise.

2 Tested over the operating temperature range and at nominal supply voltage with **Iref** = −8.88mA.

3 From the value predicted by the design equation, sync and black level pedestals off.

4 About the mid point of the distribution of the 3 DACs measured at full scale deflection.

5 Linearity measured from the best fit line through the DAC characteristic. Monotonicity guaranteed.

6 Load = 37.5Ω +30 pF with **Iref** = −8.88mA.

7 This parameter is sampled not 100% tested.

7.16.3 Power supply and reference circuit

7.16.4 Power supply and current reference

It is recommended that a high frequency decoupling capacitor (preferably a chip capacitor) in parallel with a larger tantalum capacitor (22μF to 47μF) be placed between **AVDD** and **GND** to provide the best possible supply to the analogue circuitry of the DACs.

It is further recommended that the IMS G332 is soldered directly into the PCB without using a socket in order to minimise inductance.

To ensure that the output current of the DACs is predictable and stable with temperature variations, an active current reference is recommended. Figure 7.16 shows four designs of current reference.

If the board **VDD** supply is very noisy, then it is advisable to provide a quiet supply for just the IMS G332. This may be done by supplying both **VDD** and **AVDD** through a small inductor (1-5μH). This will act as an ac filter for high frequency noise. However, if this is done care should be taken to ensure the power rating of this inductor is not exceeded.

Figure 7.16(d) shows the use of the LM334 precision current source as a current reference. It is shown in its temperature compensated configuration. The reference current is set by a single resistor (15Ω in this case) and is independent of the value of power supply voltage.

Figures 7.16(a)-(c) are similar circuits. Each circuit uses three resistors and the power supply voltage to set the reference current **Iref** through a transistor. In circuits 7.16(b) and 7.16(c) the thermal variations in

the base emitter voltage of the transistor are compensated by the use of a forward biased diode (a transistor acting as a diode in the case of circuit 7.16(c)).

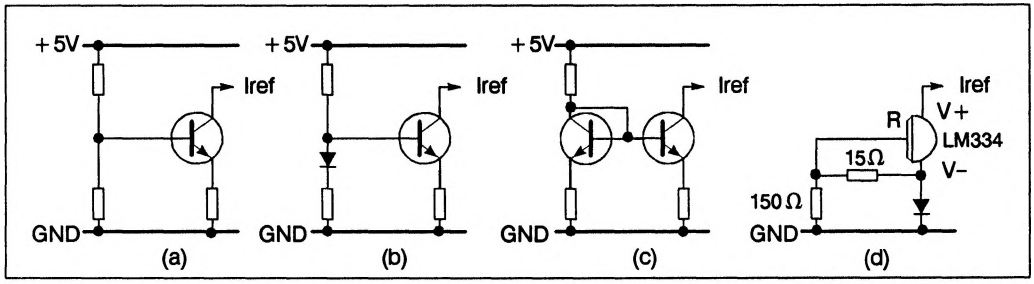


Figure 7.16

7.16.5 Current reference – decoupling

The DACs in the IMS G332 are made from switched current sources which are based around a current mirror. The total current output by each DAC is determined by the number of active current sources and the reference current **Iref**.

So long as any supply variations are minor, or a suitably high quality current reference is used which tracks the variations, then no coupling capicitors need be used.

However, voltage variations on the supply not managed by the current reference circuit will result in variations in the DAC output current. If the bandwidth of the current reference circuit is not sufficient to track these supply variations it is recommended that a coupling capacitor (47μF to 100μF) in parallel with a high frequency capacitor of 100nF should be used to couple the **Iref** input to VDD. This will enable the current reference to track both low and high frequency variations in the supply.

7.16.6 Analogue output – line driving

The G332 is designed to drive a doubly terminated 75Ω line. This arrangement is illustrated in figure 7.17. The effective load seen by the G332 video outputs with this circuit is 37.5Ω.

The connection beteween the DAC outputs on the G332 and the input to the colour monitor should be regarded as a transmission line. Impedance changes along this line will result in reflection of part of the video signal back along the line. These reflections can result in a degradation of the picture displayed by the monitor. To ensure good fidelity RF techniques should be used; in particular the PCB trace from the G332 video output pins to the video sockets on the graphics board should be kept short (less than 3 inches is ideal). If this is done then any reflections due to a mismatched impedance at the video connectors will occur within the risetime of the DAC waveform and will not cause a degradation of the image quality.

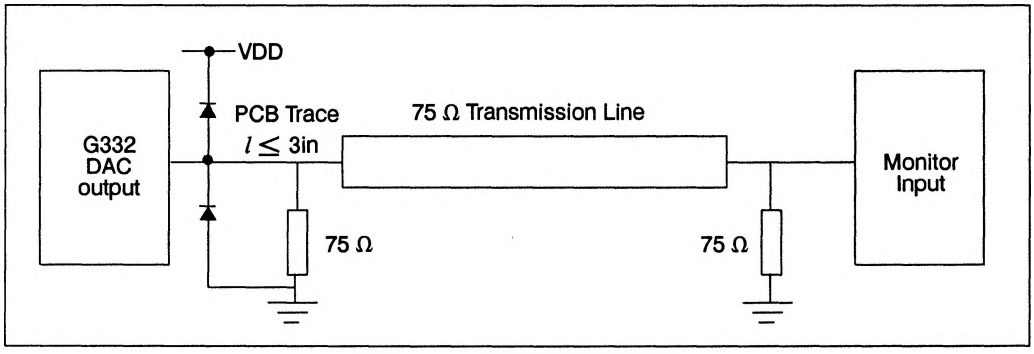


Figure 7.17 DAC output loading

7.16.7 Analogue output – protection

CMOS devices are susceptible to damage from high electrostatic voltages. Normal antistatic precautions should be observed when handling the IMS G332 during system manufacture.

Once assembled into a system devices are much less exposed to static damage. However if the analogue outputs of the IMS G332 are made available at connectors outside the graphic system they are still exposed to static damage and other hazardous voltages. Protection diodes to the power rails are recommended at this exposed interface.

7.17 General parametric conditions and characteristics

7.17.1 Absolute Maximum ratings

Symbol	Parameter	Min.	Max.	Units	Notes
AVDD/VDD	DC Supply Voltage		7	Volts	
	Voltage on other pins	VSS–1	VDD + 0.5	Volts	
TS	Storage temperature (ambient)	–65	150	°C	
TA	Temperature under bias	–40	85	°C	
PDmax	Power dissipation		TBD	W	
Iref	Reference current		15	mA	
	Analogue O/P current		45	mA	1
	DC Digital O/P current		25	mA	

Notes

1 Per output

7.17.2 Operating conditions

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
VDD	Positive Supply Voltage	4.75	5.0	5.25	Volts	1
GND	Ground		0		Volts	
VIH	Input Logic '1' Voltage	2.0		VDD + 0.5	Volts	
VIL	Input Logic '0' Voltage	–0.5		0.8	Volts	
TPQFP	Case Temperature	TBD		TBD	°C	2
TCQFP	Case Temperature	TBD		TBD	°C	2
Note: These figures are not characterised and are subject to change						

Notes

1 AVDD = VDD

2 Measured on the lid of the package at maximum power dissipation.

7.17.3 Operating characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
IDD	Power Supply Current		TBD	TBD	mA	
IIN	Digital Input Current			±10	µA	
IOZ	TriState Dig Output Current			±50	µA	
VOH	Output Logic '1' Voltage	2.4			Volts	
IOH	Output Logic '1' Current	−5			mA	
VOL	Output Logic '0' Voltage			0.4	Volts	
IOL	Output Logic '0' Current	5			mA	
Note: These figures are not characterised and are subject to change						

7.17.4 Output drive capability

Parameter	Min.	Max.	Units	Notes
notShiftClkA		25	pF	1
notShiftClkB		25	pF	1
notSerialClk		25	pF	1
TransferA		25	pF	
TransferB		25	pF	
ADBus [0..23]		25	pF	

Notes

1 **These loadings must be strictly adhered to in order to avoid a degradation in picture quality.**

7.18 Package specifications

7.18.1 100 pin ceramic quad flatpack package

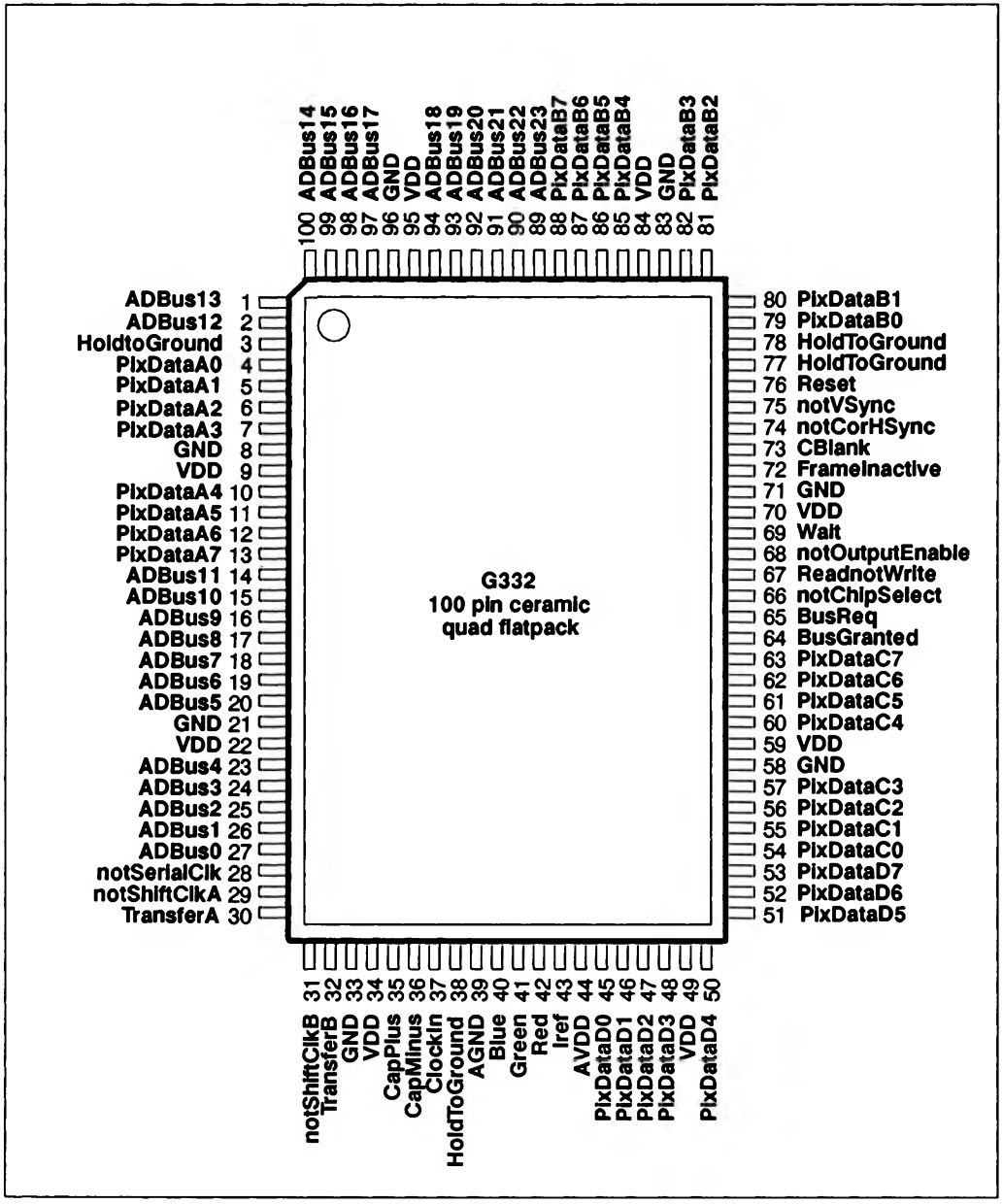


Figure 7.18 IMS G332 pin configuration

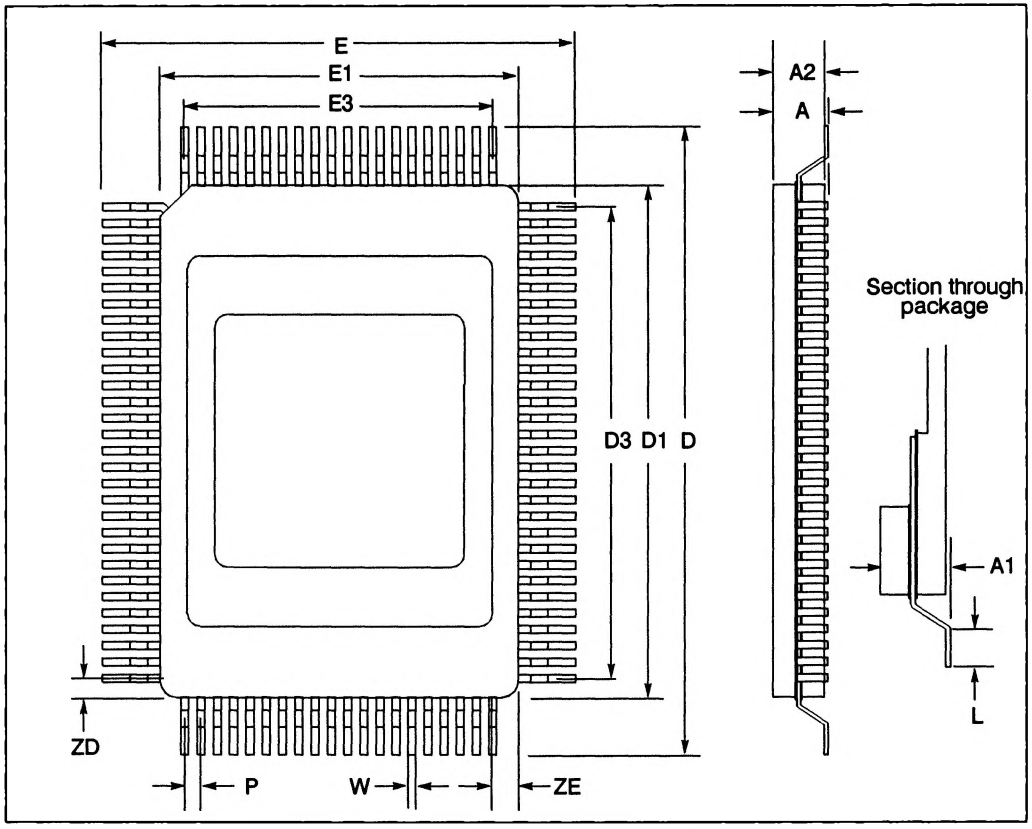


Figure 7.19 100 pin ceramic quad flatpack package dimensions

Dim	Millimetres			Inches			Notes
	Min	Nom	Max	Min	Nom	Max	
A			3.300			0.130	
A1	0.000		0.250	0.000		0.010	
A2	2.550	2.800	3.050	0.100	0.110	0.120	
D	23.650	23.900	24.150	0.931	0.941	0.951	
D1	19.900	20.000	20.100	0.783	0.787	0.791	
D3		18.850			0.742		Ref.
ZD		0.580			0.023		Ref.
E	17.650	17.900	18.150	0.695	0.705	0.715	
E1	13.900	14.000	14.100	0.547	0.551	0.555	
E3		12.350			0.486		Ref.
ZE		0.830			0.033		Ref.
L	0.650	0.800	0.950	0.026	0.031	0.037	
P		0.650			0.026		BSC
W	0.220		0.380	0.087		0.015	

Table 7.14 100 pin ceramic quad flatpack package dimensions

7.18.2 Ordering information

Device	Clock rate	Package	Part number
IMS G332	85 MHz	100 pin ceramic quad flatpack	IMS G332F-85S
IMS G332	100 MHz	100 pin ceramic quad flatpack	IMS G332F-10S
IMS G332	110 MHz	100 pin ceramic quad flatpack	IMS G332F-11S
*IMS G332	135 MHz	100 pin ceramic quad flatpack	IMS G332F135S
Note: PQFP for this device is currently under development			

* Available 1991