Supertex inc. HV20822

16 Channel High Voltage Analog Switch

Ordering Information

V_{PP}-V_{NN}	Package Options	
	48-lead TQFP	Die
220V	HV20822FG	HV20822X

Features

- ❑ HVCMOS® technology for high performance
- ❑ 220V operating conditions
- ❑ Output On-resistance typically 22Ω
- ❑ 5.0V and 12.0V CMOS logic compatibility
- ❑ Very low quiescent power dissipation-10µA
- ❑ -45dB min off isolation at 7.5MHz
- ❑ Low parasitic capacitance
- ❑ Excellent noise immunity
- ❑ Flexible high voltage supplies

General Description

The Supertex HV208 is a 220V 16-channel high-voltage analog switch integrated circuit (IC) configured as 2 sets of 8 single pole single throw analog switches. It is intended for use in applications requiring high voltage switching controlled by low voltage control signals such as ultrasound imaging and printers. The 2 sets of 8 analog switches are controlled by 2 input logic controls, $D_{IN}1$ and $D_{IN}2$. A logic high on $D_{IN}1$ will turn ON switches 0 to 7 and a logic high on $D_{IN}2$ will turn ON switches 8 to 15.

Absolute Maximum Ratings*

V_{DD} Logic power supply voltage		-0.5V to +15V
V_{PP} - V_{NN} Supply voltage		+225V
V_{PP} Positive high voltage supply		-0.5V to V_{NN} +225V
V_{NN} Negative high voltage supply		+0.5V to -225V
Logic input voltages		-0.5V to V_{DD} +0.3V
V_{SIG} Analog Signal Range		V_{NN} to V_{PP}
Peak analog signal current/channel		3.0A
Storage temperature		-65°C to +150°C
Power dissipation	48-lead TQFP	1.0W

* All voltages are referenced to ground. Absolute maximum ratings are those values which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability.

06/26/01

Electrical Characteristics

DC Characteristics (over recommended operating conditions unless otherwise noted)

Characteristics	Sym	0°C		+25°C			+70°C		Units	Test Conditions
		min	max	min	typ	max	min	max		
Small Signal Switch (ON) Resistance	R_{ONS}		30		26	32		40	ohms	V_{SIG} = 0V, I_{SIG} = 5mA, V_{PP} = 50V, V_{NN} = -170V
			25		22	27		35		V_{SIG} = 0V, I_{SIG} = 200mA, V_{PP} = 50V, V_{NN} = -170V
			15		22	27		30		V_{SIG} = 0V, I_{SIG} = 5mA, V_{PP} = 110V, V_{NN} = -110V
			20		18	22		25		V_{SIG} = 0V, I_{SIG} = 200mA, V_{PP} = 110V, V_{NN} = -110V
Small Signal Switch (ON) Resistance Matching	ΔR_{ONS}		20		5.0	20		20	%	V_{SIG} = 0V, I_{SIG} = 5mA, V_{PP} = 110V, V_{NN} = -110V
Large Signal Switch (ON) Resistance	R_{ONL}				15				ohms	V_{SIG} = 0V, I_{SIG} = 1.0A
Switch Off Leakage Per Switch	I_{SOL}		5.0		1.0	10		15	µA	V_{SIG} = V_{PP} -10V and V_{NN} +10V
DC Offset Switch OFF		300			100	300		300	mV	R_L = 100Kohms
DC Offset Switch ON		500			100	500		500		R_L = 100Kohms
Pos. HV Supply Current	I_{PPQ}				10	50			µA	All SWs OFF
Neg. HV Supply Current	I_{NNQ}				-10	-50				All SWs OFF
Pos. HV Supply Current	I_{PPQ}				10	50				All SWs ON, I_{SW} = 5 mA
Neg. HV Supply Current	I_{NNQ}				-10	-50				All SWs ON, I_{SW} = 5 mA
Switch Output Peak Current			3.0		3.0	2.0		2.0	A	V_{SIG} duty cycle $\leq$ 0.1%
Output Switch Frequency	f_{SW}					50			KHz	Duty Cycle = 50%
I_{PP} Supply Current	I_{PP}		8.1			8.8		10	mA	V_{PP} = 50V, V_{NN} = -170V, ALL SWs turning ON and OFF at 50KHz
I_{NN} Supply Current	I_{NN}		-8.1			-8.8		-10		
I_{PP} Supply Current	I_{PP}		5			6.3		6.9		V_{PP} = 110V, V_{NN} = -110V, All SWs turning ON and OFF at 50kHz
I_{NN} Supply Current	I_{NN}		-5			-6.3		-6.9		
Logic Supply Quiescent Current	I_{DDQ}		10			10		10	µA	All logic states are at DC
Logic Supply Average Current	I_{DD}		2.0			2.0		2.0	mA	$D_{IN}1$ = $D_{IN}2$ = 3MHz, $\overline{LE}$ = high

Electrical Characteristics

AC Characteristics (over recommended operating conditions unless otherwise noted)

Characteristics	Sym	0°C		+25°C			+70°C		Units	Test Conditions
		min	max	min	typ	max	min	max		
Time to Turn OFF V_{SIG}*	$t_{SIG(OFF)}$	0		0			0		ns	
Time Width of $\overline{LE}$	t_{WLE}	150		150			150		ns	
Time Width of D_{IN}	t_{WDIN}	150		150			150		ns	
Set Up Time Before $\overline{LE}$ Rises	t_{SD}	150		150			150		ns	
Turn On Time	t_{ON}		2.0			2.0		2.0	µs	V_{SIG}=V_{PP} - 10V, R_{LOAD}=10KΩ
Turn Off Time	t_{OFF}		2.0			2.0		2.0	µs	V_{SIG}=V_{PP} - 10V, R_{LOAD}=10KΩ
Off Isolation	KO	-30		-30	-33		-30		dB	f = 5.0MHz, 1KΩ/15pF Load
		-45		-45	-50		-45		dB	f = 7.5MHz, R_{LOAD} = 50Ω
Switch Crosstalk	K_{CR}	-45		-45			-45		dB	f = 5.0MHz, R_{LOAD} = 50Ω
Off Capacitance Switch to GND	$C_{GS(OFF)}$	5.0	17	5.0	12	17	5.0	17	pF	V_{SIG} = 0V, 1MHz
On Capacitance Switch to GND	$C_{GS(ON)}$	25	50	25	38	50	25	50	pF	V_{SIG} = 0V, 1MHz
Output Voltage Spike	$+V_{SPK}$				4.0				V	
	$-V_{SPK}$				-4.0					

*Time required for analog signal to turn off before output switch turns off.

Operating Conditions

Symbol	Parameter	Value
V_{PP}	Positive high voltage supply[1]	+50V to +110V
V_{NN}	Negative high voltage supply[1]	-10V to V_{PP}-220V
V_{DD}	Logic power supply voltage[1]	4.75V to +12.6V
V_{IH}	High-level input voltage	V_{DD} -1.0V to V_{DD}
V_{IL}	Low-level input voltage	0V to 1.0V
V_{SIG}	Analog signal voltage peak-to-peak[2]	V_{NN} +10V to V_{PP} -10V
T_A	Operating free air-temperature	0°C to 70°C

Notes:

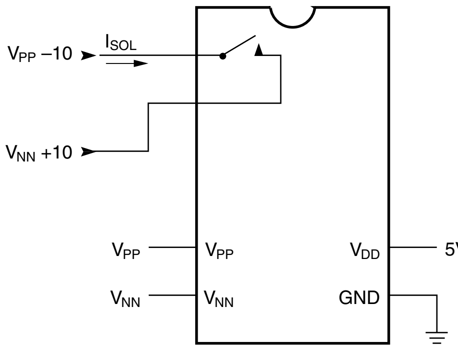
1 Power up/down sequence is arbitrary except GND must be powered-up first and powered-down last.

2 V_{SIG} must be $V_{NN} \le V_{SIG} \le V_{PP}$ or floating during power up/down transition.

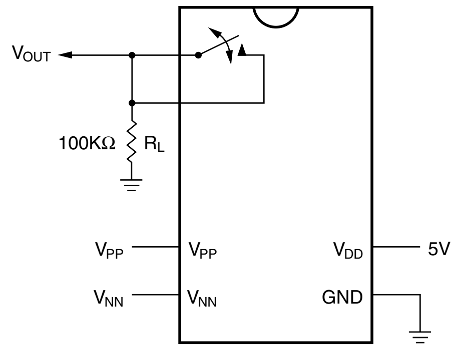
Truth Table

$D_{IN}2$	$D_{IN}1$	$\overline{LE}$	SW0 to SW7	SW8 to SW15
L	L	L	OFF	OFF
L	H	L	ON	OFF
H	L	L	OFF	ON
H	H	L	ON	ON
X	X	H	HOLD PREVIOUS STATE	

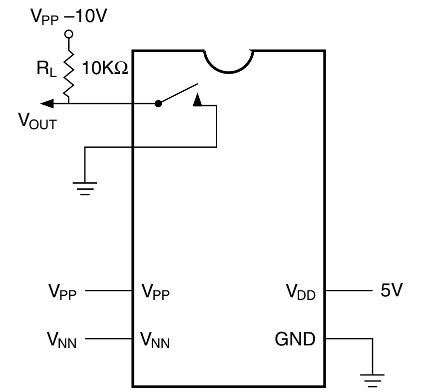
Test Circuits



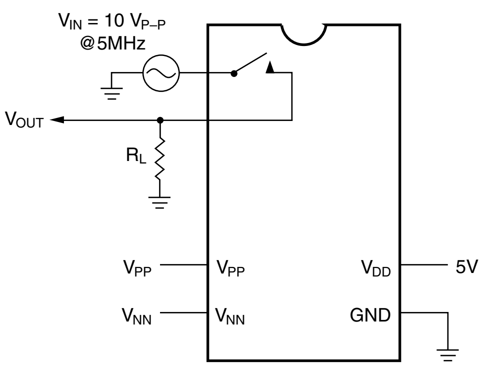
Switch OFF Leakage



DC Offset ON/OFF

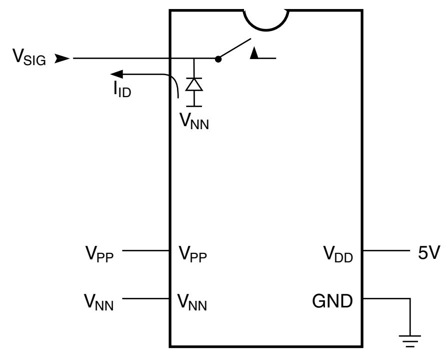


T_{ON}/T_{OFF} Test Circuit

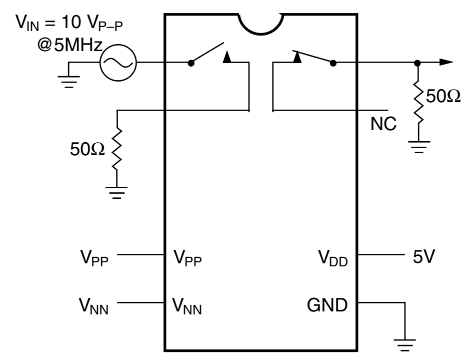


$K_O = 20\text{Log}\,\frac{V_{OUT}}{V_{IN}}$

OFF Isolation

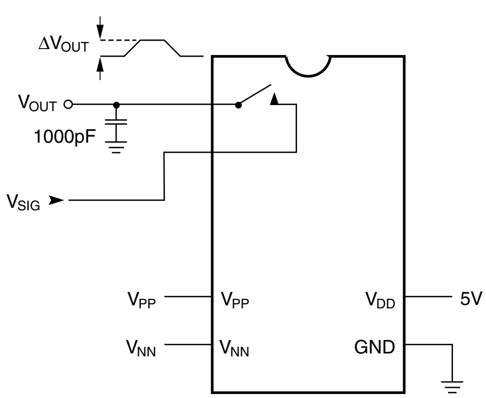


Isolation Diode Current



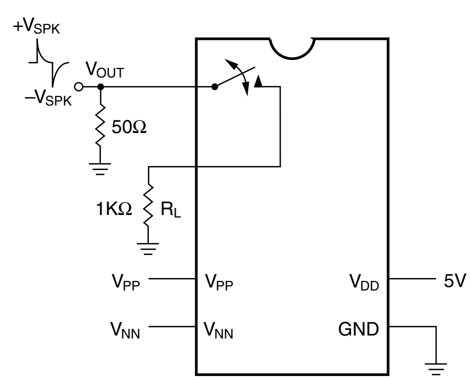
$K_{CR} = 20\text{Log}\,\frac{V_{OUT}}{V_{IN}}$

Crosstalk



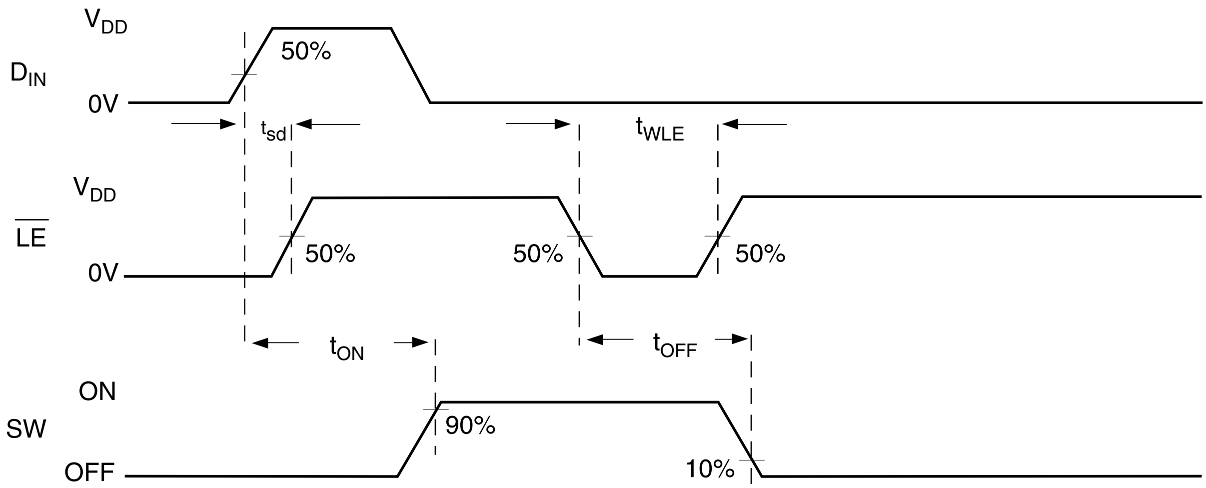
$Q = 1000\text{pF} \times \Delta V_{OUT}$

Charge Injection

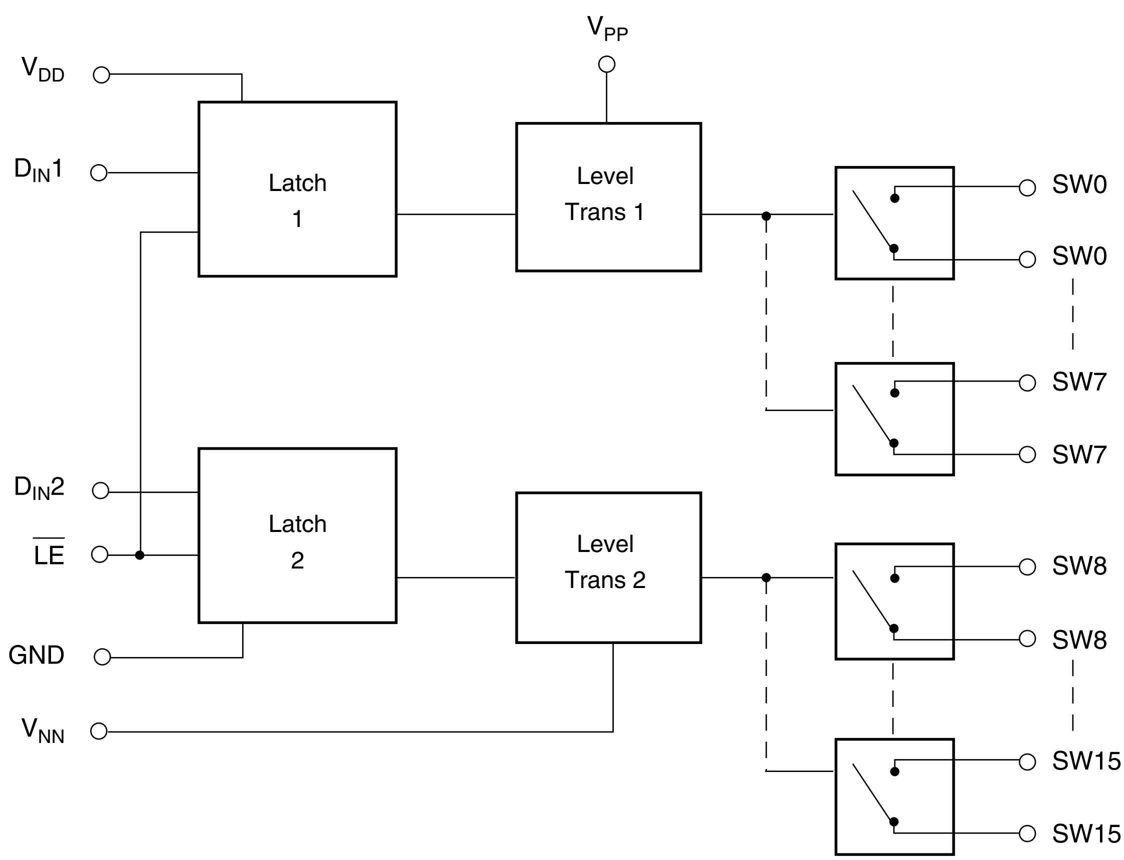


Output Voltage Spike

Logic Timing Waveform



Block Diagram

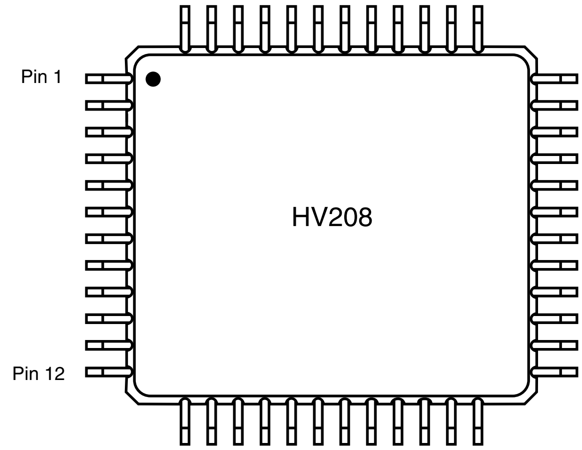


Pin Configuration

HV208 48-Pin TQFP

Pin	Function	Pin	Function
1	V_{NN}	25	SW10
2	N/C	26	SW10
3	V_{PP}	27	SW9
4	N/C	28	SW9
5	$D_{IN}1$	29	SW8
6	$\overline{LE}$	30	SW8
7	$D_{IN}2$	31	SW7
8	N/C	32	SW7
9	N/C	33	SW6
10	V_{DD}	34	SW6
11	GND	35	SW5
12	N/C	36	SW5
13	N/C	37	SW4
14	SW15	38	N/C
15	SW15	39	SW4
16	SW14	40	N/C
17	SW14	41	SW3
18	SW13	42	SW3
19	SW13	43	SW2
20	SW12	44	SW2
21	SW12	45	SW1
22	SW11	46	SW1
23	SW11	47	SW0
24	N/C	48	SW0

Package Outline



top view

48-pin TQFP

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