April 2012



FSGM0465R Green-Mode Fairchild Power Switch (FPS™)

Features

- Soft Burst-Mode Operation for Low Standby Power Consumption and Low Noise
- Precision Fixed Operating Frequency: 66kHz
- Pulse-by-Pulse Current Limit
- Various Protection Functions: Overload Protection (OLP), Over-Voltage Protection (OVP), Abnormal Over-Current Protection (AOCP), Internal Thermal Shutdown (TSD) with Hysteresis, Output-Short Protection (OSP), and Under-Voltage Lockout (UVLO) with Hysteresis
- Auto-Restart Mode
- Internal Startup Circuit
- Internal High-Voltage SenseFET: 650V
- Built-in Soft-Start: 15ms

Applications

 Power Supply for LCD TV and Monitor, STB and DVD Combination

Description

The FSGM0465R is an integrated Pulse Width Modulation (PWM) controller and SenseFET specifically designed for offline Switch-Mode Power Supplies (SMPS) with minimal external components. The PWM controller includes an integrated fixed-frequency oscillator, Under-Voltage Lockout (UVLO), Leading-Edge Blanking (LEB), optimized gate driver, internal soft-start, temperature-compensated precise current sources for loop compensation, and self-protection circuitry. Compared with a discrete MOSFET and PWM controller solution, the FSGM series can reduce total cost, component count, size, and weight; while simultaneously increasing efficiency, productivity, and system reliability. This device provides a basic platform suited for cost-effective design of a flyback converter.

Related Resources

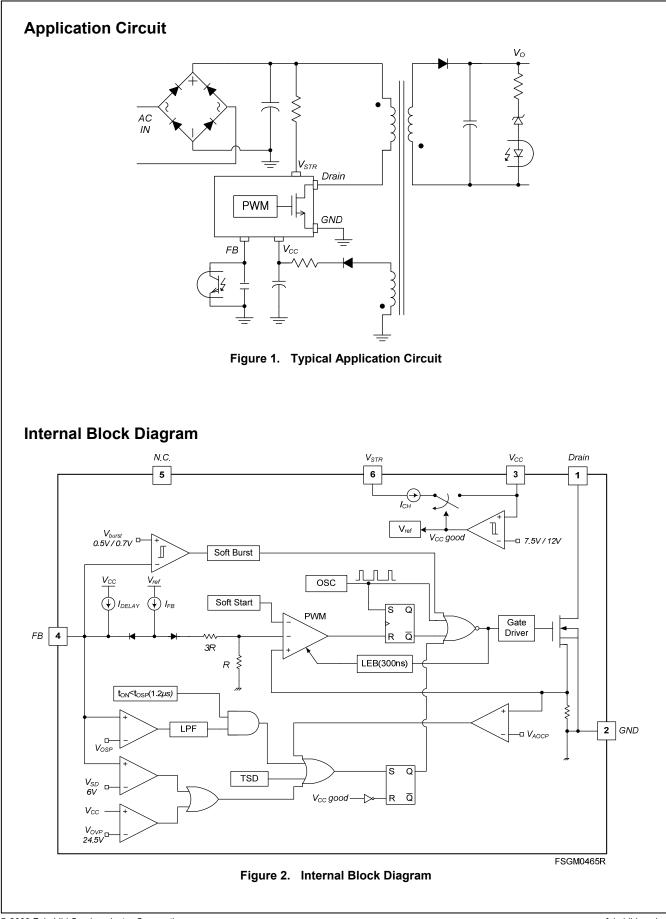
Fairchild Power Supply WebDesigner — Flyback Design & Simulation - In Minutes at No Expense

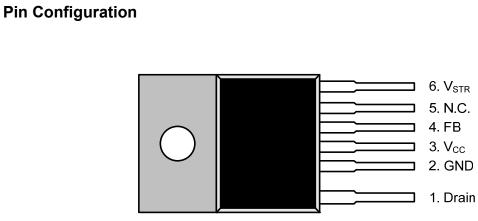
		Operating			C				
Part Number	Package	Operating Junction	Current		R _{DS(ON)} 230V _{AC} ± 15% ⁽³⁾		85-265V _{AC}		Replaces
	l denuge	Temperature	Limit	(Max.)		Open Frame ⁽⁵⁾	Adapter ⁽⁴⁾	Open Frame ⁽⁵⁾	Device
FSGM0465RWDTU	TO-220F 6-Lead ⁽¹⁾ W- Forming	-40°C ~ +125°C	1.80A	2.6Ω	60W	70W	33W	48W	FSDM0465RE
FSGM0465RUDTU	TO-220F 6-Lead ⁽¹⁾ U-Forming	-40°C ~ +125°C	1.80A	2.6Ω	60W	70W	33W	48W	FSDM0465RE
FSGM0465RLDTU	TO-220F 6-Lead ⁽¹⁾ L-Forming	-40°C ~ +125°C	1.80A	2.6Ω	60W	70W	33W	48W	FSDM0465RE

Ordering Information

Notes:

- 1. Pb-free package per JEDEC J-STD-020B.
- 2. The junction temperature can limit the maximum output power.
- 3. $230V_{AC}$ or $100/115V_{AC}$ with voltage doubler.
- 4. Typical continuous power in a non-ventilated enclosed adapter measured at 50°C ambient temperature.
- 5. Maximum practical continuous power in an open-frame design at 50°C ambient temperature.





FSGM0465R

Figure 3. Pin Configuration (Top View)

Pin Definitions

Pin #	Name	Description
1	Drain	SenseFET Drain. High-voltage power SenseFET drain connection.
2	GND	Ground. This pin is the control ground and the SenseFET source.
3	V _{cc}	Power Supply . This pin is the positive supply input, which provides the internal operating current for both startup and steady-state operation.
4	FB	Feedback . This pin is internally connected to the inverting input of the PWM comparator. The collector of an opto-coupler is typically tied to this pin. For stable operation, a capacitor should be placed between this pin and GND. If the voltage of this pin reaches 6V, the overload protection triggers, which shuts down the FPS.
5	N.C.	No connection.
6	V _{STR}	Startup . This pin is connected directly, or through a resistor, to the high-voltage DC link. At startup, the internal high-voltage current source supplies internal bias and charges the external capacitor connected to the V_{CC} pin. Once V_{CC} reaches 12V, the internal current source (I_{CH}) is disabled.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol		Min.	Max.	Unit		
V _{STR}	V _{STR} Pin Voltage				650	V
V _{DS}	Drain Pin Voltage				650	V
V _{CC}	V _{CC} Pin Voltage				26	V
V _{FB}	Feedback Pin Voltage			-0.3	12.0	V
I _{DM}	Drain Current Pulsed				10	А
	Continuous Switching	Drain Current ⁽⁶⁾	T _C =25°C		5.0	А
I _{DS}	Continuous Switching	Drain Current	T _C =100°C		3.2	А
E _{AS}	Single Pulsed Avalanc		250	mJ		
PD	Total Power Dissipatio	n(T _C =25°C) ⁽⁸⁾			45	W
-	Maximum Junction Ter	mperature			150	°C
TJ	Operating Junction Te	mperature ⁽⁹⁾		-40	+125	°C
T _{STG}	Storage Temperature	Storage Temperature				°C
V _{ISO}	Minimum Isolation Voltage ⁽¹⁰⁾			2.5		kV
	Electrostatic	ElectrostaticHuman Body Model, JESD22-A114Discharge CapabilityCharged Device Model, JESD22-C101				
ESD	Discharge Capability					- kV

Notes:

 Repetitive peak switching current when the inductive load is assumed: Limited by maximum duty (D_{MAX}=0.75) and junction temperature (see Figure 4).

7. L=45mH, starting T_J =25°C.

8. Infinite cooling condition (refer to the SEMI G30-88).

- 9. Although this parameter guarantees IC operation, it does not guarantee all electrical characteristics.
- 10. The voltage between the package back side and the lead is guaranteed.

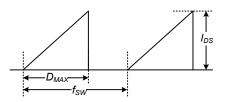


Figure 4. Repetitive Peak Switching Current

Thermal Impedance

 T_A =25°C unless otherwise specified.

Symbol	Parameter	Value	Unit
θ_{JA}	Junction-to-Ambient Thermal Impedance ⁽¹¹⁾	62.5	°C/W
θ_{JC}	Junction-to-Case Thermal Impedance ⁽¹²⁾	3	°C/W

Notes:

11. Infinite cooling condition (refer to the SEMI G30-88).

12. Free standing with no heat-sink under natural convection.

Electrical Characteristics

 T_J = 25°C unless otherwise specified.

Symbol	Parameter		Conditions	Min.	Тур.	Max.	Unit
SenseFET	Section						
BV _{DSS}	Drain-Source B	Breakdown Voltage	$V_{CC} = 0V, I_{D} = 250 \mu A$	650			V
I _{DSS}	Zero-Gate-Voltage Drain Current		V _{DS} = 520V, T _A = 125°C			250	μA
R _{DS(ON)}	Drain-Source C	Dn-State Resistance	V _{GS} =10V, I _D =1A		2.1	2.6	Ω
C _{ISS}	Input Capacitar	nce ⁽¹³⁾	V_{DS} = 25V, V_{GS} = 0V,f=1MHz		436		pF
C _{OSS}	Output Capacit	ance ⁽¹³⁾	V_{DS} = 25V, V_{GS} = 0V,f=1MHz		65		pF
t _r	Rise Time		V_{DS} = 325V, I_{D} = 4A, R_{G} =25 Ω		24		ns
t _f	Fall Time		V_{DS} = 325V, I_{D} = 4A, R_{G} =25 Ω		24		ns
t _{d(on)}	Turn-on Delay	Time	V_{DS} = 325V, I_{D} = 4A, R_{G} =25 Ω		13		ns
t _{d(off)}	Turn-off Delay	Time	V_{DS} = 325V, I_{D} = 4A, R_{G} =25 Ω		30		ns
Control Sec	ction						
f _S	Switching Freq	uency	$V_{CC} = 14V, V_{FB} = 4V,$	60	66	72	kHz
Δf_S	Switching Frequency Variation ⁽¹³⁾		−25°C < T _J < +125°C		±5	±10	%
D _{MAX}	Maximum Duty Ratio		V _{CC} = 14V, V _{FB} = 4V	65	70	75	%
D _{MIN}	Minimum Duty Ratio		V _{CC} = 14V, V _{FB} = 0V			0	%
I _{FB}	Feedback Source Current		V _{FB} = 0	160	210	260	μA
V _{START}	UVLO Threshold Voltage		V_{FB} = 0V, V_{CC} Sweep	11	12	13	V
V _{STOP}			After Turn-on, V _{FB} = 0V	7.0	7.5	8.0	V
V _{OP}	V _{CC} Operating Range			13		23	V
t _{S/S}	Internal Soft-St	art Time	V _{STR} = 40V, V _{CC} Sweep		15		ms
Burst-Mode	Section						
V _{BURH}				0.6	0.7	0.8	V
V _{BURL}	Burst-Mode Vo	Itage	V _{CC} = 14V, V _{FB} Sweep	0.4	0.5	0.6	V
Hys	-				200		mV
Protection	Section						
I _{LIM}	Peak Drain Cu	rrent Limit	di/dt = 300mA/µs	1.64	1.80	1.96	Α
V_{SD}	Shutdown Feed	dback Voltage	V _{CC} = 14V, V _{FB} Sweep	5.5	6.0	6.5	V
I _{DELAY}	Shutdown Dela	y Current	V _{CC} = 14V, V _{FB} = 4V	2.5	3.3	4.1	μA
t_{LEB}	Leading-Edge I	Blanking Time ⁽¹³⁾⁽¹⁴⁾			300		ns
V _{OVP}	Over-Voltage F	Protection	V _{CC} Sweep	23.0	24.5	26.0	V
t _{OSP}		Threshold Time	OSP Triggered when t _{on} <t<sub>osp</t<sub>	1.0	1.2	1.4	μs
V _{OSP}	Output Short Protection ⁽¹³⁾	Threshold V _{FB}	& V _{FB} >V _{OSP}	1.8	2.0	2.2	V
t _{OSP_FB}		V _{FB} Blanking Time	(Lasts Longer than t _{OSP_FB})	2.0	2.5	3.0	μs
T _{SD}	The second second	.	Shutdown Temperature	130	140	150	°C
Hys	- Thermal Shutde	own Temperature ⁽¹³⁾	Hysteresis		30		°C

Continued on the following page...

5

Electrical Characteristics (Continued)

 T_J = 25°C unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit		
Total Devic	Fotal Device Section							
I _{OP}	Operating Supply Current, (Control Part in Burst Mode)	V _{CC} = 14V, V _{FB} = 0V	1.2	1.6	2.0	mA		
I _{OPS}	Operating Switching Current, (Control Part and SenseFET Part)	V_{CC} = 14V, V_{FB} = 4V	2.0	2.5	3.0	mA		
I _{START}	Start Current	V_{CC} = 11V (Before V_{CC} Reaches V_{START})	0.5	0.6	0.7	mA		
I _{CH}	Startup Charging Current	$V_{CC} = V_{FB} = 0V, V_{STR} = 40V$	1.00	1.15	1.30	mA		
V_{STR}	Minimum V _{STR} Supply Voltage	$V_{CC} = V_{FB} = 0V, V_{STR}$ Sweep		26		V		

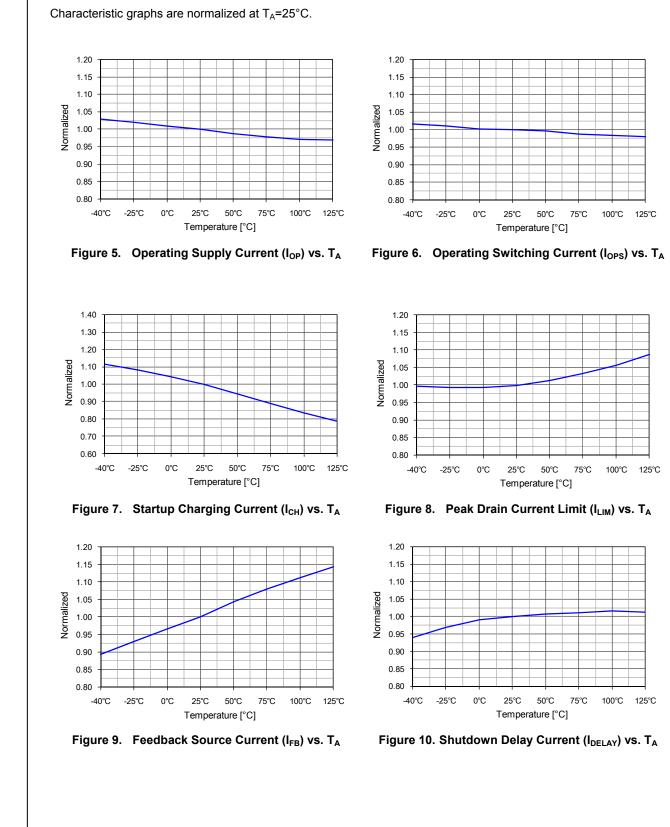
Notes:

13. Although these parameters are guaranteed, they are not 100% tested in production.

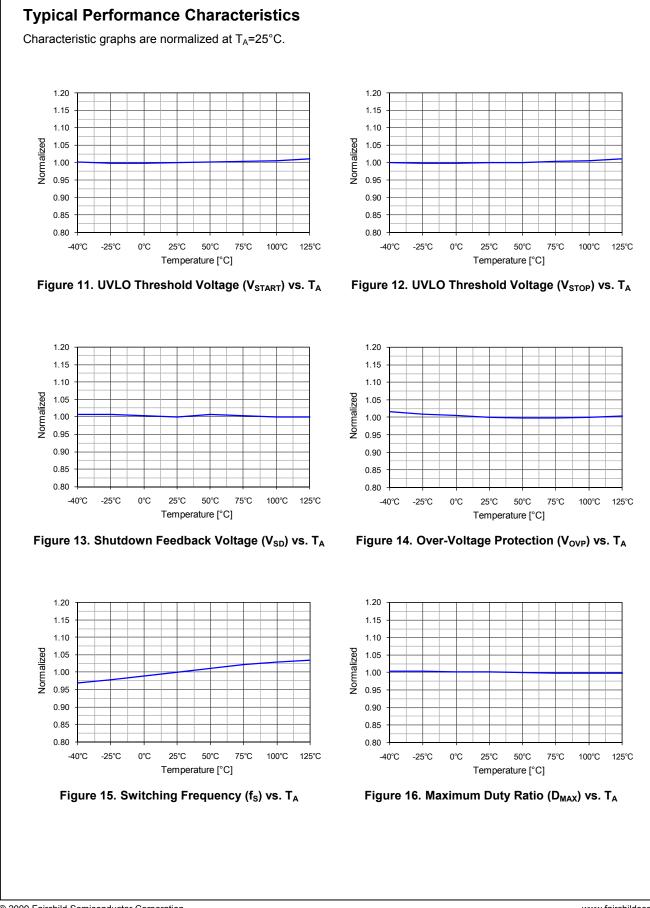
14. t_{LEB} includes gate turn-on time.

Comparison of FSDM0465RE and FSGM0465R

Function	FSDM0465RE	FSGM0465R	Advantages of FSGM0465R
Burst Mode	Advanced Burst	Advanced Soft Burst	Low noise and low standby power
Lightning Surge		Strong	Enhanced SenseFET and controller against lightning surge
Soft-Start	10ms (Built-in)	15ms (Built-in)	Longer soft-start time
		OLP	
	OLP	OVP	
Protections	OVP	OSP	Enhanced protections and high reliability
	TSD	AOCP	
		TSD with Hysteresis	
Power Balance	Long T _{CLD}	Very Short T_{CLD}	The difference of input power between the low and high input voltage is quite small



Typical Performance Characteristics



Functional Description

1. Startup: At startup, an internal high-voltage current source supplies the internal bias and charges the external capacitor (C_{Vcc}) connected to the V_{CC} pin, as illustrated in Figure 17. When V_{CC} reaches 12V, the FSGM0465R begins switching and the internal high-voltage current source is disabled. The FSGM0465R continues normal switching operation and the power is supplied from the auxiliary transformer winding unless V_{CC} goes below the stop voltage of 7.5V.

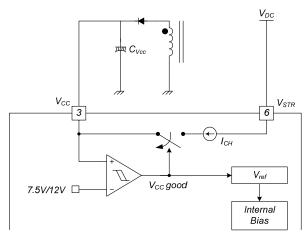


Figure 17. Startup Block

2. Soft-Start: The FSGM0465R has an internal softstart circuit that increases PWM comparator inverting input voltage, together with the SenseFET current, slowly after it starts. The typical soft-start time is 15ms. The pulse width to the power switching device is progressively increased to establish the correct working conditions for transformers, inductors, and capacitors. The voltage on the output capacitors is progressively increased to smoothly establish the required output voltage. This helps prevent transformer saturation and reduces stress on the secondary diode during startup. **3. Feedback Control**: This device employs currentmode control, as shown in Figure 18. An opto-coupler (such as the FOD817) and shunt regulator (such as the KA431) are typically used to implement the feedback network. Comparing the feedback voltage with the voltage across the R_{SENSE} resistor makes it possible to control the switching duty cycle. When the reference pin voltage of the shunt regulator exceeds the internal reference voltage of 2.5V, the opto-coupler LED current increases, pulling down the feedback voltage and reducing drain current. This typically occurs when the input voltage is increased or the output load is decreased.

3.1 Pulse-by-Pulse Current Limit: Because currentmode control is employed, the peak current through the SenseFET is limited by the inverting input of PWM comparator (V_{FB}*), as shown in Figure 18. Assuming that the 210 μ A current source flows only through the internal resistor (3R + R =11.6k Ω), the cathode voltage of diode D2 is about 2.4V. Since D1 is blocked when the feedback voltage (V_{FB}) exceeds 2.4V, the maximum voltage of the cathode of D2 is clamped at this voltage. Therefore, the peak value of the current through the SenseFET is limited.

3.2 Leading-Edge Blanking (LEB): At the instant the internal SenseFET is turned on, a high-current spike usually occurs through the SenseFET, caused by primary-side capacitance and secondary-side rectifier reverse recovery. Excessive voltage across the R_{SENSE} resistor leads to incorrect feedback operation in the current mode PWM control. To counter this effect, the FSGM0465R employs a leading-edge blanking (LEB) circuit. This circuit inhibits the PWM comparator for t_{LEB} (300ns) after the SenseFET is turned on.

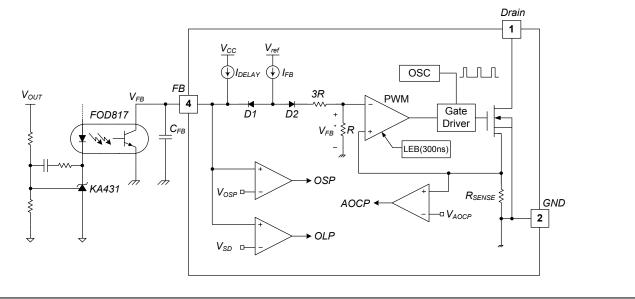


Figure 18. Pulse Width Modulation Circuit

4. Protection Circuits: The FSGM0465R has several self-protective functions, such as Overload Protection (OLP), Abnormal Over-Current Protection (AOCP), Output-Short Protection (OSP), Over-Voltage Protection (OVP), and Thermal Shutdown (TSD). All the protections are implemented as auto-restart. Once the fault condition is detected, switching is terminated and the SenseFET remains off. This causes V_{CC} to fall. When V_{CC} falls to the Under-Voltage Lockout (UVLO) stop voltage of 7.5V, the protection is reset and the startup circuit charges the V_{CC} capacitor. When V_{CC} reaches the start voltage of 12.0V, the FSGM0465R resumes normal operation. If the fault condition is not removed, the SenseFET remains off and V_{CC} drops to stop voltage again. In this manner, the auto-restart can alternately enable and disable the switching of the power SenseFET until the fault condition is eliminated. Because these protection circuits are fully integrated into the IC without external components, the reliability is improved without increasing cost.

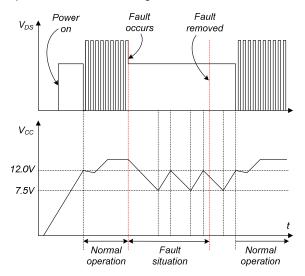


Figure 19. Auto-Restart Protection Waveforms

4.1 Overload Protection (OLP): Overload is defined as the load current exceeding its normal level due to an unexpected abnormal event. In this situation, the protection circuit should trigger to protect the SMPS. However, even when the SMPS is in normal operation, the overload protection circuit can be triggered during the load transition. To avoid this undesired operation, the overload protection circuit is designed to trigger only after a specified time to determine whether it is a transient situation or a true overload situation. Because of the pulse-by-pulse current limit capability, the maximum peak current through the SenseFET is limited and, therefore, the maximum input power is restricted with a given input voltage. If the output consumes more than this maximum power, the output voltage (V_{OUT}) decreases below the set voltage. This reduces the current through the opto-coupler LED, which also reduces the opto-coupler transistor current, thus increasing the feedback voltage (V_{FB}). If V_{FB} exceeds 2.4V, D1 is blocked and the $3.3\mu A$ current source starts to charge C_{FB} slowly up. In this condition, V_{FB} continues

increasing until it reaches 6.0V, when the switching operation is terminated, as shown in Figure 20. The delay time for shutdown is the time required to charge C_{FB} from 2.4V to 6.0V with 3.3μ A. A 25 ~ 50ms delay is typical for most applications. This protection is implemented in auto-restart mode.

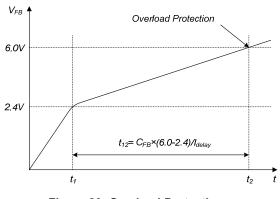


Figure 20. Overload Protection

4.2 Abnormal Over-Current Protection (AOCP): When the secondary rectifier diodes or the transformer pins are shorted, a steep current with extremely high di/dt can flow through the SenseFET during the minimum turn-on time. Even though the FSGM0465R has overload protection, it is not enough to protect the FSGM0465R in that abnormal case; since severe current stress is imposed on the SenseFET until OLP is triggered. The FSGM0465R internal AOCP circuit is shown in Figure 21. When the gate turn-on signal is applied to the power SenseFET, the AOCP block is enabled and monitors the current through the sensing resistor. The voltage across the resistor is compared with a preset AOCP level. If the sensing resistor voltage is greater than the AOCP level, the set signal is applied to the S-R latch, resulting in the shutdown of the SMPS.

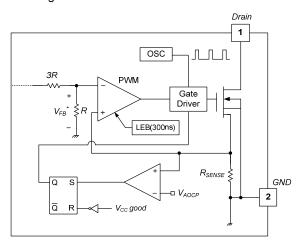
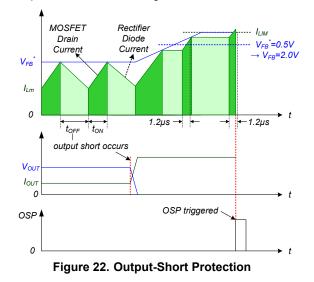


Figure 21. Abnormal Over-Current Protection

4.3. Output-Short Protection (OSP): If the output is shorted, steep current with extremely high di/dt can flow through the SenseFET during the minimum turnon time. Such a steep current brings high-voltage stress on the drain of the SenseFET when turned off. To protect the device from this abnormal condition, OSP is included. It is comprised of detecting V_{FB} and SenseFET turn-on time. When the V_{FB} is higher than 2V and the SenseFET turn-on time is lower than 1.2 μ s, the FSGM0465R recognizes this condition as an abnormal error and shuts down PWM switching until V_{CC} reaches V_{START} again. An abnormal condition output short is shown in Figure 22.



4.4 Over-Voltage Protection (OVP): If the secondary-side feedback circuit malfunctions or a solder defect causes an opening in the feedback path, the current through the opto-coupler transistor becomes almost zero. Then V_{FB} climbs up in a similar manner to the overload situation, forcing the preset maximum current to be supplied to the SMPS until the overload protection is triggered. Because more energy than required is provided to the output, the output voltage may exceed the rated voltage before the overload protection is triggered, resulting in the breakdown of the devices in the secondary side. To prevent this situation, an OVP circuit is employed. In general, the V_{CC} is proportional to the output voltage and the FSGM0465R uses V_{CC} instead of directly monitoring the output voltage. If V_{CC} exceeds 24.5V, an OVP circuit is triggered, resulting in the termination of the switching operation. To avoid undesired activation of OVP during normal operation, V_{CC} should be designed to be below 24.5V.

4.5 Thermal Shutdown (TSD): The SenseFET and the control IC on a die in one package makes it easier for the control IC to detect the over temperature of the SenseFET. If the temperature exceeds ~140°C, the thermal shutdown is triggered and the FSGM0465R stops operation. The FSGM0465R operates in autorestart mode until the temperature decreases to around 110°C, when normal operation resumes.

5. Soft Burst-Mode Operation: To minimize power dissipation in standby mode, the FSGM0465R enters burst-mode operation. As the load decreases, the feedback voltage decreases. As shown in Figure 23, the device automatically enters burst mode when the feedback voltage drops below V_{BURL} (500mV). At this point, switching stops and the output voltages start to drop at a rate dependent on standby current load. This causes the feedback voltage to rise. Once it passes V_{BURH} (700mV), switching resumes. At this point, the drain current peak increases gradually. This soft burstmode can reduce audible noise during burst-mode operation. The feedback voltage then falls and the process repeats. Burst-mode operation alternately enables and disables switching of the SenseFET, thereby reducing switching loss in standby mode.

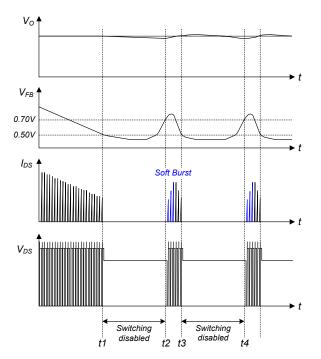


Figure 23. Burst-Mode Operation

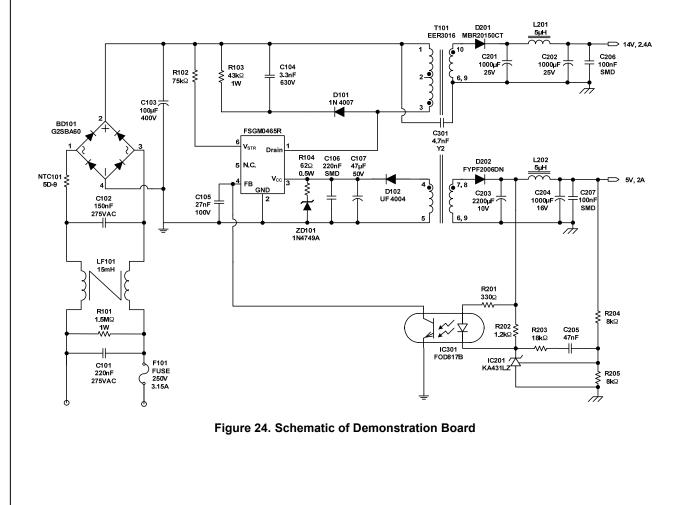
Typical Application Circuit

Application	Input Voltage	Rated Output	Rated Power
LCD TV, Monitor Power Supply	85 ~ 265V _{AC}	5.0V(2A) 14.0V(2.4A)	43.6W

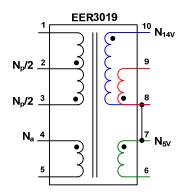
Key Design Notes:

- 1. The delay time for overload protection is designed to be about 30ms with C105 (27nF). OLP time between 25ms (22nF) and 50ms (43nF) is recommended.
- The SMD-type capacitor (C106) must be placed as close as possible to the V_{CC} pin to avoid malfunction by abrupt pulsating noises and to improve ESD and surge immunity. Capacitance between 100nF and 220nF is recommended.

1. Schematic



2. Transformer



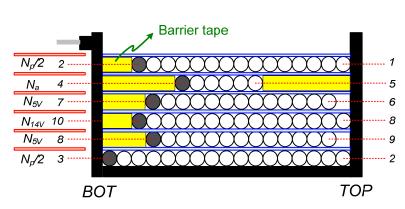


Figure 25. Schematic of Transformer

3. Winding Specification

		Wire	Turn	Winding Mathed	Ba	arrier Tape	Э
	Pin (S \rightarrow F)	vvire	S	Winding Method	ТОР	вот	Ts
N _p /2	$3 \rightarrow 2$	0.3φ×1	23	Solenoid Winding			
Insulation: Polyes	Insulation: Polyester Tape t = 0.025mm, 2 Layers						
N _{5V}	$8 \rightarrow 9$	0.4φ×2 (TIW)	3	Solenoid Winding		3.0mm	1
Insulation: Polyes	Insulation: Polyester Tape t = 0.025mm, 2 Layers						
N _{14V}	$10 \rightarrow 8$	0.4φ×2 (TIW)	5	Solenoid Winding		2.0mm	1
Insulation: Polyes	ter Tape t = 0.025	mm, 2 Layers					
N _{5V}	$7 \rightarrow 6$	0.4φ×2 (TIW)	3	Solenoid Winding		3.0mm	1
Insulation: Polyes	ter Tape t = 0.025	mm, 2 Layers					
N _a	$4 \rightarrow 5$	0.2φ×1	6	Solenoid Winding	3.0mm	4.0mm	1
Insulation: Polyes	Insulation: Polyester Tape t = 0.025mm, 2 Layers						
N _p /2	$2 \rightarrow 1$	0.3φ×1	22	Solenoid Winding		2.0mm	1
Insulation: Polyes	Insulation: Polyester Tape t = 0.025mm, 2 Layers						

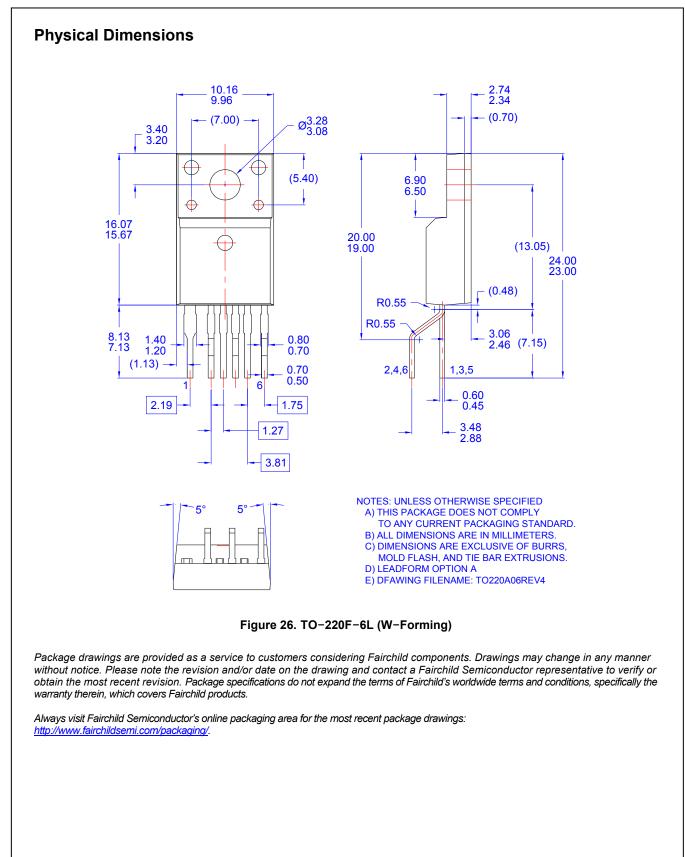
4. Electrical Characteristics

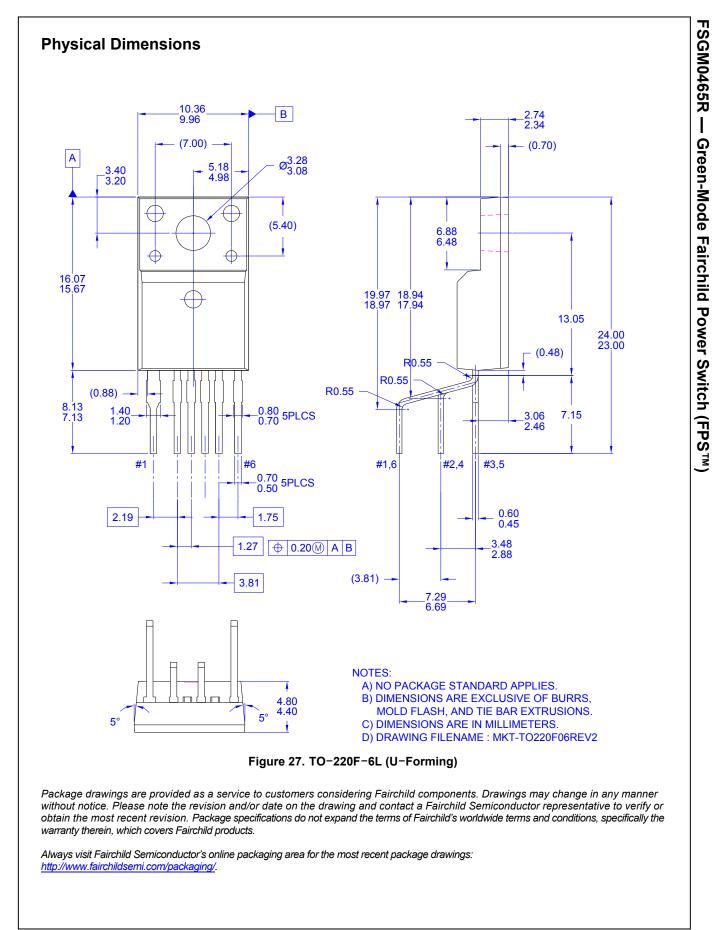
	Pin	Specification	Remark
Inductance	1—3	830μH ± 7%	67kHz, 1V
Leakage	1–3	15μH Maximum	Short All Other Pins

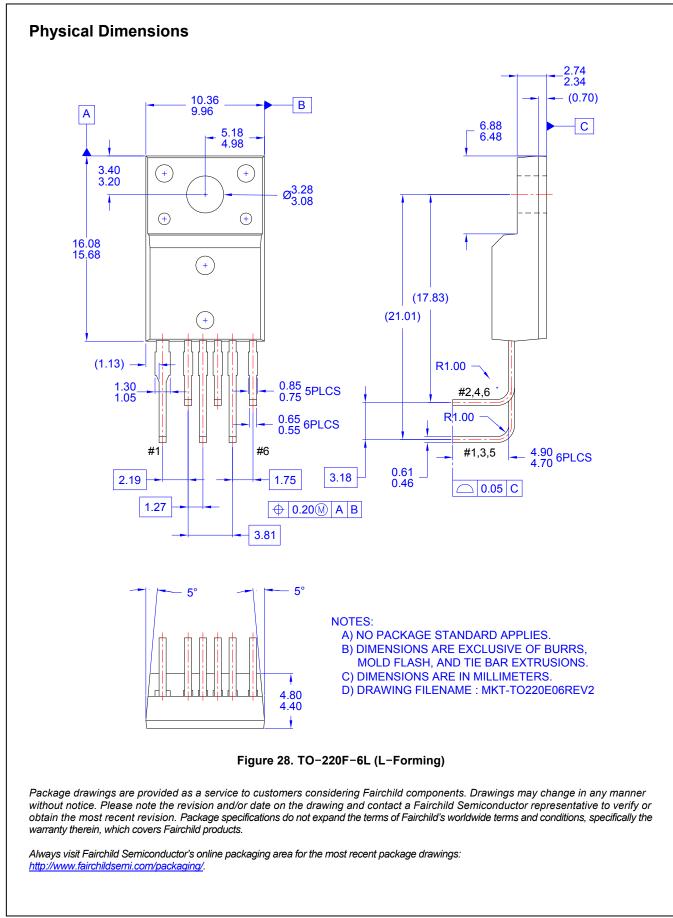
5. Core & Bobbin

- Core: EER3019 (Ae=134.0mm²)
- Bobbin: EER3019

Part #	Value	Note	Part #	Value	Note
Fuse				Capacitor	
F101	250V 3.15A		C101	220nF/275V	Box (Pilkor)
	NTC		C102	150nF/275V	Box (Pilkor)
NTC101	5D-9	DSC	C103	100µF/400V	Electrolytic (SamYoung
Resistor			C104	3.3nF/630V	Film (Sehwa)
R101	1.5MΩ, J	1W	C105	27nF/100V	Film (Sehwa)
R102	75kΩ, J	1/2W	C106	220nF	SMD (2012)
R103	43kΩ, J	1W	C107	47μF/50V	Electrolytic (SamYoung
R104	62Ω, J	1/2W	C201	1000µF/25V	Electrolytic (SamYoung
R201	330Ω, F	1/4W, 1%	C202	1000µF/25V	Electrolytic (SamYoung
R202	1.2kΩ, F	1/4W, 1%	C203	2200μF/10V	Electrolytic (SamYoung
R203	18kΩ, F	1/4W, 1%	C204	1000µF/16V	Electrolytic (SamYoun
R204	8kΩ, F	1/4W, 1%	C205	47nF/100V	Film (Sehwa)
R205	8kΩ, F	1/4W, 1%	C206	100nF	SMD (2012)
	IC		C207	100nF	SMD (2012)
FSGM0465R	FSGM0465R	Fairchild Semiconductor	C301	4.7nF/Y2	Y-cap (Samhwa)
IC201	KA431LZ	Fairchild Semiconductor		Inductor	
IC301	FOD817B	Fairchild Semiconductor	LF101	15mH	Line filter 0.5Ø
	Diode		L201	5μΗ	5A Rating
D101	1N4007	Vishay	L202	5μΗ	5A Rating
D102	UF4004	Vishay		Jumper	
ZD101	1N4749	Vishay	J101		
D201	MBR20150CT	Fairchild Semiconductor		Transformer	
D202	FYPF2006DN	Fairchild Semiconductor	Τ101 830μΗ		
BD101	G2SBA60	Vishay			







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