June 2007

**Motion-SPM**<sup>™</sup>

# FAIRCHILD

SEMICONDUCTOR®

# FSBF10CH60B Smart Power Module

# Features

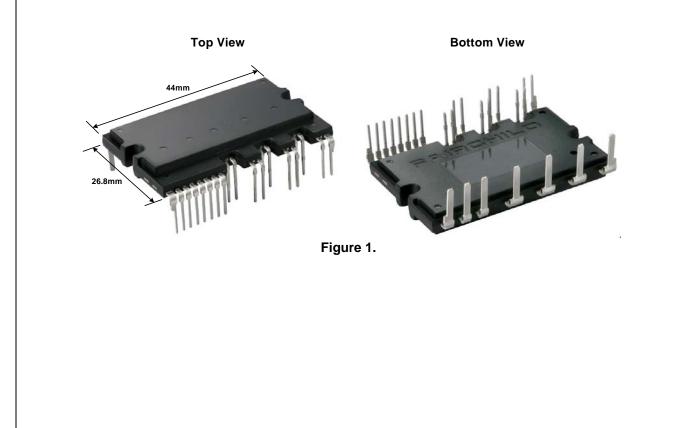
- UL Certified No.E209204(SPM27-JA package)
- 600V-10A 3-phase IGBT inverter bridge including control ICs for gate driving and protection
- Easy PCB layout due to built in bootstrap diode
- Divided negative dc-link terminals for inverter current sensing applications
- Single-grounded power supply due to built-in HVIC
- Isolation rating of 2500Vrms/min.

# Applications

- AC 100V ~ 253V three-phase inverter drive for small power ac motor drives
- Home appliances applications like air conditioner and washing machine

### **General Description**

It is an advanced motion-smart power module (Motion-SPM<sup>™</sup>) that Fairchild has newly developed and designed to provide very compact and high performance ac motor drives mainly targeting low-power inverter-driven application like air conditioner and washing machine. It combines optimized circuit protection and drive matched to low-loss IGBTs. System reliability is further enhanced by the integrated under-voltage lock-out and short-circuit protection. The high speed built-in HVIC provides opto-coupler-less single-supply IGBT gate driving capability that further reduce the overall size of the inverter system design. Each phase current of inverter can be monitored separately due to the divided negative dc terminals.



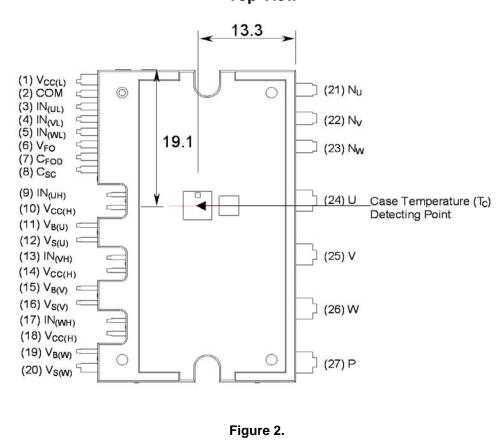
### **Integrated Power Functions**

• 600V-10A IGBT inverter for three-phase DC/AC power conversion (Please refer to Figure 3)

### Integrated Drive, Protection and System Control Functions

- For inverter high-side IGBTs: Gate drive circuit, High voltage isolated high-speed level shifting Control circuit under-voltage (UV) protection Note) Available bootstrap circuit example is given in Figures 12 and 13.
- For inverter low-side IGBTs: Gate drive circuit, Short circuit protection (SC) Control supply circuit under-voltage (UV) protection
- Fault signaling: Corresponding to UV (Low-side supply) and SC faults
- Input interface: 3.3/5V CMOS/LSTTL compatible, Schmitt trigger input

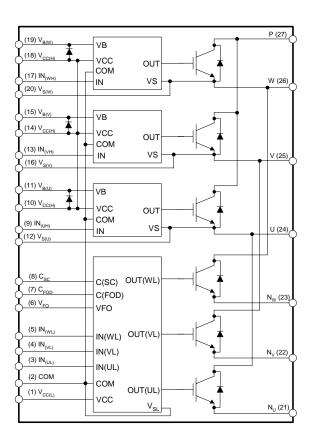
### **Pin Configuration**



# **Top View**

Pin Number	Pin Name	Pin Description	
1	V <sub>CC(L)</sub>	Low-side Common Bias Voltage for IC and IGBTs Driving	
2	СОМ	Common Supply Ground	
3	IN <sub>(UL)</sub>	Signal Input for Low-side U Phase	
4	IN <sub>(VL)</sub>	Signal Input for Low-side V Phase	
5	IN <sub>(WL)</sub>	Signal Input for Low-side W Phase	
6	V <sub>FO</sub>	Fault Output	
7	C <sub>FOD</sub>	Capacitor for Fault Output Duration Time Selection	
8	C <sub>SC</sub>	Capacitor (Low-pass Filter) for Short-Current Detection Input	
9	IN <sub>(UH)</sub>	Signal Input for High-side U Phase	
10	V <sub>CC(H)</sub>	High-side Common Bias Voltage for IC and IGBTs Driving	
11	V <sub>B(U)</sub>	High-side Bias Voltage for U Phase IGBT Driving	
12	V <sub>S(U)</sub>	High-side Bias Voltage Ground for U Phase IGBT Driving	
13	IN <sub>(VH)</sub>	Signal Input for High-side V Phase	
14	V <sub>CC(H)</sub>	High-side Common Bias Voltage for IC and IGBTs Driving	
15	V <sub>B(V)</sub>	High-side Bias Voltage for V Phase IGBT Driving	
16	V <sub>S(V)</sub>	High-side Bias Voltage Ground for V Phase IGBT Driving	
17	IN <sub>(WH)</sub>	Signal Input for High-side W Phase	
18	V <sub>CC(H)</sub>	High-side Common Bias Voltage for IC and IGBTs Driving	
19	V <sub>B(W)</sub>	High-side Bias Voltage for W Phase IGBT Driving	
20	V <sub>S(W)</sub>	High-side Bias Voltage Ground for W Phase IGBT Driving	
21	NU	Negative DC-Link Input for U Phase	
22	N <sub>V</sub>	Negative DC-Link Input for V Phase	
23	N <sub>W</sub>	Negative DC-Link Input for W Phase	
24	U	Output for U Phase	
25	V	Output for V Phase	
26	W	Output for W Phase	
27	Р	Positive DC-Link Input	

# Internal Equivalent Circuit and Input/Output Pins



#### Note:

1. Inverter low-side is composed of three IGBTs, freewheeling diodes for each IGBT and one control IC. It has gate drive and protection functions.

2. Inverter power side is composed of four inverter dc-link input terminals and three inverter output terminals.

3. Inverter high-side is composed of three IGBTs, freewheeling diodes and three drive ICs for each IGBT.



4

## Absolute Maximum Ratings (T<sub>J</sub> = 25°C, Unless Otherwise Specified)

### **Inverter Part**

Symbol	Parameter Conditions		Rating	Units
V <sub>PN</sub>	Supply Voltage	Applied between P- $N_U$ , $N_V$ , $N_W$	450	V
V <sub>PN(Surge)</sub>	Supply Voltage (Surge)	Applied between P- $N_U$ , $N_V$ , $N_W$	500	V
V <sub>CES</sub>	Collector-emitter Voltage		600	V
± I <sub>C</sub>	Each IGBT Collector Current	$T_{\rm C} = 25^{\circ}{\rm C}$	10	А
± I <sub>CP</sub>	Each IGBT Collector Current (Peak)	$T_{C} = 25^{\circ}C$ , Under 1ms Pulse Width	20	А
P <sub>C</sub>	Collector Dissipation	T <sub>C</sub> = 25°C per One Chip	22	W
Τ <sub>J</sub>	Operating Junction Temperature	(Note 1)	-40 ~ 150	°C

Note:

1. The maximum junction temperature rating of the power chips integrated within the SPM is  $150^{\circ}C(@T_{C} \le 125^{\circ}C)$ .

#### **Control Part**

Symbol	Parameter	Conditions	Rating	Units
V <sub>CC</sub>	Control Supply Voltage	Applied between V <sub>CC(H)</sub> , V <sub>CC(L)</sub> - COM	20	V
V <sub>BS</sub>	High-side Control Bias Voltage	Applied between $V_{B(U)}$ - $V_{S(U)}$ , $V_{B(V)}$ - $V_{S(V)}$ , $V_{B(W)}$ - $V_{S(W)}$	20	V
V <sub>IN</sub>	Input Signal Voltage	$\begin{array}{llllllllllllllllllllllllllllllllllll$	-0.3~17	V
V <sub>FO</sub>	Fault Output Supply Voltage	Applied between V <sub>FO</sub> - COM	-0.3~V <sub>CC</sub> +0.3	V
I <sub>FO</sub>	Fault Output Current	Sink Current at V <sub>FO</sub> Pin	5	mA
V <sub>SC</sub>	Current Sensing Input Voltage	Applied between C <sub>SC</sub> - COM	-0.3~V <sub>CC</sub> +0.3	V

### **Bootstrap Diode Part**

Symbol	ol Parameter Conditions		Rating	Units
V <sub>RRM</sub>	Maixmum Repetitive Reverse Voltage		600	V
١ <sub>F</sub>	Forward Current	$T_{\rm C} = 25^{\circ}{\rm C}$	0.5	А
I <sub>FP</sub>	Forward Current (Peak)	$T_{C} = 25^{\circ}C$ , Under 1ms Pulse Width	2	А
TJ	Operating Junction Temperature		-40 ~ 150	°C

### **Total System**

Symbol	Parameter	Conditions	Rating	Units
V <sub>PN(PROT)</sub>	Self Protection Supply Voltage Limit (Short Circuit Protection Capability)	$V_{CC} = V_{BS} = 13.5 \sim 16.5 V$ T <sub>J</sub> = 150°C, Non-repetitive, less than 2µs	400	V
T <sub>C</sub>	Module Case Operation Temperature	-40°C $\leq$ T <sub>J</sub> $\leq$ 150°C, See Figure 2	-40 ~ 125	°C
T <sub>STG</sub>	Storage Temperature		-40 ~ 150	°C
V <sub>ISO</sub>	Isolation Voltage	60Hz, Sinusoidal, AC 1 minute, Connection Pins to heat sink plate	2500	V <sub>rms</sub>

### Thermal Resistance

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Units
R <sub>th(j-c)Q</sub>	Junction to Case Thermal	Inverter IGBT part (per 1/6 module)	-	-	5.5	°C/W
R <sub>th(j-c)F</sub>	Resistance	Inverter FWD part (per 1/6 module)	-	-	6.3	°C/W

Note:

2. For the measurement point of case temperature(T\_C), please refer to Figure 2.

## Electrical Characteristics (T<sub>J</sub> = 25°C, Unless Otherwise Specified)

### **Inverter Part**

S	ymbol	Parameter	Cond	itions	Min.	Тур.	Max.	Units
V	CE(SAT)	Collector-Emitter Saturation Voltage	$V_{CC} = V_{BS} = 15V \qquad I_C = 10A, T_J = 25^{\circ}C \\ V_{IN} = 5V \qquad I_C = 10A, T_J = 25^{\circ}C $		-	-	2.0	V
	V <sub>F</sub>	FWD Forward Voltage	$V_{IN} = 0V$	I <sub>F</sub> = 10A, T <sub>J</sub> = 25°C	-	-	2.1	V
HS	t <sub>ON</sub>	Switching Times	V <sub>PN</sub> = 300V, V <sub>CC</sub> = V <sub>BS</sub> = 15V		-	0.75	-	μs
	t <sub>C(ON)</sub>		$I_{C} = 10A$ $V_{IN} = 0V \leftrightarrow 5V$ , Inducti	veload	-	0.15	-	μs
	t <sub>OFF</sub>		(Note 3)		-	0.60	-	μs
	t <sub>C(OFF)</sub>				-	0.15	-	μs
	t <sub>rr</sub>				-	0.10	-	μs
LS	t <sub>ON</sub>	Ī	$V_{PN} = 300V, V_{CC} = V_{B2}$	<sub>S</sub> = 15V	-	0.50	-	μs
	t <sub>C(ON)</sub>		$I_{C} = 10A$ $V_{IN} = 0V \leftrightarrow 5V$ , Inducti	veload	-	0.20	-	μs
	t <sub>OFF</sub>		(Note 3) $(Note 3)$	ve Load	-	0.55	-	μS
	t <sub>C(OFF)</sub>	]			-	0.15	-	μs
	t <sub>rr</sub>				-	0.10	-	μs
	I <sub>CES</sub>	Collector-Emitter Leakage Current	$V_{CE} = V_{CES}$		-	-	1	mA

Note:

3. t<sub>ON</sub> and t<sub>OFF</sub> include the propagation delay time of the internal drive IC. t<sub>C(ON)</sub> and t<sub>C(OFF)</sub> are the switching time of IGBT itself under the given gate driving condition internally. For the detailed information, please see Figure 4.

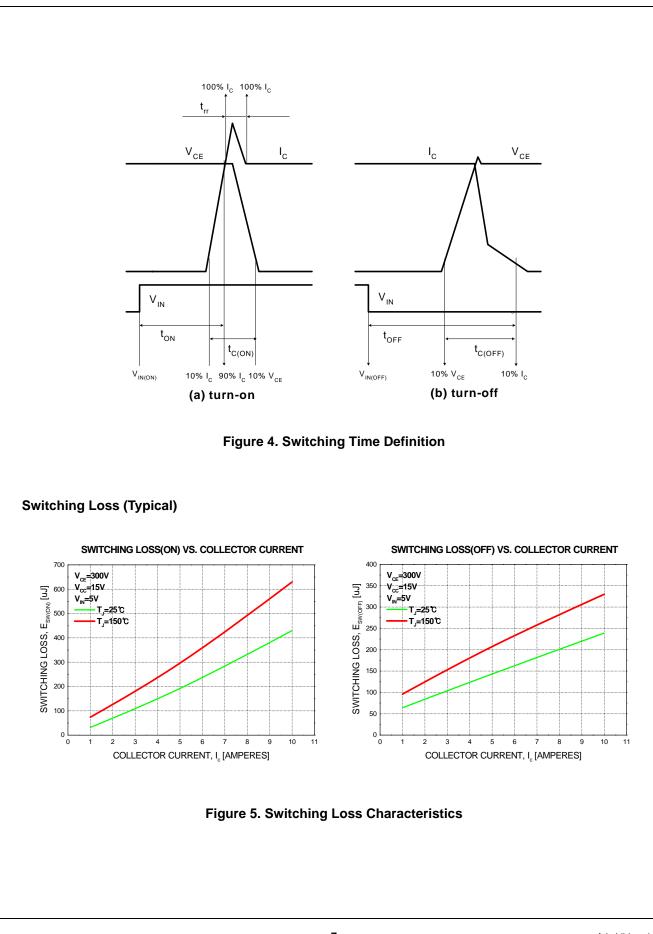
#### **Control Part**

Symbol	Parameter	Co	nditions	Min.	Тур.	Max.	Units
I <sub>QCCL</sub>	Quiescent V <sub>CC</sub> Supply Current	V <sub>CC</sub> = 15V IN <sub>(UL, VL, WL)</sub> = 0V	V <sub>CC(L)</sub> - COM	-	-	23	mA
IQCCH		V <sub>CC</sub> = 15V IN <sub>(UH, VH, WH)</sub> = 0V	V <sub>CC(H)</sub> - COM	-	-	600	μΑ
I <sub>QBS</sub>	Quiescent V <sub>BS</sub> Supply Current	V <sub>BS</sub> = 15V IN <sub>(UH, VH, WH)</sub> = 0V	$ \begin{array}{c} V_{B(U)} \ - \ V_{S(U)}, \ V_{B(V)} \ - \ V_{S(V)}, \\ V_{B(W)} \ - \ V_{S(W)} \end{array} $	-	-	500	μΑ
V <sub>FOH</sub>	Fault Output Voltage	V <sub>SC</sub> = 0V, V <sub>FO</sub> Circu	it: 4.7kΩ to 5V Pull-up	4.5	-	-	V
V <sub>FOL</sub>		V <sub>SC</sub> = 1V, V <sub>FO</sub> Circu	$V_{SC}$ = 1V, $V_{FO}$ Circuit: 4.7k $\Omega$ to 5V Pull-up		-	0.8	V
V <sub>SC(ref)</sub>	Short Circuit Trip Level	V <sub>CC</sub> = 15V (Note 4)		0.45	0.5	0.55	V
TSD	Over-temperature protec- tion	Temperature at LVIC		-	160	-	°C
∆TSD	Over-temperature protec- tion hysterisis	Temperature at LVIC	;	-	5	-	°C
UV <sub>CCD</sub>	Supply Circuit Under-	Detection Level		10.7	11.9	13.0	V
UV <sub>CCR</sub>	Voltage Protection	Reset Level		11.2	12.4	13.4	V
UV <sub>BSD</sub>		Detection Level		10	11	12	V
UV <sub>BSR</sub>		Reset Level		10.5	11.5	12.5	V
t <sub>FOD</sub>	Fault-out Pulse Width	C <sub>FOD</sub> = 33nF (Note 5)		1.0	1.8	-	ms
V <sub>IN(ON)</sub>	ON Threshold Voltage	Applied between IN(UH), IN(VH), IN(WH), IN(UL),		2.8	-	-	V
V <sub>IN(OFF)</sub>	OFF Threshold Voltage	IN <sub>(VL)</sub> , IN <sub>(WL)</sub> - COM		-	-	0.8	V

Note:

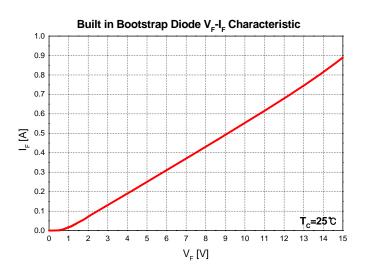
4. Short-circuit current protection is functioning only at the low-sides.

5. The fault-out pulse width  $t_{FOD}$  depends on the capacitance value of  $C_{FOD}$  according to the following approximate equation :  $C_{FOD} = 18.3 \times 10^{-6} \times t_{FOD}[F]$ 



### **Bootstrap Diode Part**

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Units
V <sub>F</sub>	Forward Voltage	I <sub>F</sub> = 0.1A, T <sub>C</sub> = 25°C	-	2.5	-	V
t <sub>rr</sub>	Reverse Recovery Time	I <sub>F</sub> = 0.1A, T <sub>C</sub> = 25°C	-	80	-	ns



Note:

6. Built in bootstrap diode includes around  $15 \! \Omega$  resistance characteristic.

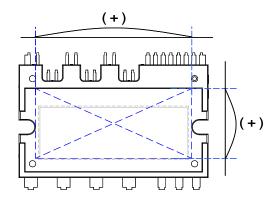


## **Recommended Operating Conditions**

Symbol	Parameter	Conditions		Value		Units	
Symbol	Farameter	Conditions	Min. Typ. Max		Max.		
V <sub>PN</sub>	Supply Voltage	Applied between P - N <sub>U</sub> , N <sub>V</sub> , N <sub>W</sub>	-	300	400	V	
V <sub>CC</sub>	Control Supply Voltage	Applied between V <sub>CC(H)</sub> , V <sub>CC(L)</sub> - COM	13.5	15	16.5	V	
V <sub>BS</sub>	High-side Bias Voltage	Applied between V <sub>B(U)</sub> - V <sub>S(U)</sub> , V <sub>B(V)</sub> - V <sub>S(V)</sub> , V <sub>B(W)</sub> - V <sub>S(W)</sub>	13.0	15	18.5	V	
dV <sub>CC</sub> /dt, dV <sub>BS</sub> /dt	Control supply variation		-1	-	1	V/µs	
t <sub>dead</sub>	Blanking Time for Preventing Arm-short	For Each Input Signal	1.5	-	-	μS	
f <sub>PWM</sub>	PWM Input Signal	$-40^{\circ}C \leq T_C \leq 125^{\circ}C, \ -40^{\circ}C \leq T_J \leq 150^{\circ}C$	-	-	20	kHz	
V <sub>SEN</sub>	Voltage for Current Sensing	Applied between N <sub>U</sub> , N <sub>V</sub> , N <sub>W</sub> - COM (Including surge voltage)	-4		4	V	

# **Mechanical Characteristics and Ratings**

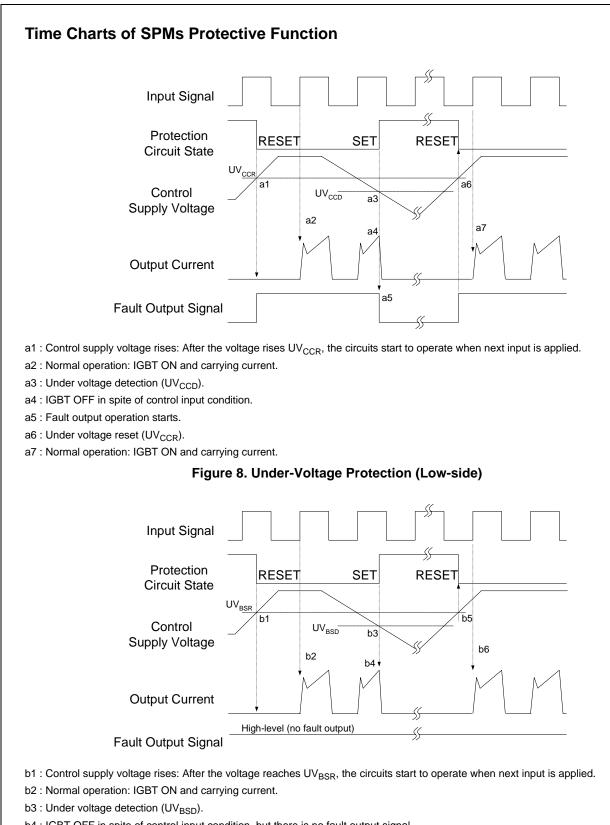
Parameter	Co	Conditions			Limits			
Farameter		lations	Min.	Тур.	Max.	Units		
Mounting Torque	Mounting Screw: - M3	Recommended 0.62N•m	0.51	0.62	1.00	N•m		
Device Flatness		Note Figure 7	0	-	+120	μm		
Weight			-	15.4	-	g		



### Figure 7. Flatness Measurement Position

# Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FSBF10CH60B	FSBF10CH60B	SPM27-JA	-	-	10

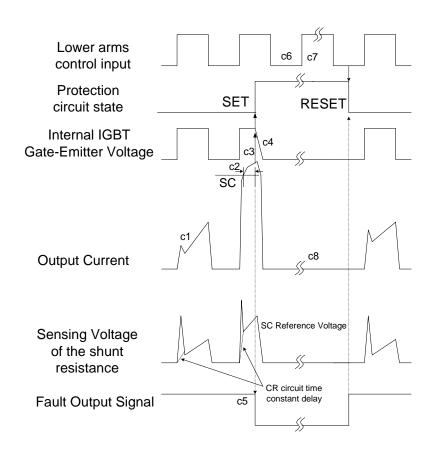


b4 : IGBT OFF in spite of control input condition, but there is no fault output signal.

b5 : Under voltage reset (UV<sub>BSR</sub>)

b6 : Normal operation: IGBT ON and carrying current

### Figure 9. Under-Voltage Protection (High-side)



(with the external shunt resistance and CR connection)

c1 : Normal operation: IGBT ON and carrying current.

c2 : Short circuit current detection (SC trigger).

c3 : Hard IGBT gate interrupt.

c4 : IGBT turns OFF.

c5 : Fault output timer operation starts: The pulse width of the fault output signal is set by the external capacitor  $C_{FO}$ .

c6 : Input "L" : IGBT OFF state.

c7 : Input "H": IGBT ON state, but during the active period of fault output the IGBT doesn't turn ON.

c8 : IGBT OFF state

Figure 10. Short-Circuit Current Protection (Low-side Operation only)

FSBF10CH60B Smart Power Module

SPM

 $IN_{(UH)},\ IN_{(VH)},\ IN_{(WH)}$ 

 $\mathrm{IN}_{(\mathrm{UL})}\,,\ \mathrm{IN}_{(\mathrm{VL})}\,,\ \mathrm{IN}_{(\mathrm{WL})}$ 

 $V_{\rm FO}$ 

COM

Note:

 RC coupling at each input might change depending on the PWM control scheme used in the application and the wiring impedance of the application's printed circuit board. The SPM input signal section integrates 5kΩ (typ.) pull-down resistor. Therefore, when using an external filtering resistor, please pay attention to the signal voltage drop at input terminal.

1nF+

1nF≑

5V-Line

R<sub>PF</sub>=4.7<sup>kΩ</sup>

 $C_{PF} = 1nF$ 

**100**Ω

**100**Ω

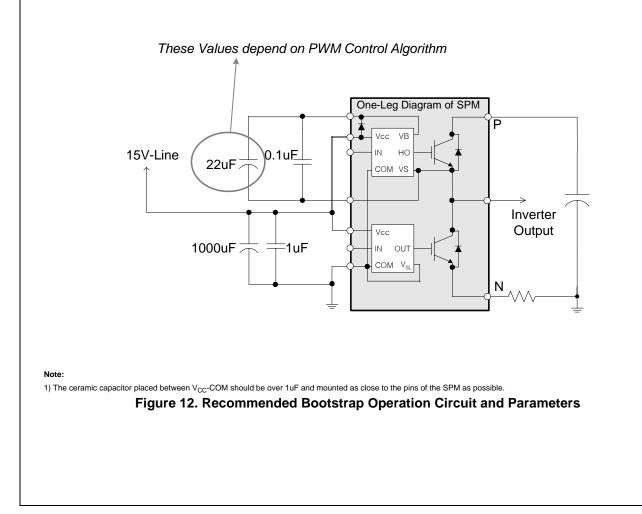
-∕∕∕∕ 100Ω

1nF

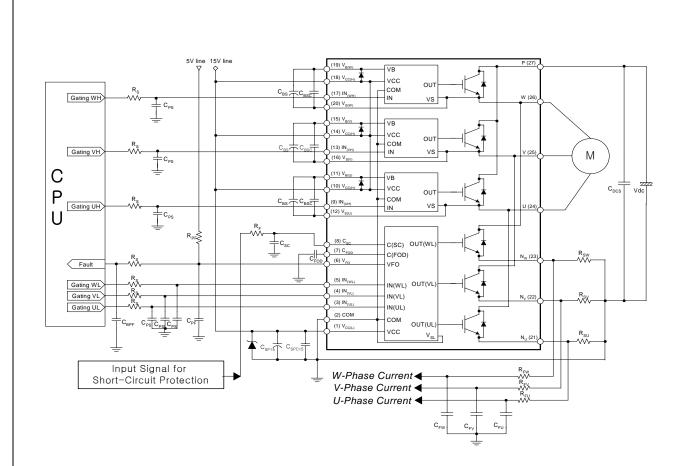
2) The logic input is compatible with standard CMOS or LSTTL outputs.

CPU

#### Figure 11. Recommended CPU I/O Interface Circuit



FSBF10CH60B Smart Power Module



#### Note:

1) To avoid malfunction, the wiring of each input should be as short as possible. (less than 2-3cm)

2) By virtue of integrating an application specific type HVIC inside the SPM, direct coupling to CPU terminals without any opto-coupler or transformer isolation is possible.

3)  $V_{FO}$  output is open collector type. This signal line should be pulled up to the positive side of the 5V power supply with approximately 4.7k $\Omega$  resistance. Please refer to Figure 11. 4)  $C_{SP15}$  of around 7 times larger than bootstrap capacitor  $C_{BS}$  is recommended.

5) V<sub>FO</sub> output pulse width should be determined by connecting an external capacitor(C<sub>FOD</sub>) between C<sub>FOD</sub>(pin7) and COM(pin2). (Example : if C<sub>FOD</sub> = 33 nF, then t<sub>FO</sub> = 1.8ms (typ.)) Please refer to the note 5 for calculation method.

6) Input signal is High-Active type. There is a  $5k\Omega$  resistor inside the IC to pull down each input signal line to GND. RC coupling circuits should be adopted for the prevention of input signal oscillation.  $R_S C_{PS}$  time constant should be selected in the range 50~150ns.  $C_{PS}$  should not be less than 1nF.(Recommended  $R_S$ =100 $\Omega$ ,  $C_{PS}$ =1nF)

7) To prevent errors of the protection function, the wiring around  $\mathsf{R}_\mathsf{F}$  and  $\mathsf{C}_\mathsf{SC}$  should be as short as possible.

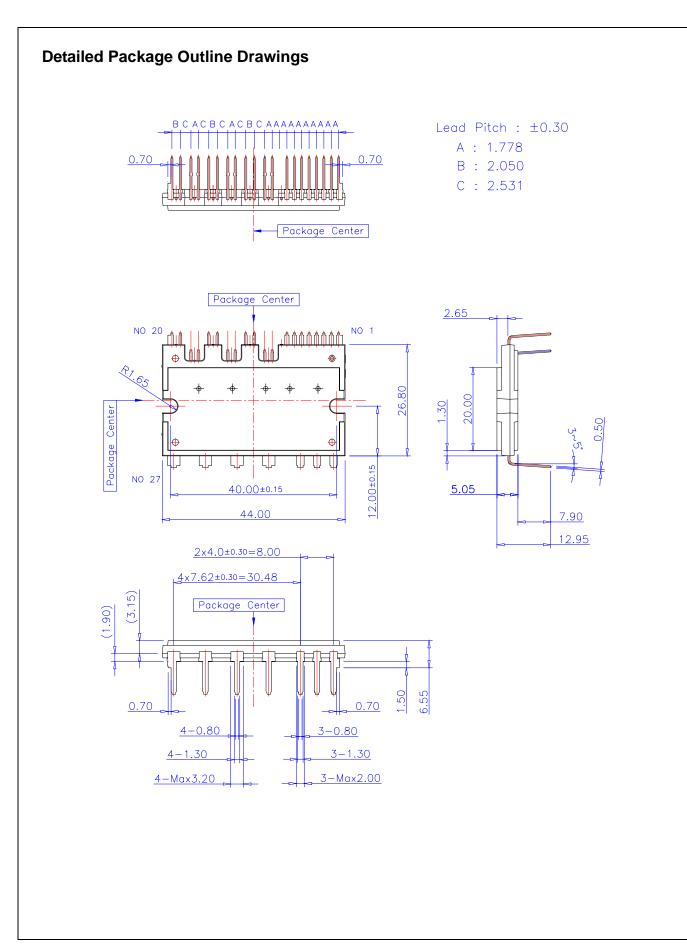
8) In the short-circuit protection circuit, please select the  $R_F C_{SC}$  time constant in the range 1.5~2  $\mu s.$ 

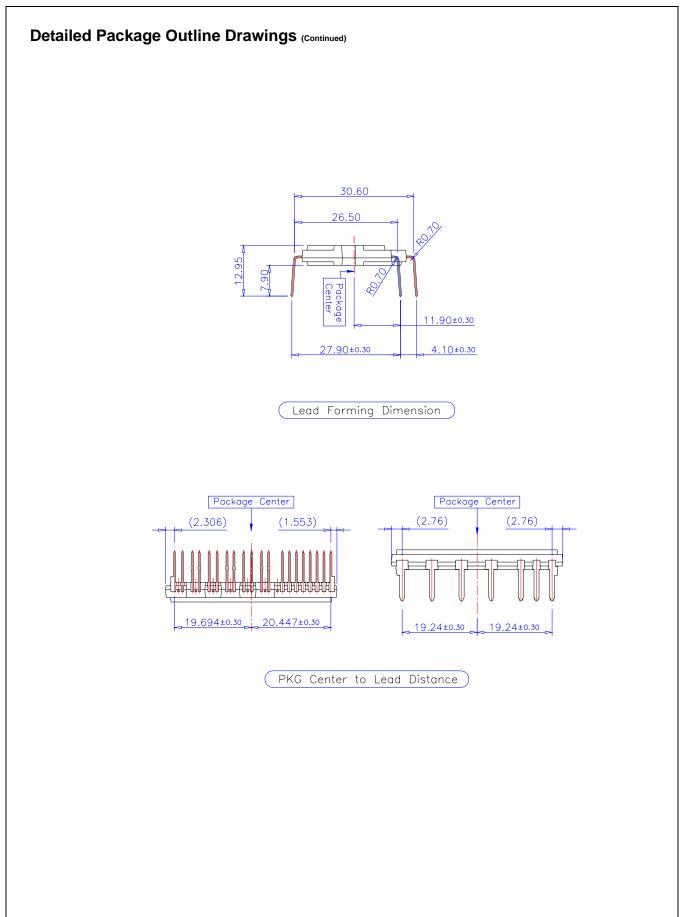
9) Each capacitor should be mounted as close to the pins of the SPM as possible.

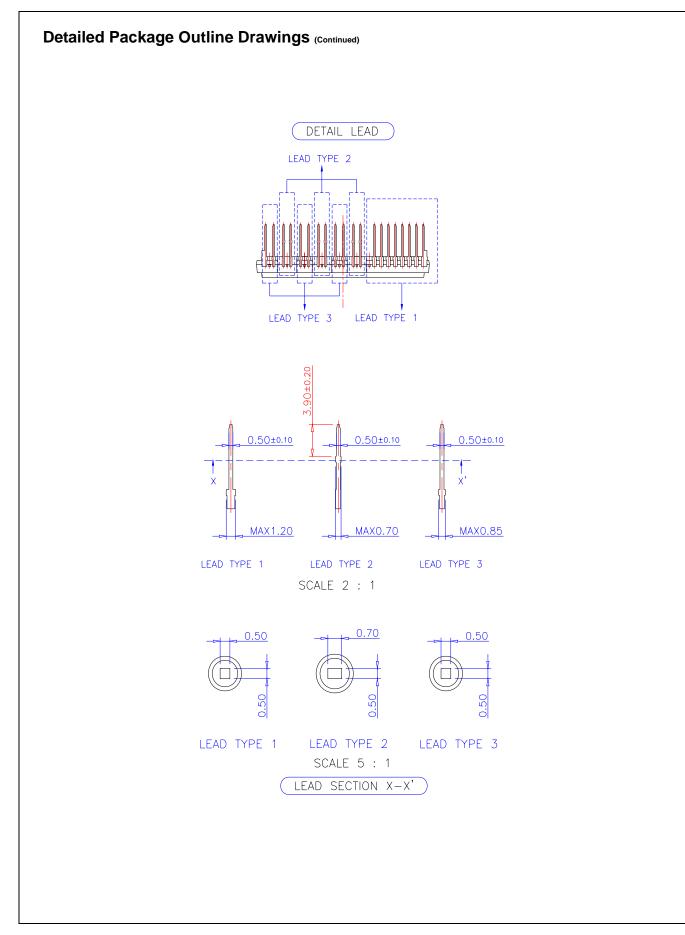
10) To prevent surge destruction, the wiring between the smoothing capacitor and the P&GND pins should be as short as possible. The use of a high frequency non-inductive capacitor of around 0.1~0.22µF between the P&GND pins is recommended.

11) Relays are used at almost every systems of electrical equipments of home appliances. In these cases, there should be sufficient distance between the CPU and the relays. 12)  $C_{SPC15}$  should be over 1µF and mounted as close to the pins of the SPM as possible.

### Figure 13. Typical Application Circuit









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GTO™ i-Lo™ IntelliMAX™ ISOPLANAR™ MegaBuck™ MICROCOUPLER™ MicroFET™ MicroPak™ Motion-SPM™ **OPTOLOGIC**<sup>®</sup> **OPTOPLANAR<sup>®</sup>** PDP-SPM™ Power220<sup>®</sup> Power247<sup>®</sup>

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No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
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