

FSB50450T Smart Power Module (SPM[®])

Features

- 500V 3.0A 3-phase FRFET inverter including high voltage integrated circuit (HVIC)
- 3 divided negative dc-link terminals for inverter current sensing applications
- HVIC for gate driving and undervoltage protection
- 3/5V CMOS/TTL compatible, active-high interface
- Optimized for low electromagnetic interference
- Isolation voltage rating of 1500Vrms for 1min.
- Extended VB pin for PCB isolation



General Description

FSB50450T is a tiny smart power module (SPM[®]) based on FRFET technology as a compact inverter solution for small power motor drive applications such as fan motors and water suppliers. It is composed of 6 fast-recovery MOSFET (FRFET), and 3 half-bridge HVICs for FRFET gate driving. FSB50450T provides low electromagnetic interference (EMI) characteristics with optimized switching speed. Moreover, since it employs FRFET as a power switch, it has much better ruggedness and larger safe operation area (SOA) than that of an IGBT-based power module or one-chip solution. The package is optimized for the thermal performance and compactness for the use in the built-in motor application and any other application where the assembly space is concerned. FSB50450T is the most solution for the compact inverter providing the energy efficiency, compactness, and low electromagnetic interference.



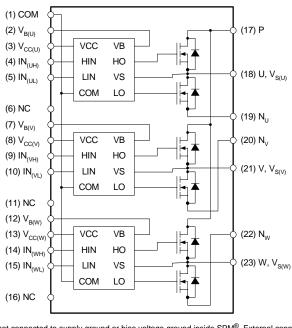
Absolute Maximum Ratings

Symbol	Parameter	Conditions	Rating	Units	
V _{PN}	DC Link Input Voltage, Drain-source Voltage of each FRFET		500	V	
I _{D25}	Each FRFET Drain Current, Continuous	$T_{\rm C} = 25^{\circ}{\rm C}$	1.5	А	
I _{D80}	Each FRFET Drain Current, Continuous	$T_{\rm C} = 100^{\circ}{\rm C}$	1.0	А	
I _{DP}	Each FRFET Drain Current, Peak	T _C = 25°C, PW < 100μs	3.0	А	
PD	Maximum Power Dissipation	$T_{C} = 25^{\circ}C$, Each FRFET	10	W	
V _{CC}	Control Supply Voltage	Applied between V _{CC} and COM	20	V	
V _{BS}	High-side Bias Voltage	Applied between V _{B(U)} -U, V _{B(V)} -V, V _{B(W)} -W	20	V	
V _{IN}	Input Signal Voltage	Applied between IN and COM	-0.3 ~ VCC+0.3	V	
TJ	Operating Junction Temperature		-20 ~ 150	°C	
T _{STG}	Storage Temperature		-50 ~ 150	°C	
R_{\thetaJC}	Junction to Case Thermal Resistance	Each FRFET under inverter operating con- dition (Note 1)	8.9	°C/W	
V _{ISO}	Isolation Voltage	60Hz, Sinusoidal, 1 minute, Connection pins to heatsink	1500	V _{rms}	

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Pin Descriptions

Pin Number	Pin Name	Pin Description	
1	СОМ	IC Common Supply Ground	
2	V _{B(U)}	Bias Voltage for U Phase High Side FRFET Driving	
3	V _{CC(U)}	Bias Voltage for U Phase IC and Low Side FRFET Driving	
4	IN _(UH)	Signal Input for U Phase High-side	
5	IN _(UL)	Signal Input for U Phase Low-side	
6	NC	No Connection	
7	V _{B(V)}	Bias Voltage for V Phase High Side FRFET Driving	
8	V _{CC(V)}	Bias Voltage for V Phase IC and Low Side FRFET Driving	
9	IN _(VH)	Signal Input for V Phase High-side	
10	IN _(VL)	Signal Input for V Phase Low-side	
11	NC	No Connection	
12	V _{B(W)}	Bias Voltage for W Phase High Side FRFET Driving	
13	V _{CC(W)}	Bias Voltage for W Phase IC and Low Side FRFET Driving	
14	IN _(WH)	Signal Input for W Phase High-side	
15	IN _(WL)	Signal Input for W Phase Low-side	
16	NC	No Connection	
17	Р	Positive DC-Link Input	
18	U, V _{S(U)}	Output for U Phase & Bias Voltage Ground for High Side FRFET Driving	
19	NU	Negative DC-Link Input for U Phase	
20	N _V	Negative DC-Link Input for V Phase	
21	V, V _{S(V)}	Output for V Phase & Bias Voltage Ground for High Side FRFET Driving	
22	N _W	Negative DC-Link Input for W Phase	
23	W, V _{S(W)}	Output for W Phase & Bias Voltage Ground for High Side FRFET Driving	



Note: Source terminal of each low-side MOSFET is not connected to supply ground or bias voltage ground inside SPM[®]. External connections should be made as indicated in Figure 2 and 5.

Figure 1. Pin Configuration and Internal Block Diagram (Bottom View)

Electrical Characteristics ($T_J = 25^{\circ}C$, $V_{CC} = V_{BS} = 15V$ Unless Otherwise Specified)

Inverter Part (Each FRFET Unless Otherwise Specified)

Symbol	Parameter	Conditions		Тур	Max	Units
BV _{DSS}	Drain-Source Breakdown Voltage	V _{IN} = 0V, I _D = 250μA (Note 2)		-	-	V
$\Delta BV_{DSS}/\Delta T_{J}$	Breakdown Voltage Tem- perature Coefficient	I _D = 250μA, Referenced to 25°C		0.53	-	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{IN} = 0V, V _{DS} = 500V	-	-	250	μΑ
R _{DS(on)}	Static Drain-Source On-Resistance	V _{CC} = V _{BS} = 15V, V _{IN} = 5V, I _D = 1.0A		1.9	2.4	Ω
V _{SD}	Drain-Source Diode Forward Voltage	$V_{CC} = V_{BS} = 15V, V_{IN} = 0V, I_D = -1.0A$		-	1.2	V
t _{ON}		V _{PN} = 300V, V _{CC} = V _{BS} = 15V, I _D = 1.0A	-	1152	-	ns
t _{OFF}		$V_{IN} = 0V \leftrightarrow 5V$ Inductive load L=3mH High- and low-side FRFET switching	-	600	-	ns
t _{rr}	Switching Times		-	185	-	ns
E _{ON}				85	-	μJ
E _{OFF}		(Note 3)		11	-	μJ
RBSOA	Reverse-bias Safe Oper- ating Area	$V_{PN} = 400V$, $V_{CC} = V_{BS} = 15V$, $I_D = I_{DP}$, $R_{EH} = 0\Omega$ $V_{DS}=BV_{DSS}$, $T_J = 150^{\circ}C$ High- and low-side FRFET switching (Note 4)	Full Square			

Control Part (Each HVIC Unless Otherwise Specified)

Symbol	Parameter	Conditions		Min	Тур	Max	Units
I _{QCC}	Quiescent V _{CC} Current	V _{CC} =15V, V _{IN} =0V	Applied between $V_{\mbox{\scriptsize CC}}$ and COM	-	-	160	μA
I _{QBS}	Quiescent V _{BS} Current	V _{BS} =15V, V _{IN} =0V	Applied between $V_{B(U)}$ -U, $V_{B(V)}$ -V, $V_{B(W)}$ -W	-	-	100	μA
UV _{CCD}	Low-side Undervoltage	V _{CC} Undervoltage Protection Detection Level		7.4	8.0	9.4	V
UV _{CCR}	Protection (Figure 6)	V _{CC} Undervoltage Protection Reset Level		8.0	8.9	9.8	V
UV _{BSD}	High-side Undervoltage	V _{BS} Undervoltage Protection Detection Level		7.4	8.0	9.4	V
UV _{BSR}	Protection (Figure 7)	V _{BS} Undervoltage Protection Reset Level		8.0	8.9	9.8	V
V _{IH}	ON Threshold Voltage	Logic High Level		3.0	-	-	V
V _{IL}	OFF Threshold Voltage	Logic Low Level	Applied between IN and COM	-	-	0.8	V
I _{IH}	Input Dice Current	$V_{IN} = 5V$	Applied between IN and COM	-	10	20	μA
I	Input Bias Current	$V_{IN} = 0V$	Applied between IN and COM	-	-	2	μA

Note:

1. For the measurement point of case temperature T_C , please refer to Figure 3 in page 4.

2. BV_{DSS} is the absolute maximum voltage rating between drain and source terminal of each FRFET inside SPM[®]. V_{PN} should be sufficiently less than this value considering the effect of the stray inductance so that V_{DS} should not exceed BV_{DSS} in any case.

 t_{ON} and t_{OFF} include the propagation delay time of the internal drive IC. Listed values are measured at the laboratory test condition, and they can be different according to the field applications due to the effect of different printed circuit boards and wirings. Please see Figure 4 for the switching time definition with the switching test circuit of Figure 5.

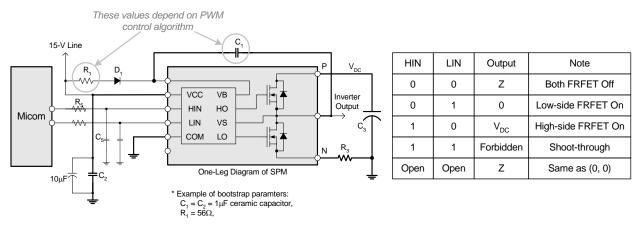
4. The peak current and voltage of each FRFET during the switching operation should be included in the safe operating area (SOA). Please see Figure 5 for the RBSOA test circuit that is same as the switching test circuit.

Package Marking & Ordering Information

Device Marking Device		Package	Reel Size	Tape Width	Quantity
FSB50450T	FSB50450T	SPM23AC	_	_	15

Recommended Operating Conditions

Symbol	Deremeter	Conditions	Value			Units	
Symbol	Parameter	Conditions	Min.	Тур.	Max.	Units	
V _{PN}	Supply Voltage	Applied between P and N	-	300	400	V	
V _{CC}	Control Supply Voltage	Applied between V_{CC} and COM	12	15	16.5	V	
V _{BS}	High-side Bias Voltage	Applied between V_B and output(U, V, W)	12	15	16.5	V	
V _{IN(ON)}	Input ON Threshold Voltage	Applied between IN and COM	3.0	-	V _{CC}	V	
V _{IN(OFF)}	Input OFF Threshold Voltage	Applied between in and COM	0	-	0.6	V	
t _{dead}	Blanking Time for Preventing Arm-short	$V_{CC}\text{=}V_{BS}\text{=}12 \sim 16.5 \text{V}, \ \textbf{T}_{J} \leq 150^{\circ}\text{C}$	1.0	-	-	μS	
f _{PWM}	PWM Switching Frequency	$T_J \le 150^{\circ}C$	-	15	-	kHz	
т _с	Case Temperature	$T_{J} \leq 150^{\circ}C$	-20	-	125	°C	



Note:

(1) It is recommended the bootstrap diode D_1 to have soft and fast recovery characteristics with 600-V rating

(2) Parameters for bootsrap circuit elements are dependent on PWM algorithm. For 15 kHz of switching frequency, typical example of parameters is shown above.

(3) RC coupling (R₅ and C₅) at each input (indicated as dotted lines) may be used to prevent improper input signal due to surge noise. Signal input of SPM[®] is compatible with standard CMOS or LSTTL outptus.

(4) Bold lines should be short and thick in PCB pattern to have small stray inductance of circuit, which results in the reduction of surge voltage. Bypass capacitors such as C₁, C₂ and C₃ should have good high-frequency characteristics to absorb high-frequency ripple current.

Figure 2. Recommended CPU Interface and Bootstrap Circuit with Parameters

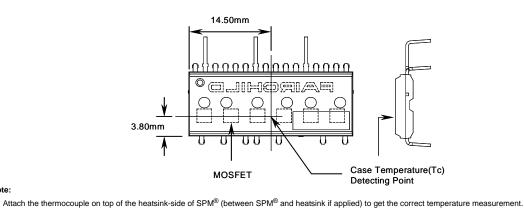
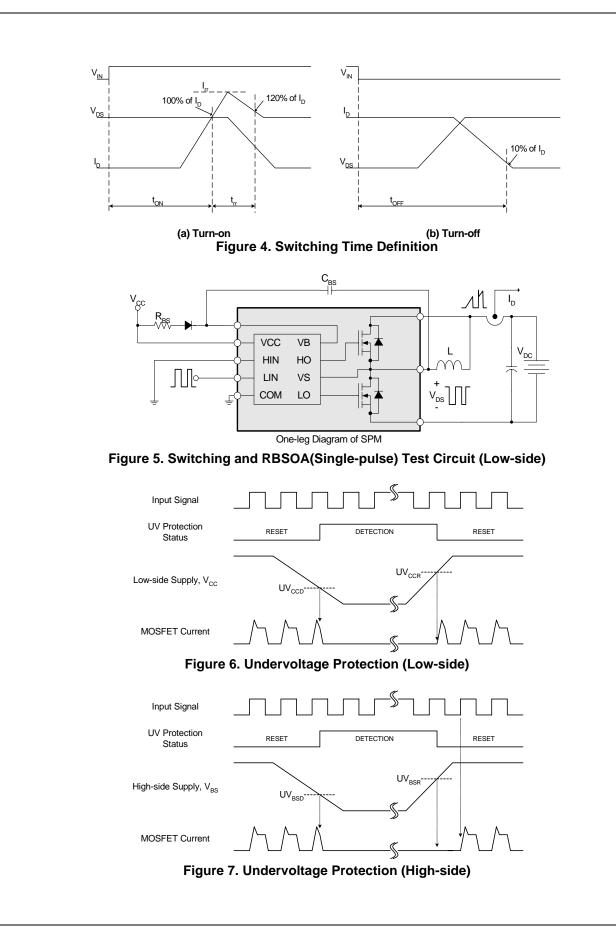


Figure 3. Case Temperature Measurement

Note:



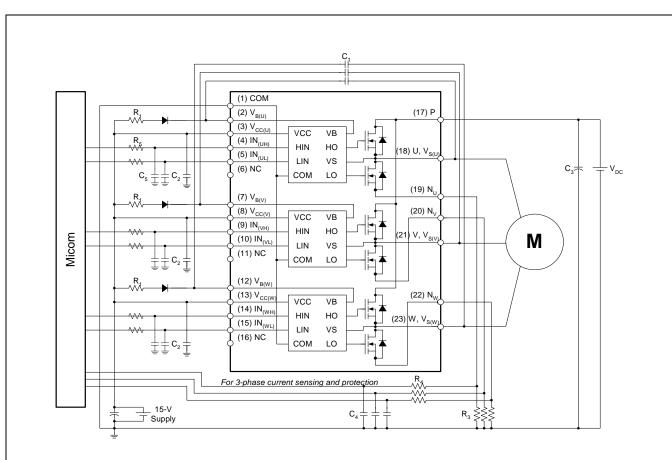
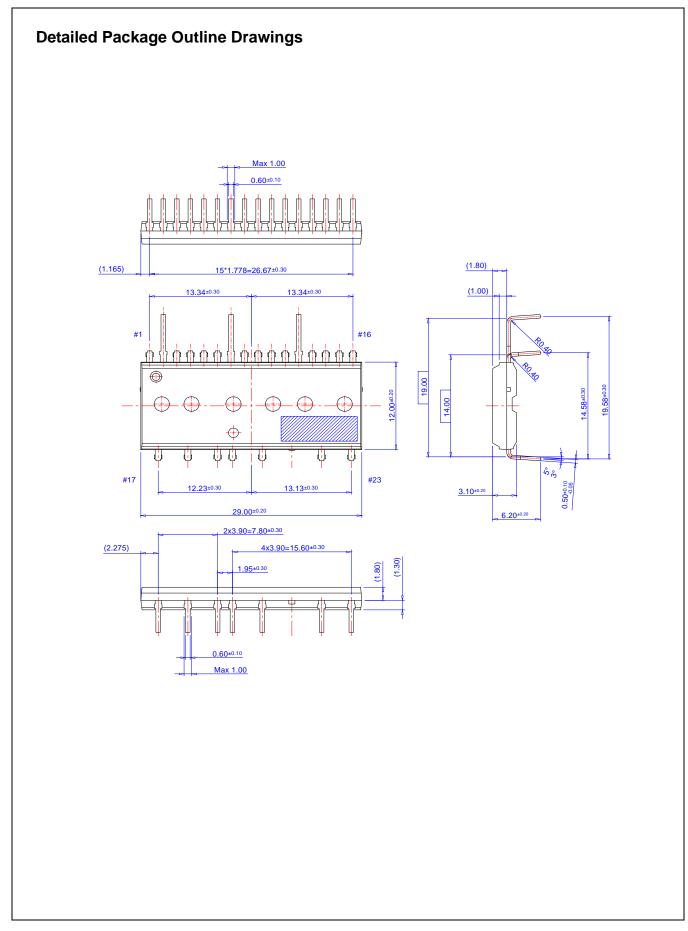


Figure 8. Example of Application Circuit



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