

April 2012

FSB117H / FSB127H / FSB147H mWSaver™ Fairchild Power Switch (FPS™)

Features

mWSaver™ Technology

- Achieve Low No-Load Power Consumption Less than 40mW at 230V_{AC} (EMI Filter Loss Included)
- Meets 2013 ErP Standby Power Regulation (Less than 0.5W Consumption with 0.25W Load) for ATX Power and LCD TV Power
- Eliminate X-Cap Discharge Resistor Loss with Ax-CAP™ Technology
- Linearly Decreased Switching Frequency at Light-Load Condition and Advanced Burst Mode Operation at No-Load Condition
- 700V High-Voltage JFET Startup Circuit to Eliminate the Startup Resistor Loss

Highly Integrated with Rich Features

- Internal Avalanche-Rugged 700V SenseFET
- Built-in 5ms Soft-Start
- Peak-Current-Mode Control
- Cycle-by-Cycle Current Limiting
- Leading-Edge Blanking (LEB)
- Synchronized Slope Compensation
- Proprietary Asynchronous Jitter to Reduce EMI

Advanced Protection

- Internal Overload / Open-Loop Protection (OLP)
- V_{DD} Under-Voltage Lockout (UVLO)
- V_{DD} Over-Voltage Protection (OVP)
- Constant Power Limit (Full AC Input Range)
- Internal Auto Restart Circuit (OLP, V_{DD} OVP, OTP)
- Internal OTP Sensor with Hysteresis
- Adjustable Peak Current Limit

Related Resources

- Evaluation Board: FEBFSB127H T001
- Fairchild Power Supply WebDesigner Flyback Design & Simulation - In Minutes at No Expense

Description

The FSB-series is a next-generation, green-mode Fairchild Power Switch (FPS™) incorporating Fairchild's innovative mWSaver™ technology, which dramatically reduces standby and no-load power consumption, enabling conformance to all worldwide Standby Mode efficiency guidelines. It integrates an advanced current-mode pulse width modulator (PWM) and an avalancherugged 700V SenseFET in a single package, allowing auxiliary power designs with higher standby energy efficiency, reduced size, improved reliability, and lower system cost than previous solutions.

Fairchild Semiconductor's mWSaver™ technology offers best-in-class minimum no-load and light-load power consumption. An innovative Ax-CAP™ method, one of the five proprietary mWSaver™ technologies, minimizes losses in the EMI filter stage by eliminating the X-cap discharge resistors while still meeting IEC61010-1 safety requirement. mWSaver™ Green Mode gradually decreases switching frequency as load decreases to minimize switching losses.

A new proprietary asynchronous jitter decreases EMI emission and built-in synchronized slope compensation allows stable peak-current-mode control over a wide range of input voltage. The proprietary internal line compensation ensures constant output power limit over entire universal line voltage range.

Requiring a minimum number of external components, the FSB-series provides a basic platform that is well suited for the cost-effective flyback converter design with low standby power consumption.

Applications

General-purpose switched-mode power supplies and flyback power converters, including:

- Auxiliary Power Supply for PC, Server, LCD TV, and Game Console
- SMPS for VCR, SVR, STB, DVD, and DVCD Player, Printer, Facsimile, and Scanner
- General Adapter
- LCD Monitor Power / Open-Frame SMPS

Ordering Information

Part Number	SenseFET	Operating Temperature Range	Package	Packing Method
FSB117HNY	1A 700V			
FSB127HNY	2A 700V	-40°C to +105°C	8-pin, Dual In-Line Package (DIP)	Tube
FSB147HNY	4A 700V			

Application Diagram

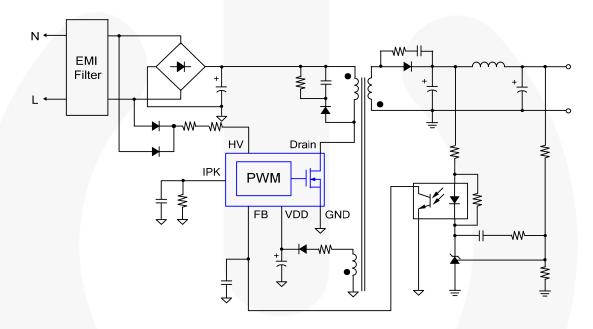


Figure 1. Typical Flyback Application

Table 1. Output Power Table⁽¹⁾

Product	230V _{AC}	±15% ⁽²⁾	85-265V _{AC}		
Product	Adapter ⁽³⁾	Open Frame ⁽⁴⁾	Adapter ⁽³⁾	Open Frame ⁽⁴⁾	
FSB117H	10W	15W	9W	13W	
FSB127H	14W	20W	11W	16W	
FSB147H	23W	35W	17W	26W	

Notes:

- 1. The maximum output power can be limited by junction temperature.
- 230 V_{AC} or 100/115 V_{AC} with voltage doubler.
- 3. Typical continuous power in a non-ventilated enclosed adapter with sufficient drain pattern of printed circuit board (PCB) as a heat sink, at 50°C ambient.
- 4. Maximum practical continuous power in an open-frame design with sufficient drain pattern of printed circuit board (PCB) as a heat sink, at 50°C ambient.

Internal Block Diagram Drain 5 6,7,8 Line Voltage Sample Circuit Auto-Re-start - OLP Protection-OTP Brownout Protection HV Startup Internal BIAS VDD 2 UVLO Clock Soft-Start Comparator 12V/6V Soft-Start Green Mode Current-Limit Comparator $V_{\text{Limit}} \\$ GND PWM Comparato V_{DD-OVP} 5.4V Slope Compensation Ō OSC2 Maximum Duty CycleLimit 3 FΒ

Figure 2. Block Diagram

OLP-

OLP Delay

OLP

Comparator

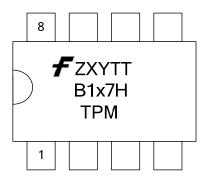
R≸

4.6V

I_{PK}(▼)50μA

Current Limit Compensation

Pin Configuration



F – Fairchild Logo

Z - Plant Code

X – 1-Digit Year Code

Y – 1-Digit Week Code

TT – 2-Digit Die Run Code

T – Package Type (N: DIP)

P – Y: Green Package

M – Manufacture Flow Code

Figure 3. Pin Configuration

Pin Definitions

Pin#	Name	Description
1	GND	Ground. This pin internally connects to the SenseFET source and signal ground of the PWM controller.
2	VDD	Supply voltage of the IC. Typically the holdup capacitor connects from this pin to ground. Rectifier diode in series with the transformer auxiliary winding connects to this pin to supply bias during normal operation.
3	FB	Feedback. The signal from the external compensation circuit connects to this pin. The PWM duty cycle is determined by comparing the signal on this pin and the internal current-sense signal.
4	IPK	Adjust peak current. Typically a resistor connects from this pin to the GND pin to program the current-limit level. The internal current source ($50\mu A$) introduces voltage drop across the resistor, which determines the current limit level of pulse-by-pulse current limit.
5	HV	Startup. Typically, resistors in series with diodes from the AC line connect to this pin to supply internal bias and to charge the external capacitor connected between the VDD pin and the GND pin during startup. This pin is also used to sense the line voltage for brownout protection and AC line disconnection detection.
6		
7	Drain	SenseFET drain. This pin is designed to directly drive the transformer.
8		

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter			Max.	Unit	
V_{DRAIN}	Drain Pin Voltage ^(5,6)			700	V	
		FSB117H		4.0		
I_{DM}	Drain Current Pulsed ⁽⁷⁾	FSB127H		8.0	Α	
		FSB147H ⁽⁹⁾		9.6		
		FSB117H		50		
E _{AS}	Single Pulsed Avalanche Energy ⁽⁸⁾	FSB127H		140	mJ	
		FSB147H		120		
V_{DD}	DC Supply Voltage			30	V	
V_{FB}	FB Pin Input Voltage		-0.3	7.0	V	
V_{IPK}	IPK Pin Input Voltage		-0.3	7.0	V	
V _{HV}	HV Pin Input Voltage			700	V	
P_D	Power Dissipation (T _A <50°C)			1.5	W	
T_J	Operating Junction Temperature		-40	Internally Limited ⁽¹⁰⁾	°C	
T _{STG}	Storage Temperature Range		-55	+150	°C	
T_L	Lead Soldering Temperature (Wave	Soldering or IR, 10 Seconds)	\	+260	°C	
	Electrostatic Discharge Capability,	Human Body Model: JESD22-A114	5.50			
ECD	All Pins Except HV Pin	Charged Device Model: JESD22-C101	2.00		10.7	
ESD	Electrostatic Discharge Capability,	Human Body Model: JESD22-A114	3.00		kV	
	All Pins Including HV Pin	Charged Device Model: JESD22-C101	1.25			

Notes:

- 5. All voltage values, except differential voltages, are given with respect to the network ground terminal.
- 6. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device.
- Non-repetitive rating: pulse width is limited by maximum junction temperature.
- 8. L=51mH, starting T_J=25°C.
- 9. L=14mH, starting T_J=25°C.
- 10. Internally limited by Over-Temperature Protection (OTP). Refer to Total.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	mbol Parameter		Max.	Unit
R _{HV}	Resistor Connect to HV Pin for Full Range Input Detection	150	250	kΩ

Thermal Resistance Table

Symbol Parameter		Тур.	Unit
θ_{JA}	Junction-to-Air Thermal Resistance	86	°C/W
Ψлт	Junction-to-Package Thermal Resistance ⁽¹¹⁾	20	°C/W

Note:

11. Measured on the package top surface.

Electrical Characteristics

 V_{DD} =15V, T_A =25°C unless otherwise specified.

Symbol	Parameter		Condition	Min.	Тур.	Max.	Unit	
SenseFET	Section ⁽¹²⁾					•	•	
BV _{DSS}	Drain-Source Breakdown Voltaç	је	V _{DS} =700V, V _{GS} =0V	700			٧	
			V _{DS} =700V, V _{GS} =0V			50		
I _{DSS}	Zero-Gate-Voltage Drain Currer	nt	V _{DS} =560V, V _{GS} =0V, T _C =125°C			200	μA	
		FSB117H	\/ -40\/ I -0.5A		8.8	11.0		
$R_{DS(ON)}$	Drain-Source On-State Resistance ⁽¹³⁾	FSB127H	V_{GS} =10V, I_{D} =0.5A		6.0	7.2	Ω	
	redistance	FSB147H	V _{GS} =10V, I _D =2.5A		2.3	2.7		
		FSB117H			250	325		
C_{ISS}	Input Capacitance	FSB127H	V_{GS} =0V, V_{DS} =25V, V		550	715	pF	
		FSB147H			450	500		
		FSB117H			25	33	pF	
Coss	Output Capacitance	FSB127H	V_{GS} =0V, V_{DS} =25V, V		38	50		
		FSB147H	1-1101112		60	72		
		FSB117H			10	15	pF	
C _{RSS}	Reverse Transfer Capacitance	FSB127H	V_{GS} =0V, V_{DS} =25V, V		17	26		
		FSB147H	1-1101112		7	21		
		FSB117H			12	34		
$t_{d(on)}$	Turn-On Delay	FSB127H	V _{DS} =350V, I _D =1.0A		20	50	ns	
		FSB147H			12	35		
		FSB117H			4	18		
tr	Rise Time	FSB127H	V _{DS} =350V, I _D =1.0A		15	40	ns	
		FSB147H			20	50		
		FSB117H			30	70		
$t_{d(off)}$	Turn-Off Delay	FSB127H	V _{DS} =350V, I _D =1.0A	7	55	120	ns	
		FSB147H	1		30	70		
		FSB117H		74	10	30	ns	
t _f	Fall Time	FSB127H	V _{DS} =350V, I _D =1.0A		25	60		
		FSB147H			16	42	1	

Continued on the following page...

Electrical Characteristics (Continued)

 V_{DD} =15V, T_A =25°C unless otherwise specified.

Symbol	Parameter	Condition	Min.	Тур.	Max.	Unit
Control S	Section					•
VDD Secti	on					
V _{DD-ON}	UVLO Start Threshold Voltage		11	12	13	V
V _{DD-OFF1}	UVLO Stop Threshold Voltage		5	6	7	V
V _{DD-OFF2}	I _{DD-OLP} Enable Threshold Voltage		8	9	10	V
$V_{\text{DD-OLP}}$	V _{DD} Voltage Threshold for HV Startup Turn- On at Protection Mode		5	6	7	V
I _{DD-ST}	Startup Supply Current	V _{DD-ON} – 0.16V			30	μA
I _{DD-OP1}	Operating Supply Current with Normal Switching Operation	V _{DD} =15V, V _{FB} =3V			3.8	mA
I _{DD-OP2}	Operating Supply Current without Switching Operation	V _{DD} =15V, V _{FB} =1V			1.8	mA
I _{DD-OLP}	Internal Sinking Current	V _{DD-OLP} + 0.1V	30	60	90	μA
$V_{\text{DD-OVP}}$	V _{DD} Over-Voltage Protection		27	28	29	V
t _{D-VDDOVP}	V _{DD} Over-Voltage Protection Debounce Time		70	140	210	μs
HV Section	n					
I _{HV}	Supply Current Drawn from HV Pin	HV=120V _{DC} , V _{DD} =0V with 10µF	1.5		5.0	mA
I _{HV-LC}	Leakage Current after Startup	HV=700V, V _{DD} =V _{DD-OFF1} +1V			10	μА
V _{AC-ON}	Brown-in Threshold Level (V _{DC})	DC Voltage Applied	105	110	115	V
V _{AC-OFF}	Brownout Threshold Level (V _{DC})	to HV Pin Through 200kΩ Resistor		V _{AC-ON} -10		V
t _{UVP}	Brownout Protection Time		0.8	1.2	1.6	S
Oscillator	Section					
fosc	Frequency in Nominal Mode	Center Frequency	94	100	106	kHz
IOSC	. ,	Hopping Range	±4.0	±6.0	±8.0	NI IZ
t _{HOP}	Hopping Period ⁽¹²⁾		//	20		ms
f _{OSC-G}	Green-Mode Frequency		20	23	26	kHz
f_{DV}	Frequency Variation vs. V _{DD} Deviation	V _{DD} =11V to 22V			5	%
f_{DT}	Frequency Variation vs. Temperature Deviation ⁽¹²⁾	T _A =-40 to 105°C			5	%

Continued on the following page...

Electrical Characteristics (Continued)

 V_{DD} =15V, T_A =25°C unless otherwise specified.

Symbol			Condition	Min.	Тур.	Max.	Unit
Feedback	Input Section			•			
A _V	Internal Voltage Dividing Factor of	FB Pin ⁽¹²⁾		1/4.5	1/4.0	1/3.5	V/V
Z _{FB}	Pull-Up Impedance of FB Pin			15	21	27	kΩ
V _{FB-OPEN}	FB Pin Pull-Up Voltage		FB Pin Open	5.2	5.4	5.6	V
V _{FB-OLP}	FB Voltage Threshold to Trigger C Protection)pen-Loop		4.3	4.6	4.9	V
t _{D-OLP}	Delay of FB Pin Open-Loop Protect	ction		46	56	66	ms
$V_{\text{FB-N}}$	FB Voltage Threshold to Exit Gree	en Mode	V _{FB} is Rising	2.4	2.6	2.8	V
V _{FB-G}	FB Voltage Threshold to enter Gre	een Mode	V _{FB} is Falling		V _{FB-N} -0.2		V
V _{FB-ZDC}	FB Voltage Threshold to Enter Zer State	ro-Duty	V _{FB} is Falling	1.95	2.05	2.15	V
V _{FB-ZDCR}	FB Voltage Threshold to Exit Zero	-Duty State	V _{FB} is Rising		V _{FB-ZDC} +0.1		V
IPK Pin Se	ection						
V _{IPK-OPEN}	IPK Pin Open Voltage			3.0	3.5	4.0	V
V _{IPK-H}	Internal Upper Clamping Voltage of	of IPK Pin				3 ⁽¹²⁾	V
V_{IPK-L}	Internal Lower Clamping Voltage of	of IPK Pin		1.5 ⁽¹²⁾			V
I _{PK}	Internal Current Source of IPK Pin		T _A =-40 to 105°C, V _{IPK} =2.25V	45	50	55	μΑ
	Current Limit Plateau when IPK	FSB117H		0.72	0.80	0.88	
I _{LMT-FL-H}	Pin Voltage is Internally Clamped	FSB127H	V _{IPK} =3V, Duty>40%	0.90	1.00	1.10	Α
	to Upper Limit	FSB147H	- Duty>40 /6	1.35	1.50	1.65	
		FSB117H			I _{LMT-FL-H} -0.20		
I _{LMT-VA-H}	Initial Current Limit when I _{PK} Pin Voltage is Internally Clamped to Upper Limit		V _{IPK} =3V, Duty=0%		I _{LMT-FL-H} -0.25		Α
	оррог Еши	FSB147H			I _{LMT-FL-H} - 0.37		
	Current Limit Plateau when IPK	FSB117H		0.36	0.40	0.44	
I _{LMT-FL-L}	Pin Voltage is Internally Clamped	FSB127H	V _{IPK} =1.5V, Duty>40%	0.45	0.50	0.55	Α
	to Lower Limit	FSB147H	Daty 40 70	0.67	0.75	0.83	1
		FSB117H			I _{LMT-FL-L} -0.10		
I _{LMT-VA-L}	Initial Current Limit when I _{PK} Pin Voltage is Internally Clamped to Lower Limit		V _{IPK} =1.5V, Duty=0%		I _{LMT-FL-L} -0.12		Α
	201101 211111	FSB147H			I _{LMT-FL-L} - 0.18	U	V

Continued on the following page...

Electrical Characteristics (Continued)

V_{DD}=15V, T_A=25°C unless otherwise specified.

Symbol	Parameter	Condition	Min.	Тур.	Max.	Unit
Current-Sen	se Section ⁽¹⁴⁾	•				•
t _{PD}	Current Limit Turn-Off Delay			100	200	ns
t _{LEB}	Leading-Edge Blanking Time		230	280	330	ns
t _{SS}	Soft-Start Time ⁽¹²⁾			5		ms
GATE Section	on ⁽¹⁴⁾					
DCY _{MAX}	Maximum Duty Cycle		70			%
Over-Tempe	erature Protection Section (OTP)					
T _{OTP}	Junction Temperature to trigger OTP ⁽¹²⁾		135	142	150	°C
ΔT_{OTP}	Hysteresis of OTP ⁽¹²⁾			25		°C

Notes:

- 12. Guaranteed by design; not 100% tested in production.
- 13. Pulse test: pulse width \leq 300µs, duty \leq 2%.
- 14. These parameters, although guaranteed, are tested in wafer-sort process.

Typical Characteristics

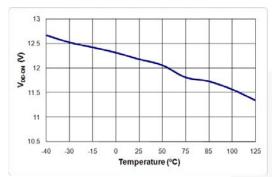


Figure 4. V_{DD-ON} vs. Temperature

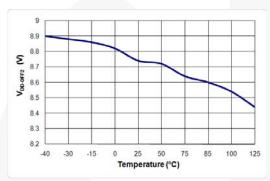


Figure 6. V_{DD-OFF2} vs. Temperature

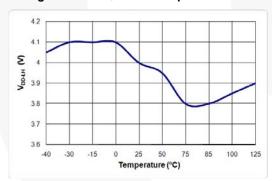


Figure 8. V_{DD-LH} vs. Temperature

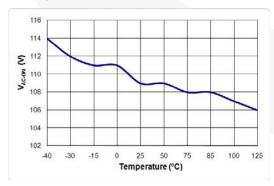


Figure 10. V_{AC-ON} vs. Temperature

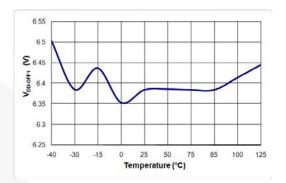


Figure 5. V_{DD-OFF1} vs. Temperature

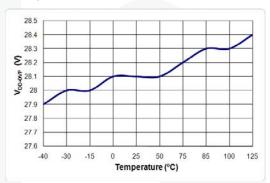


Figure 7. V_{DD-OVP} vs. Temperature

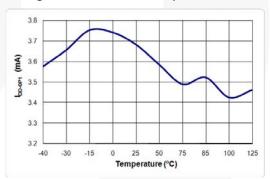


Figure 9. IDD-OP1 vs. Temperature

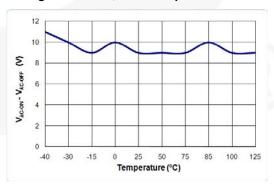


Figure 11. V_{AC-ON} – V_{AC-OFF} vs. Temperature

Typical Characteristics

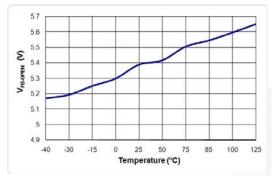


Figure 12. V_{FB-OPEN} vs. Temperature

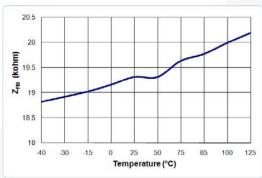


Figure 14. Z_{FB} vs. Temperature

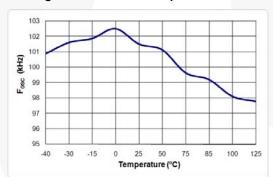


Figure 16. fosc vs. Temperature

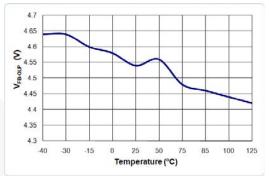


Figure 13. V_{FB-OLP} vs. Temperature

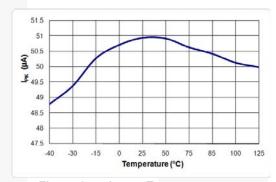


Figure 15. IPK vs. Temperature

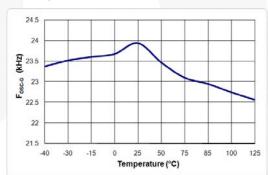


Figure 17. f_{OSC-G} vs. Temperature

Functional Description

Startup Operation

The HV pin is typically connected to the AC line input through two external diodes and one resistor (R_{HV}), as shown in Figure 18. When the AC line voltage is applied, the V_{DD} hold-up capacitor is charged by the line voltage through the diodes and resistor. After V_{DD} voltage reaches the turn-on threshold voltage (V_{DD-ON}), the startup circuit charging V_{DD} capacitor is switched off and V_{DD} is supplied by the auxiliary winding of the transformer. Once the FSB-series starts, it continues operation until V_{DD} drops below 6V ($V_{DD-OFF1}$). The IC startup time with a given AC line input voltage is:

$$t_{STARTUP} = R_{HV} \cdot C_{DD} \cdot \ln \frac{V_{AC-IN} \cdot \frac{2\sqrt{2}}{\pi}}{V_{AC-IN} \cdot \frac{2\sqrt{2}}{\pi} - V_{DD-ON}}$$
(1)

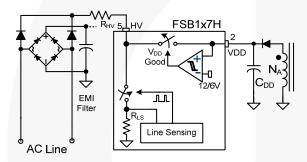


Figure 18. Startup Circuit

Brown-in/out Function

The HV pin can detect the AC line voltage using a switched voltage divider that consists of external resistor (R_{HV}) and internal resistor (R_{LS}), as shown in Figure 18. The internal line sensing circuit detects the real RMS value of the line voltage using sampling circuit and peak detection circuit. Since the voltage divider causes power consumption when it is switched on, the switching is driven by a signal with a very narrow pulse width to minimize power loss. The sampling frequency is adaptively changed according to the load condition to minimize the power consumption in light-load condition.

Based on the detected line voltage, brown-in and brownout thresholds are determined. Since the internal resistor (R_{LS}) of the voltage divider is much smaller than R_{HV} , the thresholds are given as:

$$V_{BROWN-IN}(RMS) = \frac{R_{HV}}{200k} \cdot \frac{V_{AC-ON}}{\sqrt{2}}$$
 (2)

$$V_{BROWN-OUT}(RMS) = \frac{R_{HV}}{200k} \cdot \frac{V_{AC-OFF}}{\sqrt{2}}$$
 (3)

PWM Control

The FSB-series employs current-mode control, as shown in Figure 19. An opto-coupler (such as the H11A817A) and shunt regulator (such as the KA431) are typically used to implement the feedback network. Comparing the feedback voltage with the voltage across the R_{sense} resistor makes it possible to control the switching duty cycle. A synchronized positive slope is added to the SenseFET current information to guarantee stable current-mode control over a wide range of input voltage. The built-in slope compensation stabilizes the current loop and prevents sub-harmonic oscillation.

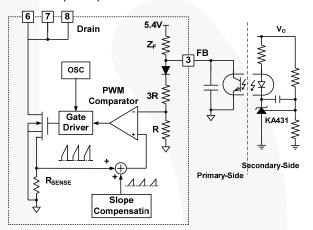


Figure 19. Current Mode Control

Soft-Start

The FSB-series has an internal soft-start circuit that progressively increases the pulse-by-pulse current limit level of MOSFET during startup to establish the correct working conditions for transformers and capacitors, as shown in Figure 20. The current limit levels have nine steps, as shown in Figure 21. This prevents transformer saturation and reduces stress on the secondary diode during startup.

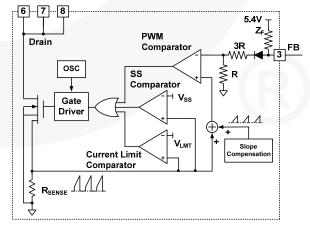


Figure 20. Soft-Start and Current-Limit Circuit

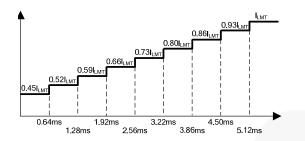


Figure 21. Current Limit Variation During Soft-Start

Adjustable Peak Current Limit & H/L Line Compensation for Constant Power Limit

To make the limited output power constant regardless of the line voltage condition, a special current-limit profile with sample and hold is used (as shown in Figure 22). The current-limit level is sampled and held at the falling edge of gate drive signal as shown in Figure 23. Then, the sampled current limit level is used for the next switching cycle. The sample-and-hold function prevents sub-harmonic oscillation in currentmode control.

The current-limit level increases as the duty cycle increases, which reduces the current limit as duty cycle decreases. This allows lower current-limit level for highline voltage condition where the duty cycle is smaller than that of low line. Therefore, the limited maximum output power can remain constant even for a wide input voltage range.

The peak current limit is programmable using a resistor on the IPK pin. The internal current 50µA source for the IPK pin generates voltage drop across the resistor. The voltage of the IPK pin determines the current-limit level. Since the upper and lower clamping voltage of the IPK pin are 3V and 1.5V, respectively, the suggested resistor value is from $30k\Omega$ to $60k\Omega$.

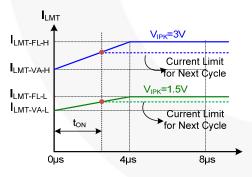


Figure 22. I_{LMT} vs. PWM Turn-On Time

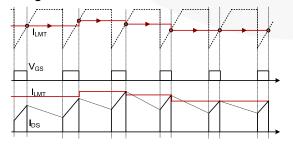


Figure 23. Current Limit Variation with Duty Cycle

mWSaver™ Technology

Ax-CAP[™] to Remove X-Cap Discharge Resistor

The EMI filter in the front end of the switched mode power supply typically includes a capacitor across the AC line connector, as shown in Figure 24. Most of the safety regulations, such as UL 1950 and IEC61010-1, require the capacitor be discharged to a safe level within a given time after unplugged from the power outlet. Typically a discharge resister across the capacitor is used to ensure the capacitor is discharged naturally, which however introduces power loss of the power supply. As power level increases, the EMI filter capacitor tends to increase, requiring a smaller discharge resistor to maintain same discharge time. This typically results in more power dissipation in high-power applications. The innovative Ax-CAP™ technology intelligently discharges the filter capacitor only when the power supply is unplugged from the power outlet. Since the Ax-CAP™ discharge circuit is disabled in normal operation, the power loss in the EMI filter size can be virtually removed.

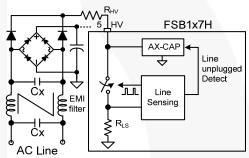


Figure 24. AX-Cap™ Circuit

Green Mode

The FSB-series modulates the PWM frequency as a function of FB voltage, as shown in Figure 25. Since the output power is proportional to the FB voltage in currentmode control, the switching frequency decreases as load decreases. In heavy-load conditions, the switching frequency is 100kHz. Once V_{FB} decreases below V_{FB-N} (2.6V), the PWM frequency linearly decreases from 100kHz to 23kHz to reduce switching losses at light-load condition. As V_{FB} decreases to V_{FB-G} (2.4V), the switching frequency is fixed at 23kHz.

As V_{FB} falls below V_{FB-ZDC} (2.1V), the FSB-series enters Burst Mode operation, where PWM switching is disabled. Then, the output voltage starts to drop, causing the feedback voltage to rise. Once V_{FR} rises above V_{FR}-ZDCR, switching resumes. Burst Mode alternately enables and disables switching, thereby reducing switching loss to reduce power consumption, as shown in Figure 26.

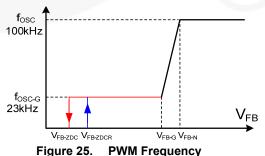


Figure 25.

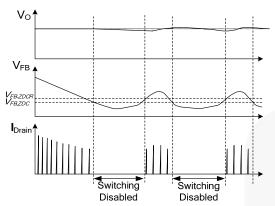


Figure 26. Burst-Mode Operation

Protections

The FSB-series provides protection function, that include Overload / Open-Loop Protection (OLP), Over-Voltage Protection (OVP), and Over-Temperature Protection (OTP). All the protections are implemented as Auto-Restart Mode. Once the fault condition is detected, switching is terminated and the SenseFET remains off. This causes V_{DD} to fall. When V_{DD} falls to 6V, the protection is reset and HV startup circuit charges V_{DD} up to 12V voltage, allowing re-startup.

Open-Loop / Overload Protection (OLP)

Because of the pulse-by-pulse current-limit capability, the maximum peak current through the SenseFET is limited and maximum input power is limited. If the output consumes more than the limited maximum power, the output voltage ($V_{\rm O}$) drops below the set voltage. Then the current through the opto-coupler LED and the transistor become virtually zero and FB voltage is pulled HIGH as shown in Figure 27. If feedback voltage is above 4.6V for longer than 56ms, OLP is triggered. This protection is also triggered when the feedback loop is open due to a soldering defect.

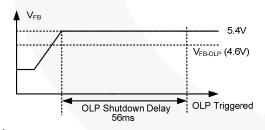


Figure 27. OLP Operation

V_{DD} Over-Voltage Protection (OVP)

If the secondary-side feedback circuit malfunctions or a solder defect causes an opening in the feedback path, the current through the opto-coupler transistor becomes virtually zero. Then feedback voltage climbs up in a similar manner to the overload situation, forcing the preset maximum current to be supplied to the SMPS until the overload protection triggers. Because more energy than required is provided to the output, the output voltage may exceed the rated voltage before the overload protection triggers, resulting in the breakdown of the devices in the secondary side. To prevent this situation, an OVP circuit is employed. Since V_{DD} voltage

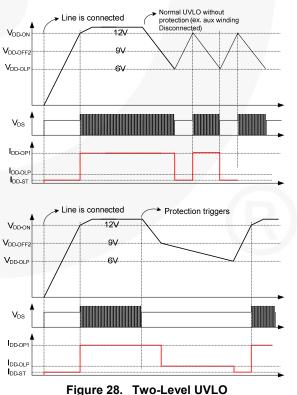
is proportional to the output voltage by the transformer coupling, the over voltage of output is indirectly detected using $V_{\rm DD}$ voltage. The OVP is triggered when $V_{\rm DD}$ voltage reaches 28V. Debounce time (typically 150 μ s) is applied to prevent false triggering by switching noise.

Over-Temperature Protection (OTP)

The SenseFET and the control IC are integrated in one package. This makes it easy for the control IC to detect the abnormal over temperature of the SenseFET. If the temperature exceeds approximately 140°C, the OTP is triggered and the MOSFET remains off. When the junction temperature drops by 25°C from OTP temperature, the FSB-series resumes normal operation.

Two-Level UVLO

Since all the protections of the FSB-series are autorestart, the power supply repeats shutdown and restartup until the fault condition is removed. FSB-series has two-level UVLO, which is enabled when protection is triggered, to delay the re-startup by slowing down the discharge of V_{DD}. This effectively reduces the input power of the power supply during the fault condition, minimizing the voltage/current stress of the switching devices. Figure 28 shows the normal UVLO operation and two-step UVLO operation. When V_{DD} drops to 6V without triggering the protection, PWM stops switching and V_{DD} is charged up by the HV startup circuit. Meanwhile, when the protection is triggered, FSB-series has a different V_{DD} discharge profile. Once the protection is triggered, the IC stops switching and V_{DD} drops. When V_{DD} drops to 9V, the operating current becomes very small and V_{DD} is slowly discharged. When V_{DD} is naturally discharged down to 6V, the protection is reset and V_{DD} is charged up by the HV startup circuit. Once V_{DD} reaches 12V, the IC resumes switching operation.



Typical Application Circuit

Application	Fairchild Devices	Input Voltage Range	Output
Standby Auxiliary Power	FSB127H	85V _{AC} ~ 265V _{AC}	5V/3.2A

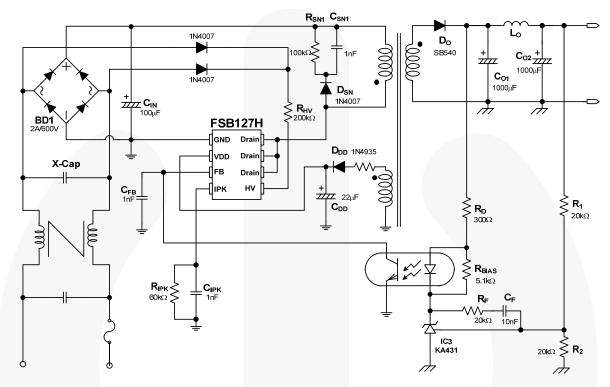


Figure 29. Schematic of Typical Application Circuit

Typical Application Circuit (Continued)

Transformer Specification

Core: El 22Bobbin: El 22

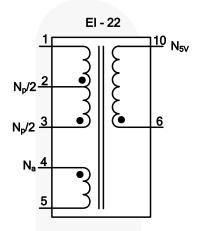


Figure 30. Transformer Specification

	$\textbf{Pin (S} \rightarrow \textbf{F)}$	Wire	Turns	Winding Method
Na	4 → 5	0.15φ×1	12	Solenoid Winding
Insulation: F	Polyester Tape t = 0.025mm	, 1-Layer		
N _p /2	3 → 2	0.27φ×1	31	Solenoid Winding
Insulation: F	Polyester Tape t = 0.025mm	, 2-Layer		
N _{5V}	6 → 10	0.55φ×2	5	Solenoid Winding
Insulation: F	Polyester Tape t = 0.025mm	, 2-Layer		
N _p /2	2 → 1	0.27φ×1	31	Solenoid Winding
Insulation: F	Polyester Tape t = 0.025mm	, 2-Layer		

	Pin	Specification	Remark
Primary-Side Inductance	1-3	900μH ±10%	100kHz, 1V
Primary-Side Effective Leakage	1-3	< 30μH Maximum	Short All Other Pins

Physical Dimensions 0.400 10.160 0.355 9.017 5 PIN 1 INDICATOR 0.280 **7**.112 0.240 6.096 0.015 [0.389] GAGE PLANE HALF LEAD 4X **FULL LEAD 4X** 0.005 [0.126] 0.005 [0.126] MIN 0.325 **8**.263 **7**.628 MAX 0.210 [5.334] **SEATING PLANE** 0.150 3.811 0.115 2.922 MIN 0.015 [0.381] 0.100 [2.540] 0.300 [7.618] 0.045 **1**.144 **0**.030 **0**.763 0.430 [10.922] MAX 0.070 [1.778] 4X 0.045 [1.143] ⊕ 0.10∭ C NOTES: A) THIS PACKAGE CONFORMS TO JEDEC MS-001 VARIATION BA B) CONTROLING DIMS ARE IN INCHES C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS. D) DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1982 E) DRAWING FILENAME AND REVSION: MKT-N08MREV1.

Figure 31. 8-Pin, Dual In-Line Package (DIP)

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings: http://www.fairchildsemi.com/packaging/.





TRADEMARKS

The following includes registered and unregistered trademarks and service marks, owned by Fairchild Semiconductor and/or its global subsidiaries, and is not intended to be an exhaustive list of all such trademarks.

F-PFS™ FRFET® AccuPower™ Global Power ResourceSM AX-CAPTM* GreenBridge™ BitSiC™ Green FPS™ Build it Now™ Green FPS™ e-Series™ CorePLUS™ Gmax™ CorePOWER™

GTO™ CROSSVOLT™ IntelliMAX™ CTL™ Current Transfer Logic™ ISOPLANAR™ DEUXPEED Making Small Speakers Sound Louder

Dual Cool™ EcoSPARK® MegaBuck™ MICROCOUPLER™ EfficientMax™ MicroFET™ **ESBC™**

18 Fairchild® Fairchild Semiconductor® FACT Quiet Series™ FACT FAST® FastvCore™

FETBench™ FlashWriter®* FPST

PowerTrench® PowerXS^T

Programmable Active Droop™

OFET OSTM Quiet Series™ RapidConfigure™

Saving our world, 1mW/W/kW at a time™

SignalWise™ SmartMax™ SMART START™

Solutions for Your Success™

SPM® STEALTH™ SuperFET[®] SuperSOT™-3 SuperSOT™-6 SuperSOT™-8 SupreMOS® SyncFET™ Sync-Lock™ SYSTEM GENERAL®* The Power Franchise® wer franchis

TinyBoost™ TinyBuck™ TinyCalc™ TinyLogic® TINYOPTO™ TinyPower™ TinyPWM™ TinyWire™ TranSiC™ TriFault Detect™ TRUECURRENT®* μSerDes™

UHC Ultra FRFET™ UniFET™ VCX™ VisualMax™ VoltagePlus™ XS™

and Better

MicroPak™

MicroPak2™

Miller Drive™

Motion Max™

mWSaver™

OptoHiT™

Motion-SPM™

OPTOLOGIC®

OPTOPI ANAR®

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION, OR DESIGN, FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

- Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
- A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

ANTI-COUNTERFEITING POLICY

Fairchild Semiconductor Corporation's Anti-Counterfeiting Policy. Fairchild's Anti-Counterfeiting Policy is also stated on our external website, www.fairchildsemi.com, under Sales Support.

Counterfeiting of semiconductor parts is a growing problem in the industry. All manufacturers of semiconductor products are experiencing counterfeiting of their parts. Customers who inadvertently purchase counterfeit parts experience many problems such as loss of brand reputation, substandard performance, failed applications, and increased cost of production and manufacturing delays. Fairchild is taking strong measures to protect ourselves and our customers from the proliferation of counterfeit parts. Fairchild strongly encourages customers to purchase Fairchild parts either directly from Fairchild or from Authorized Fairchild Distributors who are listed by country on our web page cited above. Products customers buy either from Fairchild directly or from Authorized Fairchild Distributors are genuine parts, have full traceability, meet Fairchild's quality standards for handling and storage and provide access to Fairchild's full range of up-to-date technical and product information. Fairchild and our Authorized Distributors will stand behind all warranties and will appropriately address any warranty issues that may arise. Fairchild will not provide any warranty coverage or other assistance for parts bought from Unauthorized Sources. Fairchild is committed to combat this global problem and encourage our customers to do their part in stopping this practice by buying direct or from authorized distributors.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition	
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.	
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.	
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.	
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.	

Rev. 161

^{*} Trademarks of System General Corporation, used under license by Fairchild Semiconductor,