

FSA644 — 2:1 MIPI D-PHY (1.5Gbps) 4-Data Lane Switch

Features

Switch Type	SPDT (10x)
Signal Types	MIPI, D-PHY
V _{CC}	1.65 to 4.5 V
Input Signals	0 to V _{CC}
R _{ON}	6 Ω Typical HS MIPI 8 Ω Typical LP MIPI
ΔR _{ON}	0.6 Ω Typical HS & LP MIPI
R _{ON_FLAT}	0.3 Ω Typical
I _{CCZ}	5 μA Maximum
I _{CC}	32 μA Maximum
O _{IRR}	-40 dB Typical
X _{TALK}	-25 dB Typical
Bandwidth	1100 MHz Minimum
Channel-to-Channel Skew	6 ps Typical
C _{ON}	5.2 pF
Operating Temperature	-40 to +85°C
Package	36-Ball WLCSP
Top Mark	M7
Ordering Information	FSA644UCX

Description

The FSA644 is a four-data-lane, MIPI, D-PHY switch. This single-pole, double-throw (SPDT) switch is optimized for switching between two high-speed or low-power MIPI sources. The FSA644 is designed for the MIPI specification and allows connection to a CSI or DSI module. The FSA644 features an extremely low on capacitance (C_{ON}) of 2.7 pF.

Applications

- Cellular Phones, Smart Phones
- Displays

Related Resources

- For samples and questions, please contact: analog.switch@fairchildsemi.com.
- FSA644 Demonstration Board

Typical Application

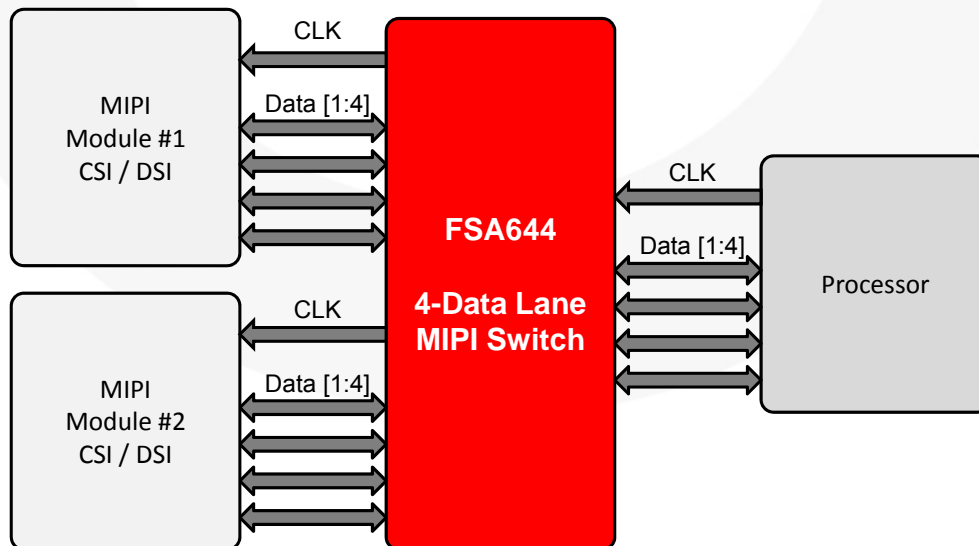


Figure 1. Mobile Phone Example

Pin Descriptions

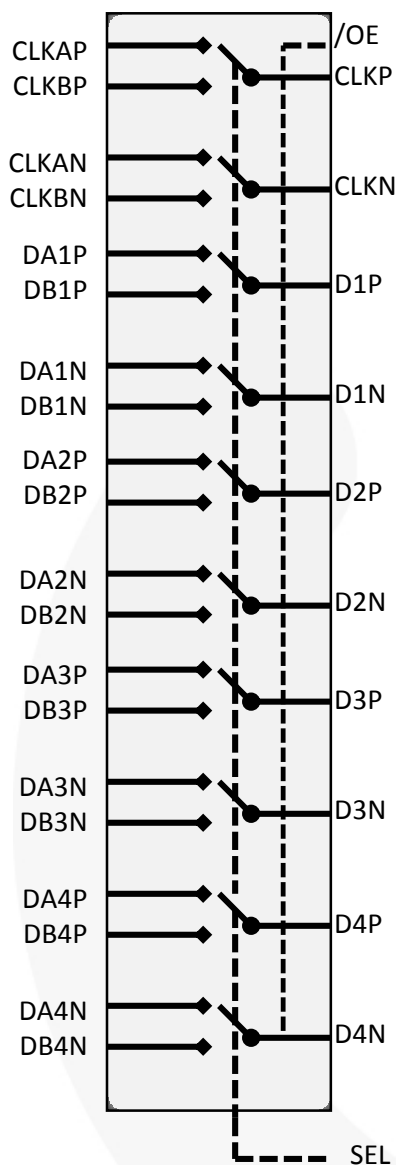


Figure 2. Analog Symbol

Pin Name		Description	
CLK _{P/N}		Common Clock Path	
D1 _{P/N}		Common Data Path 1	
D2 _{P/N}		Common Data Path 2	
D3 _{P/N}		Common Data Path 3	
D4 _{P/N}		Common Data Path 4	
CLKA _{P/N}		A-Side Clock Path	
DA1 _{P/N}		A-Side Data Path 1	
DA2 _{P/N}		A-Side Data Path 2	
DA3 _{P/N}		A-Side Data Path 3	
DA4 _{P/N}		A-Side Data Path 4	
CLKB _{P/N}		B-Side Clock Path	
DB1 _{P/N}		B-Side Data Path 1	
DB2 _{P/N}		B-Side Data Path 2	
DB3 _{P/N}		B-Side Data Path 3	
DB4 _{P/N}		B-Side Data Path 4	
SEL	Control Pin	SEL=0	CLKP=CLKAP, CLKN=CLKAN, Dn(P/N)=DAn(P/N)
		SEL=1	CLKP=CLKBP, CLKN=CLKBN, Dn(P/N)=DBn(P/N)
/OE		Output Enable	
V _{CC}		Power	
GND		Ground	
NC _n		No Connect	

Pin Definitions

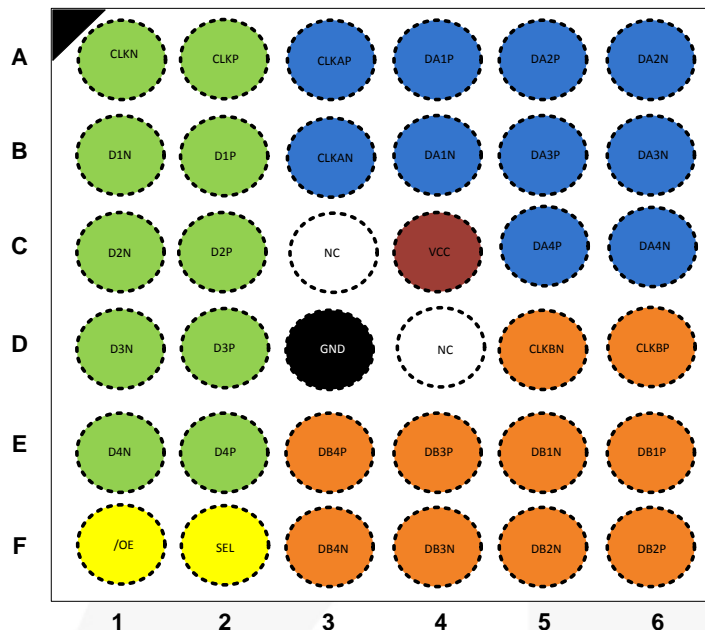


Figure 3. Top Through View

Table 1. Ball-to-Pin Mappings

Ball	Pin Name
A1	CLK _N
A2	CLK _P
A3	CLKA _P
A4	DA1 _P
A5	DA2 _P
A6	DA2 _N
B1	D1 _N
B2	D1 _P
B3	CLKA _N
B4	DA1 _N
B5	DA3 _P
B6	DA3 _N
C1	D2 _N
C2	D2 _P
C3	NC
C4	V _{CC}
C5	DA4 _P
C6	DA4 _N
D1	D3 _N
D2	D3 _P
D3	GND
D4	NC
D5	CLKB _N
D6	CLKB _P
E1	D4 _N
E2	D4 _P
E3	DB4 _P
E4	DB3 _P
E5	DB1 _N
E6	DB1 _P
F1	/OE
F2	SEL
F3	DB4 _N
F4	DB3 _N
F5	DB2 _N
F6	DB2 _P

Truth Table

SEL	/OE	Function
LOW	LOW	CLK _P =CLKA _P , CLK _N =CLKA _N , Dn(P/N)=DAn(P/N)
HIGH	LOW	CLK _P =CLKB _P , CLK _N =CLKB _N , Dn(P/N)=DBn(P/N)
X	HIGH	DAn(P/N), DBn(P/N) Data Ports High Impedance

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit
V _{CC}	Supply Voltage	-0.50	+5.25	V
V _{CNTRL}	DC Input Voltage (/OE) ⁽¹⁾	-0.5	V _{CC}	V
V _{SW}	DC Switch I/O Voltage ⁽¹⁾	-0.50	5.25	V
I _{IK}	DC Input Diode Current	-50		mA
I _{OUT}	DC Output Current		50	mA
T _{STG}	Storage Temperature	-65	+150	°C
ESD	Human Body Model, JEDEC: JESD22-A114	All Pins	3.5	kV
		I/O to GND	3.5	
		Power to GND	8.0	
	Charged Device Model, JEDEC: JESD22-C101		1.5	
	IEC 61000-4-2 System	Contact	8.0	
		Air Gap	15.0	

Note:

- The input and output negative ratings may be exceeded if the input and output diode current ratings are observed.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
V _{CC}	Supply Voltage	1.65	4.50	V
V _{CNTRL}	Control Input Voltage (S, /OE) ⁽²⁾	0	V _{CC}	V
V _{SW}	Switch I/O Voltage (CLKn, CLKA _n , CLKB _n , D _n , DAn, DBn)	HS Mode	0.1	V
		LP Mode	0	
T _A	Operating Temperature	-40	+85	°C

Note:

- The control input must be held HIGH or LOW; it must not float.

DC Electrical Characteristics

All typical values are at $T_A=25^\circ\text{C}$ unless otherwise specified.

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A=-40^\circ\text{C}$ to $+85^\circ\text{C}$			Unit
				Min.	Typ.	Max.	
V_{IK}	Clamp Diode Voltage	$I_{IN}=-18\text{ mA}$	2.8			-1.2	V
V_{IH}	Input Voltage High		1.65 to 4.5	1.0			V
V_{IL}	Input Voltage Low		1.65 to 4.5			0.5	V
I_{IN}	Control Input Leakage (SEL,/OE)	$V_{SW}=0$ to V_{CC}	1.65 to 4.5	-100		100	nA
$I_{NO(OFF)}, I_{NC(OFF)}$	Off Leakage Current of Port CLKn, DAn, CLKBn, DBn	CLKn, Dn=0.3 V; $V_{CC}=0.3\text{ V}$; CLKn, DAn, or CLKBn; DBn= $V_{CC}-0.3\text{ V}$, 0.3 V, or Floating; /OE=0 V	1.65 to 4.5	-100		100	nA
$I_{A(ON)}$	On Leakage Current of Common Ports (CLKn, Dn)	CLKn, Dn = 0.3 V; $V_{CC}=0.3\text{ V}$; CLKn, DAn, or CLKBn; DBn= $V_{CC}-0.3\text{ V}$, 0.3 V, or Floating; /OE=0 V	1.65 to 4.5	-100		100	nA
I_{OFF}	Power-Off Leakage Current	CLKn, Dn, or CLKn; DAn or CLKBn, DBn; $V_{IN}=0\text{ V}$ to 4.5 V; $V_{CC}=0\text{ V}$	0	-100		100	nA
I_{OZ}	Off-State Leakage	$0 \leq$ CLKn, Dn, CLKn, CLKBn, DAn, DBn $\leq 3.6\text{ V}$, /OE=High	4.5	-100		100	nA
$R_{ON_MIPI_HS}$	Switch On Resistance for HS MIPI Applications ⁽³⁾	$I_{ON}=-10\text{ mA}$, /OE=0 V, SEL= V_{CC} or 0V, CLK _{A, B} , DBn or DAn=0.1, 0.2, 0.3	1.8		7	12	Ω
			2.5		6	9	
			3.6		6	9	
			4.5		6	9	
$R_{ON_MIPI_LP}$	Switch On Resistance for LP MIPI Applications ⁽³⁾	$I_{ON}=-10\text{ mA}$, /OE=0 V, SEL= V_{CC} or 0V, CLK _{A, B} , DBn or DAn=0, 0.6, 1.2 V	1.8		6.7	12.0	Ω
			2.5		6.4	9.0	
			3.6		6.2	9.0	
			4.5		6.0	9.0	
$\Delta R_{ON_MIPI_HS}$	On Resistance Matching Between HS MIPI Channels ⁽⁴⁾	$I_{ON}=-10\text{ mA}$, /OE=0 V, SEL= V_{CC} or 0 V, CLK _{A, B} , DBn or DAn=0.1, 0.2, 0.3	1.8		0.8		Ω
			2.5		0.6		
			3.6		0.5		
			4.5		0.5		
$\Delta R_{ON_MIPI_LP}$	On Resistance Matching Between LP MIPI Channels ⁽⁴⁾	$I_{ON}=-10\text{ mA}$, /OE=0 V, SEL= V_{CC} or 0 V, CLK _{A, B} , DBn or DAn= 0.0, 0.6, 1.2 V	1.8		0.8		Ω
			2.5		0.6		
			3.6		0.5		
			4.5		0.5		
$R_{ON_FLAT_MIPI_HS}$	On Resistance Flatness for HS MIPI Signals ⁽⁴⁾	$I_{ON}=-10\text{ mA}$, /OE=0 V, SEL= V_{CC} or 0 V, CLK _{A, B} , DBn or DAn=0.1, 0.2, 0.3	1.8		1.5		Ω
			2.5		0.5		
			3.6		0.3		
			4.5		0.2		
$R_{ON_FLAT_MIPI_LP}$	On Resistance Flatness for LP MIPI Signals ⁽⁴⁾	$I_{ON}=-10\text{ mA}$, /OE=0 V, SEL= V_{CC} or 0 V, CLK _{A, B} , DBn or DAn=0.0, 0.6, 1.2 V	1.8		35		Ω
			2.5		2		
			3.6		1		
			4.5		0.5		

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DC Electrical Characteristics

All typical values are at $T_A=25^\circ\text{C}$ unless otherwise specified.

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A=-40^\circ\text{C}$ to $+85^\circ\text{C}$			Unit
				Min.	Typ.	Max.	
I_{CCZ}	Quiescent Hi-Z Supply Current	$V_{IN}=0$ or V_{CC} , $I_{OUT}=0$	4.5			0.5	μA
I_{CC}	Quiescent Supply Current	$V_{IN}=0$ or V_{CC} , $I_{OUT}=0$	2.5 to 4.5			32	μA
			1.8			22	
I_{CCT}	Increase in I_{CC} Current Per Control Voltage and V_{CC}	$V_{SEL/OE}=1.65\text{ V}$	4.5			4	μA
			2.5			0.1	

Notes:

- Measured by the voltage drop between A and B pins at the indicated current through the switch. On resistance is determined by the lower of the voltage on the two (A or B ports).
- Guaranteed by characterization.

AC Electrical Characteristics

All typical values are for $V_{CC}=3.3\text{V}$ at $T_A=25^\circ\text{C}$ unless otherwise specified.

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A=-40^\circ\text{C}$ to $+85^\circ\text{C}$			Units
				Min.	Typ.	Max.	
t_{INIT}	Initialization Time V_{CC} to Output ⁽⁵⁾	$R_L=50\ \Omega$, $C_L=5\ \text{pF}$, $V_{SW}=1.2\ \text{V}$	2.5 to 4.5			100	μs
			1.8			150	
t_{EN}	Enable Turn-On Time, /OE to Output	$R_L=50\ \Omega$, $C_L=5\ \text{pF}$, $V_{SW}=1.2\ \text{V}$	2.5 to 4.5		120	200	μs
			1.8		250	500	
t_{DIS}	Disable Turn-Off Time, /OE to Output	$R_L=50\ \Omega$, $C_L=5\ \text{pF}$, $V_{SW}=1.2\ \text{V}$	2.5 to 4.5		25	50	ns
			1.8		50	90	
t_{ON}	Turn-On Time, SEL to Output	$R_L=50\ \Omega$, $C_L=5\ \text{pF}$, $V_{SW}=1.2\ \text{V}$	2.5 to 4.5		50	100	ns
			1.8		75	125	
t_{OFF}	Turn-Off Time SEL to Output	$R_L=50\ \Omega$, $C_L=5\ \text{pF}$, $V_{SW}=1.2\ \text{V}$	2.5 to 4.5		50	200	ns
			1.8		200	325	
t_{BBM}	Break-Before-Make Time	$R_L=50\ \Omega$, $C_L=5\ \text{pF}$, $V_{SW}=1.2\ \text{V}$		10	50		ns
O_{IRR}	Off Isolation for MIPI ⁽⁵⁾	$R_L=50\ \Omega$, $f=750\ \text{MHz}$, /OE= V_{CC} $V_{SW}=-1\ \text{dBm}$ (200 mV _{PP})	1.65 to 4.5		-18		dB
X_{TALK}	Crosstalk for MIPI ⁽⁵⁾	$R_L=50\ \Omega$, $f=750\ \text{MHz}$, $V_{SW}=-1\ \text{dBm}$ (200 mV _{PP})	1.65 to 4.5		-25		dB
BW	-3db Bandwidth ⁽⁵⁾	$R_L=50\ \Omega$, $C_L=0\ \text{pF}$	3.0	1100	1600		MHz
S_{DD21}	Differential Data Rate	Inter-operability Data Rate	3.0		1.5		Gbps

Note:

- Guaranteed by characterization.

High-Speed-Related AC Electrical Characteristics

Symbol	Parameter	Conditions	V _{CC} (V)	T _A =- 40°C to +85°C			Units
				Min.	Typ.	Max.	
t _{SK(O)}	Channel-to-Channel Single-Ended Skew ⁽⁶⁾	TDR-Based Method (V _{SW} =0.2 V _{PP} , C _L =C _{ON})	3.3		6	20	ps
t _{SK(P)}	Skew of Opposite Transitions of the Same Output ⁽⁶⁾	TDR-Based Method (V _{SW} =0.2 V _{PP} , C _L =C _{ON})	3.3		6	20	ps

Note:

6. Guaranteed by characterization.

Capacitance

Symbol	Parameter	Conditions	T _A =- 40°C to +85°C			Units
			Min.	Typ.	Max.	
C _{IN}	Control Pin Input Capacitance	V _{CC} =0 V, f=1 MHz		2.1		pF
C _{ON}	Out On Capacitance	V _{CC} =3.3 V, /OE=0 V, f=1 MHz		5.2		
C _{OFF}	Out Off Capacitance	V _{CC} and /OE=3.3 V, f=1 MHz		2.0		

Physical Dimensions

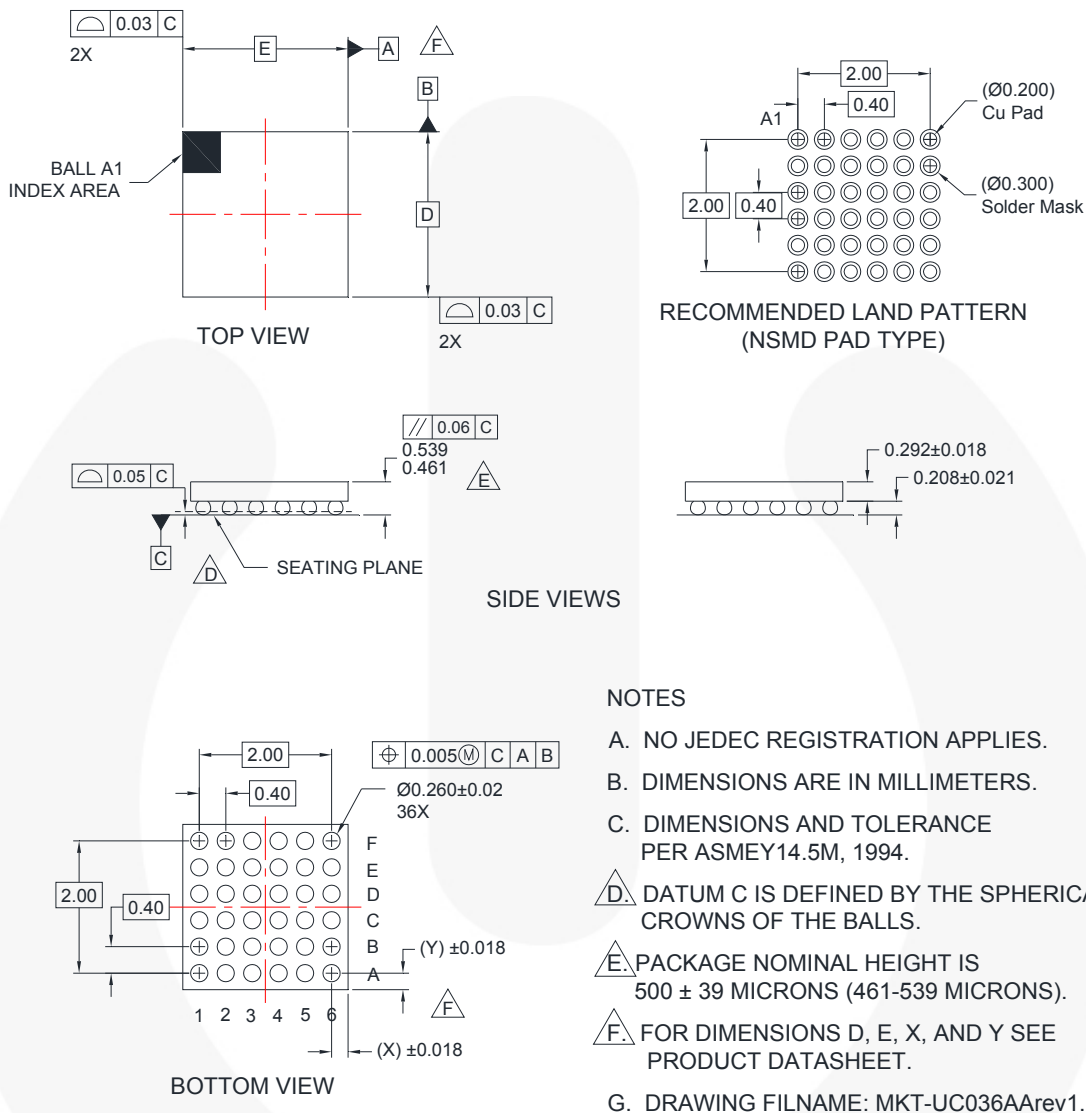


Figure 4. 36-Ball WLCSP, Non-JEDEC 2.4 mm x 2.4 mm, 0.4 mm Pitch

Ordering Information

Part Number	Top Mark	Package	D	E	X	Y
FSA644UCX	M7	36-Ball WLCSP, Non-JEDEC 2.4 mm x 2.4 mm, 0.4 mm Pitch	2.36 mm	2.36 mm	0.18 mm	0.18 mm






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